# Signetics Military Products Handbook, Volume 1

Signetics

Philips Components

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Military Products

# Military Products Handbook

Philips Components

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# Preface

**Military Products**

Signetics, since 1961, has been dedicated to manufacturing integrated circuits to the stringent requirements of the Defense and Aerospace Industries. Today, the commitment to this charter is evidenced by our continuing efforts to offer state-of-the-art processes and product technologies which result in unequalled overall product reliability.

As further evidence of the Signetics commitment to serve the specific needs of the Military and Aerospace marketplaces, all of the Signetics fabrication facilities are JAN certified. We also maintain a separate marketing and manufacturing organization dedicated to servicing the special needs of the Defense and Aerospace community.

Our mission is one of total customer satisfaction by providing industry leading products and uncompromised quality and responsiveness.

# Product Status

## DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| *Objective Specification* | Formative or In Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| *Preliminary Specification* | Preproduction Product | This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| *Product Specification* | Full Production | This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

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Military Products

# Section 1
# Introduction

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# Quality and Reliability

## Military Products

### SIGNETICS MILITARY PRODUCT QUALITY

Signetics Quality leadership begins with the Industry's first zero defect warranty. If a single defect is found in any lot that we ship, the entire lot may be sent back to the factory.

Since 1984, Signetics has adopted zero accept sampling plans in electrical, mechanical, and hermetic acceptance testing. Zero accept lot acceptance rates are typically 99.5% with any lot in which a defect is found being rescreened or scrapped.

The Department of Defense has issued contractor/vendor correlated quality objectives of less than 100 ppm by 1990. Signetics Estimated Process Quality (EPQ) in 1987 and 1988 was well under 100 ppm.

### SIGNETICS PPM PROGRAM

Signetics offers a unique PPM Program to all customers who are willing to commit resources to defect reduction. The program contains five basic steps:

1) The customer assigns an engineering contact to work defect analysis with a Signetics Quality Assurance Engineer (QAE).
2) Measurements are established at the customer's facility summarizing inspection data by product, test quantity and reported defects.
3) Each month this data is analyzed, compared to Signetics data, and a Parieto Analysis is generated to identify the top 10 suspect device types measured in ppm by Signetics QAE.
4) The customer agrees to send all defects found of these device types to the Signetics Assigned QAE regardless of lot dispositioning. (If the entire lot is returned, the defects remain segregated with the lot.)
5) Signetics will retest each and every reported defect and, if invalid, will return the devices to the customer's contact with complete variables data to substantiate the invalidation. If valid, Signetics will implement corrective action.

This process iteration continues until corrective action is complete. The next 10 suspect devices are then determined and the process is repeated until the overall customer ppm measurement agrees with Signetics data.

### SIGNETICS SHIP-TO-STOCK (STS) PROGRAM

Customers who have demonstrated the effectiveness of the PPM program may choose to reduce incoming inspection sampling, implement skip-lot sampling, or discontinue inspection completely. Signetics offers a proven STS program which provides for mutually agreeable device types to be shipped and received directly to the customer's stock with reduced or no receiving inspection. Signetics ppm database, as validated through the PPM Program, is monitored by Signetics QAE to assure continued defect-free performance. Acceptable candidates for STS are selected from the customer and Signetics ppm databases, where performance by device is agreed to be below 100 ppm (this is an arbitrary limit which can be negotiated with each customer).

Signetics QAE will again perform a Parieto Analysis based on device type, quantity shipped/received, and the reported defect levels. Those devices with a history of over 1000 devices shipped (again, arbitrary) and under 100 ppm are candidates for STS. Written agreement from the customer initiates the system. Shipments of STS certified material are uniquely labeled by Signetics for easy recognition by the customer's receiving group. Signetics QAE will continue to monitor the performance of these device types to assure less than 100 ppm defective on an ongoing basis. Should the Signetics performance exceed 100 ppm in a rolling 3 month period, Signetics will formally notify the customer that the device has been removed from STS and the customer's receiving inspection should be resumed. Similarly, the customer may abandon the system at any time, for any reason, simply by notifying the Signetics QAE.

Signetics Commercial Divisions have successfully implemented STS programs at over 82 customer locations, involving over 5100 device types. These customers enjoy the benefit of lower cost-of-ownership, reduced competition, and increased profits. STS is our customers reward for their investment in the PPM Program.

### SIGNETICS JUST-IN-TIME (JIT) PROGRAM

A further customer benefit of the PPM and STS Programs is the Just-in-Time Program. The Signetics JIT program supplements STS to assure defect-free, on-time delivery, while minimizing the customer's inventory. JIT is available to any participating STS customer, but only on those STS device types which are also on the customer's Volume Purchase Agreement (VPA) with Signetics. A firm VPA release of 6 months minimum will assure monthly, bi-weekly, or weekly defect-free shipments to the customer's stock. Contact Military Marketing for more information.

### SIGNETICS MILITARY PRODUCTS RELIABILITY

Signetics Reliability Assurance is involved throughout the initial design and process definition, characterization, product release, and production phases. Reliability organizations exist in each product group of Signetics, as well as in a Central Reliability group which establishes reliability standards and ongoing test programs. A well-defined reliability program not only assures quality and quality-over-time, but provides dependability, lower cost of ownership, and technical responsiveness to our customers.

Each Military product, new process, or revised product released to production must first pass the rigid commercial reliability standards, and then be qualified to Military Standards. Each Military die and package type are subjected to MIL-STD-883, Method 5005 Group C and D (die and packages, respectively) to demonstrate its suitability for Military usage. Thereafter, Quality Conformance Inspections conducted on each microcircuit group and package type on an annual basis, per paragraph 1.2.1 of MIL-STD-883.

The Corporate SURE Program also continuously monitors Commercial products with respect to processes and packages. The Military and SURE data bases together assure the Industry's highest reliable products. Further detail on the Signetics SURE Program may be found in any Signetics Commercial Data Manual, or contact your local sales representative to obtain a SURE Reliability Report.

### SIGNETICS MILITARY QUALITY IMPROVEMENT PROCESS

In 1980, Signetics recognized the need to improve product quality from the 10,000 ppm level to below 100 ppm. As evidenced by the preceding sections, the Quality Improvement Process has more than achieved that initial ppm quality goal. Today, Signetics strives to demonstrate continuous improvement in all business measures, including quality and service.

## Military Products

### MILITARY STANDARD PRODUCTS

The Signetics standard product line offering includes JAN qualified Class S and Class B products, Standard Military and DESC Drawings, and Class B and C vendor standard products.

All Signetics standard products are 100% screened to the requirements of the most current issue of MIL-STD-883, Method 5004, and periodically sampled to Quality Conformance Inspection (QCI), Method 5005. Signetics utilizes alternate Group A and alternate Group B for all product lines. The details of these test methods, as well as additional related requirements of MIL-M-38510 and MIL-STD-883, are not repeated herein so as to not mislead our customers by errors or omission of requirements included in those specifications.

This product description supersedes all prior dated Military Product literature, including commercial data books containing Military Product electrical characteristics, flow descriptions, and package physical dimensions.

### JAN Qualified Products

Signetics JAN Class S and Class B products are produced on government certified production lines and are qualified by the Defense Electronics Supply Center (DESC) in Dayton, Ohio.

JAN Class S products represent the highest level of quality and reliability as prescribed by MIL-STD-454, Requirement 64 and by MIL-HDBK-217, and are recommended for use in the most critical of applications such as manned space and satellite use.

JAN Class B products are the procurement preference for all general Military applications such as avionics, missiles, computers, launch control, fire control, and critical ground support electronics.

JAN qualified products are fabricated, assembled, tested, and inspected in U.S. Government certified facilities in Sunnyvale, California, Orem, Utah, and Albuquerque, New Mexico.

DESC prohibits any customer imposed deviations or waivers on procurement of JAN products. Products must conform completely to government specifications and are verified by Signetics Quality Control.

JAN qualified products are listed on the Qualified Products List, QPL-38510, issued periodically by DESC. For current QPL information, customers may contact their local sales representative, Military Marketing or directly with DESC-EQM at (513) 296–6355. The JAN products listed herein should be considered valid only on its date of publication.

These categories of product conform to quality Levels S and B of MIL-HDBK-217 ($\pi_Q = 0.25$ for Class S, 1.0 for Class B).

### Standard Military Drawing (SMD)

DESC selected item drawings (mini-specs) were produced by DESC-ECS during the period of 1976-1986 to serve as an interim standard for use prior to the publication of a JAN detailed slash sheet.

Standard Military Drawings (SMD), introduced in 1986, fulfill the same needs as DESC Drawings, but are streamlined about the general requirements of compliant non-JAN device types as defined by MIL-STD-883, Paragraph 1.2.1.

Until a qualified JAN device is obtained, the SMD serves as the Class B standard procurement preference as defined by MIL-STD-454, Requirement 64.

All Signetics products offered as SMD's fully conform with MIL-STD-883, Paragraph 1.2.1 and to the detailed drawing. Final electrical, Group A, and end-point electrical tests are defined by the SMD.

SMD products are marked with the government part number in addition to the information shown in the standard marking section. The case outline designator is defined by MIL-M-38510, Appendix C or by the SMD.

Many SMD products are dual-marked with the Signetics Class B standard product part number.

This category of product conforms to Quality Level B-1 of MIL-HDBK-217 ($\pi_Q = 2.0$)

### Signetics Class B Standard Products

Signetics Class B Vendor Standard products are offered for use when JAN products are not qualified on the QPL, SMD products are not available, or when program requirements allow the use of vendor standard products.

All Class B standard products are compliant to MIL-STD-883, general provisions Paragraph 1.2.1 for non-JAN devices. No claims by Signetics are otherwise made of equivalence to JAN products or to MIL-M-38510. Signetics standard products also conform with JEDEC Publication 101.

Electrical specifications are as included in the most current Signetics Military Data Manual.

- 100% final electrical tests include all data manual parameter limits, test conditions, and temperatures applicable to Subgroups 1, 2, 3, 7, 8, and 9 of MIL-STD-883, Method 5004 for digital products, or to Subgroups 1, 2, 3, 4, and 9 for Linear products.
- Group A sample electrical inspection tests include all applicable final electrical subgroups as well as all other Data Manual parameters with specified minimum or maximum limits.
- End-point electrical tests used for QCI inspection sampling (Groups C and D) are those Data Manual parameter limits, test conditions, and temperatures applicable to the Group A Subgroups specified in the most similar associated detail specification (slashsheet).

Data manual parameters which have no specified minimum or maximum limits (typical performance only) are not tested. Parameters which have limits specified at 25°C only, are tested only at that temperature. Detailed parameter assignment to Group A subgroups and other test details are contained in documented Signetics internal Product Electrical specifications, and are available upon request. Actual test program symbolics are available for customer review at the factory, but are considered proprietary and will not be copied or otherwise distributed outside of Signetics.

Waivers or deviations deemed necessary in contracts must be processed in accordance with MIL-STD-480.

Package types which do not have case outline letters assigned in MIL-M-38510, Appendix C, are assigned case outline letters per JEDEC Publication 101.

The Signetics standard Product Assurance Plan documentation is available for customer review at the factory.

This category of product conforms to quality level B-1 of MIL-HDBK-217 ($\pi_Q = 2.0$).

### Signetics Class C Standard Products

Signetics Class C product is offered for use in non-critical applications where burn-in is not required, but performance over the Military temperature range or hermetic construction is required by the customer. Class C product is identical to Class B products in all requirements, except that burn-in, PDA, and the 96 hour test requirements are not applicable.

# Product Description

Since MIL-M-38510 and MIL-STD-883 no longer define Class C requirements, these products are by definition non-compliant to MIL-STD-883, Paragraph 1.2.1.

This category of product conforms to quality level D of MIL-HDBK-217 ($\pi_Q$ = 10.0).

## General Information

- All Signetics products are considered sensitive to electrostatic discharge (ESD), regardless of ESD category. In-process factory ESD controls are maintained from die attach through shipping. Devices are packed in protective tubes or magazines, enclosed in a Faraday shield container, and labeled in accordance with MIL-STD-129.

  **WARNING: Devices may be degraded or destroyed if proper ESD handling techniques are not used when opening the shipping container. The Signetics warranty is void if product is not properly protected.**

- All Signetics production areas, critical support areas, subcontract test labs, and authorized distributor stocking locations are certified and periodically self-audited by Signetics Quality Assurance.

- Government source inspection (GSI) is provided on JAN qualified products by the Defense Contract Administration Services (DCAS). GSI services for all other non-JAN products must be delegated by the customer's Contracting Officer.

- Customer Source Inspection (CSI) which is contractually required on standard products is restricted to final documentation review only (Signetics does not identify work-in-process by customer). For custom or semi-custom products, CSI is permissible at any in-process operation, however the customer is cautioned that the most non-JAN products are fully processed in our Thailand facility.

- Source or Spec Control Drawings (SCD), Altered Item Drawings, and Selected Item Drawings (SID) are acceptable for review. The Signetics review guidelines reflect the standard requirements of MIL-STD-883, Paragraph 1.2.1.

- Signetics is agreeable to customer imposed qualification, First Article, or MIL-M-38510 QCI requirements on non-JAN products. Contact the factory for price and delivery information.

- Purchase order directed standard data pack requirements are acceptable for screening or QCI attribute data for all standard products. Contact the factory for price and delivery information.

- Signetics offers a one year limited warranty from the time of delivery to the customer on standard products for performance, workmanship, and conformance to the applicable product specifications. Products procured through Signetics authorized distributors are similarly warranteed for one year from the time of delivery to the customer. This warranty is not transferable through multiple distributor transactions, and is invalid for any product which is delivered by or transferred through a non-authorized distributor, broker or test laboratory.

- The Signetics warranty is invalid if the customer or his subcontractor subject the product to alteration (e.g., marking, lead cutting) or stresses beyond the capability of the product. Where environmental stress screening is contractually required, it is strongly recommended that Signetics be consulted as to the ability of the devices to survive the stresses, and that the test laboratory be certified by the customer's QA organization.

- All products are marked with a unique country of origin code identifying the assembly plant location. The code "USA" signifies assembly in our Orem, Utah facility, and the code "THAI" signifies assembly in our Bangkok, Thailand facility.

- The Signetics plant address information is as follows:

**Company Headquarters**
Signetics Company
811 E. Arques Avenue
P.O. Box 3409
Sunnyvale, Ca 94088–3409
Telephone: (408) 991–2000
Telex: 172–243

**JAN Manufacturing**
Signetics Company
1275 S. 800 East Street
Orem, Utah 84058
Telephone: (801) 225–6600

**Non-JAN Manufacturing**
Signetics Thailand Co. LTD.
303 Chaeng Wattana Road
Bangkhen
Bangkok, Thailand
Telephone: 66–2–521–0653
Telex: (788) 82939

# Ordering Information

## Military Products

For standard products, customers shall specify the complete part number as listed in the product description herein or in the Signetics published price book. Use of the lead finish designator "X" is highly recommended for procurement, as it simplifies multisource procurements from manufacturers who may process devices with different lead finishes. The actual lead finish designator is marked on the product and on the shipping documents. Use of the Signetics factory number (i.e., JB54LS161AF or RB54LS161AF) is not recommended due to possible errors in order entry transposition.

For non–standard products, customers shall specify the SCD number and drawing revision.

For all products, purchase order options include:

- Source Inspection; Government (GSI) and/or Customer (CSI). A letter of delegation (DCAS) and source point description must accompany the purchase order prior to order entry.
- Special packing or packaging.
- Data packs; For Class B and C product, two options may be specified: Screening and Group A attribute data (supplied as a single data set), and/or Quality Conformance Inspection (QCI) attribute data (does not include Group A). For JAN Class S products, data packs include screening attributes, QCI attributes, and all variables data (SEM photographs or X–ray film are not included).

# Coding Explanation

## Military Products

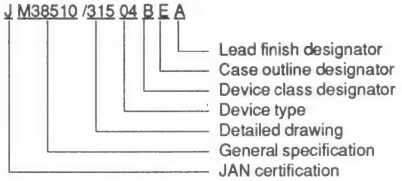
All products, whether JAN or standard product, are marked with the following information: per MIL-M-38510:

- ESD identifying triangle(s).
- Signetics manufacturer's identification logo:

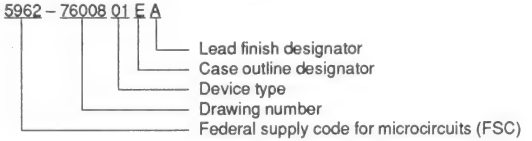
- Compliant product identifier, "C", per MIL-STD-883, 1.2.1. Not applicable to JAN or Class C products. This identifier is included on date codes after 8749.
- Inspection lot identification seal date code.
- Signetics manufacturer's designing symbol per NAVSHIPS 0967-190-4010. The Signetics manufacturer's designating symbol are the characters "DKB".
- Country of origin, "USA" or "THAI".
- Part number.
- The Pin 1 index point for most packages is found as a part of the package construction (i.e., the dual-in-line notch, the flat pack Pin 1 enlargement, or the leadless chip carrier elongated Pin 1 base terminal or chamfered package corner). The ESD identifying symbol is located in the Pin 1 quadrant, but not necessarily adjacent to Pin 1. For leadless chip carriers, the ESD identifier is located on the top surface at Pin 1.

The following examples illustrate the part marking system for 54LS161A standard product.

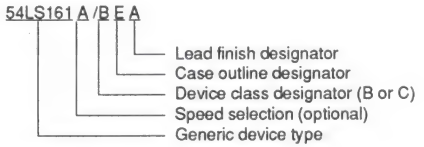
- For JAN products, the part number is per MIL-M-38510 and detailed device specification.



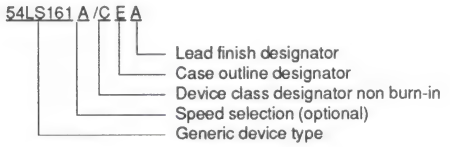

- For Standard Military Drawing products, the part number is per the drawing.




- For Signetics Vendor Standard Products, the part number is as listed in this product description or in published price lists.




- For Signetics Class C Standard products, the part number is listed in this product description or in the published price lists.



# Coding Explanation

**MARKING FORMAT EXAMPLES:**

•DIP — Example of Standard Military Drawing Marking

• FLAT — Example of JAN Military Drawing Marking

• LLCC — Example of Standard Product Military Drawing Marking

**Notes on Package Marking:**
This page is provided to help explain the general marking scheme for Signetics Military devices. For more specific information on marking details, contact the Military Marketing Group.

** Date code explanation: C918904A

△ ESD triangle. Depending on ESD level, there may be one, two or no ESD triangles. C Signifies compliance to Mil-Std-883. Not required for JAN product which is by definition, compliant. First two positions (91 in example). Fab date code indicating last digit of the year and Quarter. Last 5 positions is seal date code and suffix letter.

# Packaging Information

## Military Products

### SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

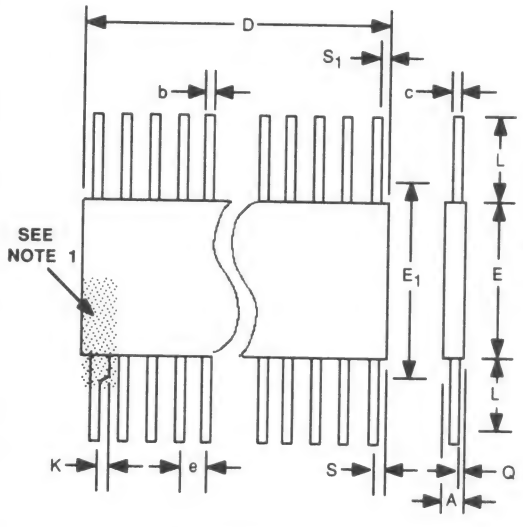
**Table 1.**

| Package Description | Type Designation | Case Outline | Theta-JC °C/Watt[4] |
|---|---|---|---|
| 8DIP3 | D-4 | P | 28 |
| 14DIP3 | D-1 | C | 28 |
| 16DIP3 | D-2 | E | 28 |
| 18DIP3 | D-6 | V | 28 |
| 20DIP3 | D-8 | R | 28 |
| 22DIP4 | D-7 | W | 28 |
| 24DIP3 | D-9 | L | 28 |
| 24DIP4 | D-11 | X[2] | 28 |
| 24DIP6 | D-3 | J | 28 |
| 28DIP6 | D-10 | X[2] | 28 |
| 40DIP6 | D-5 | Q | 28 |
| 48DIP6 | D-14[1] | X[2] | 28 |
| 50DIP9 | D-12[1] | X[2] | 28 |
| 64DIP9 | D-13[1] | X[2] | 28 |
| 14FLAT | F-2 | D | 22 |
| 16FLAT | F-5 | F | 22 |
| 18FLAT | F-10 | Y[2] | 22 |
| 20FLAT | F-9 | S | 22 |
| 24FLAT | F-6 | K | 22 |
| 28FLAT | F-11 | Y[2] | 22 |
| 52FLAT | Y-1[1] | Y[2] | 22 |
| 18LLCC | C-9 | U[2] | 20 |
| 20LLCC | C-2[3] | 2 | 20 |
| 28LLCC | C-4[3] | 3 | 20 |
| 32LLCC | C-12 | U[2] | 20 |
| 44LLCC | C-5 | U[2] | 20 |
| 68LLCC | C-7 | U[2] | 20 |
| 68PGA | P-AB | Z[2] | 20 |
| 84PGA | P-AB | Z[2] | 20 |

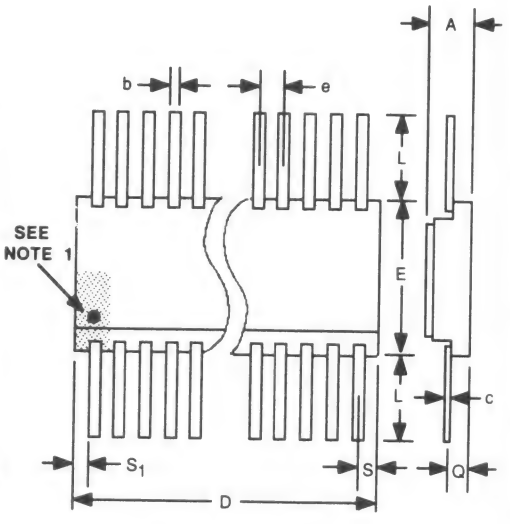
**NOTES:**
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

# Packaging Information

## CASE OUTLINES Y (FLAT PACKAGES)




Configuration 1




Configuration 2

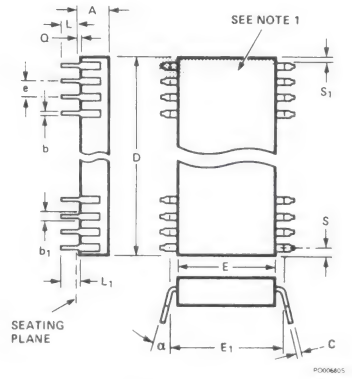
**NOTES:**

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ± 0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

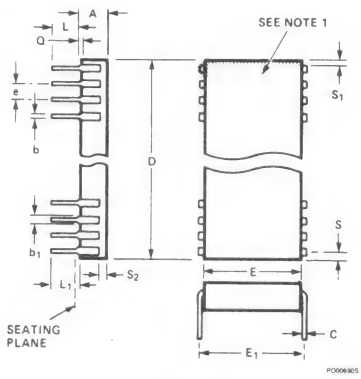
| OUTLINE | Y1 | | NOTES |
|---|---|---|---|
| CONFIGURATION | 2 | | |
| NO. LEADS | 52 | | |
| SIG. PKG. | QP | | |
| SYMBOL | INCHES | | |
| | Min | Max | |
| A | 0.045 | 0.100 | |
| b | 0.015 | 0.026 | 6 |
| c | 0.008 | 0.015 | 6 |
| D | - | 1.330 | 2 |
| E | 0.620 | 0.660 | |
| e | 0.050 BSC | | 3 |
| L | 0.250 | 0.370 | |
| Q | 0.054 | 0.0666 | 4 |
| S | - | 0.045 | 5 |
| S1 | 0.005 | - | 5 |

# Packaging Information

## CASE OUTLINES X (DUAL IN–LINE PACKAGES)




Configuration 1

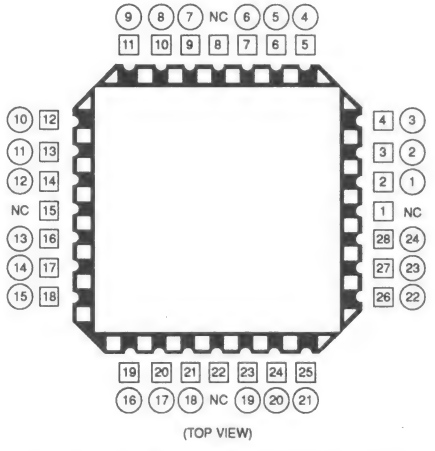



Configuration 2

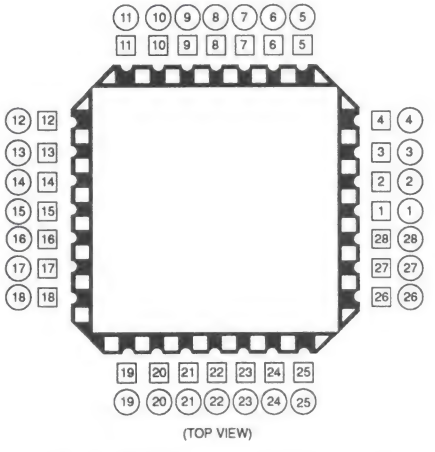
1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

# Packaging Information

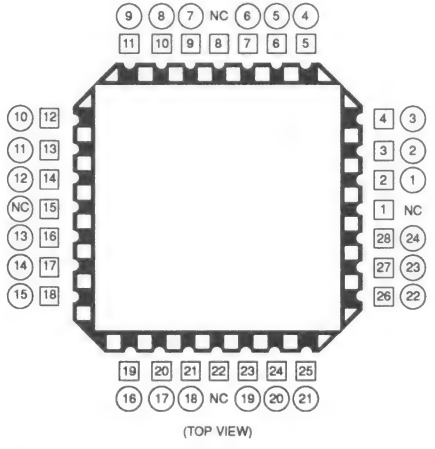
## LEADLESS CHIP CARRIER (LLCC) PINOUTS



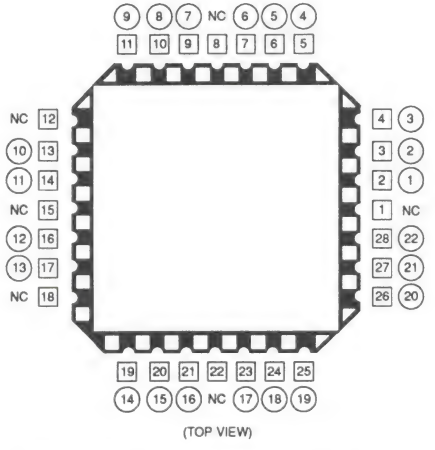

**24–Lead Logic Pinout for 28 Terminal Chip Carrier**




**28–Lead Pinout for 28 Terminal Chip Carrier for all Device Types**




**24–Lead Memory Pinout for 28 Terminal Chip Carrier**




**22–Lead Memory Pinout for 28 Terminal Chip Carrier**

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect

# Test Guidelines

## Military Products

### TEST GUIDELINES

This data book has been prepared by the Signetics Military Products Division with the intention of describing both the requirements or limits of the devices contained within and the specific conditions which will be employed to meet the requirements. To ensure the accuracy of both the test program and the data sheets, the Quality and Reliability Group for the Division has performed at 100% audit of all such material and continues to monitor the process through approval of all test programs and data sheet ECNs (Engineering Change Notices).

There are some test condition details which can be best described in an overview section such as this. They are:

**Logic Products**

1. Functional Test
   - A) Consists of applying specific Logic patterns to the device inputs while verifying the correct output states.
   - B) Uses Logic levels where $V_I = V_{OL}$ or $V_{OH}$.
   - C) Is generally performed with no output load.
2. $F_{MAX}$ Measurement
   - A) Is performed at the specified clock frequency and consists of ensuring that the device does function. There are no constraints on Pulse Rise Time, Fall Time or Setup and Hold conditions. This test can be best described as a "Toggle" test run at the maximum device specified frequency.
3. AC Parametric Measurements
   - A) Signetics has upgraded the AC specifications of the gold-doped (TTL), Low Power Schottky (LS) and Schottky (S) devices by adding in 50pF limit tables that apply over temperature. The data sheet indicates that these new limits are presently guaranteed, but Signetics Military Division is generating and implementing test capabilities and will be actually performing these new limit conditions within the next year. During the interim, Signetics will be performing testing to either the 15pF or 50pF output load and limits specified. Currently the ATE (Automatic Test equipment) being employed actually have test head/load board capacitances that exceed 50pF.
   - B) While performing any specific AC test (e.g., $t_{PLH}$), test conditions not intended to be measured at this point, but which could affect the result due to the testing environment will be set at a non-critical condition (e.g., setup and hold). In other words, critical (spec) test conditions will be generally restricted to only the parameter under test.
4. $I_{CC}$ Measurements
   - A) The input voltage conditions while performing this test is either greater than or equal to 4.0V (High State) or equal to Ground (Low State). Any $I_{CC}$ measurement which requires clocking will be so noted in the data sheet.

Signetics

# Section 2
# Linear Products
# Data Sheets

**Military Products**

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Signetics

# LM119
## Dual Voltage Comparator

*Product Specification*

**Military Communications and Industrial Products**

### DESCRIPTION

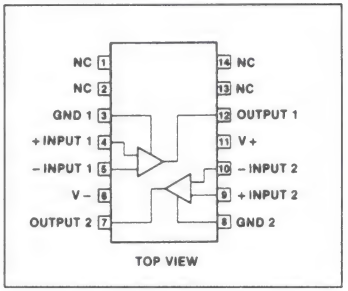
The LM119 is a precision high-speed dual comparator fabricated on a single monolithic chip. It is designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, it has higher gain and lower input currents than devices like the μA710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL, and TTL as well as capable of driving lamps and relays at currents up to 25mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 is fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high-speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the μA711.

### FEATURES

- **Two independent comparators**
- **Operates from a single 5V supply**
- **Typically 80ns response time at ±15V**
- **Minimum fanout of 3 (each side)**
- **Maximum input current of 1μA over temperature**
- **Inputs and outputs can be isolated from system ground**

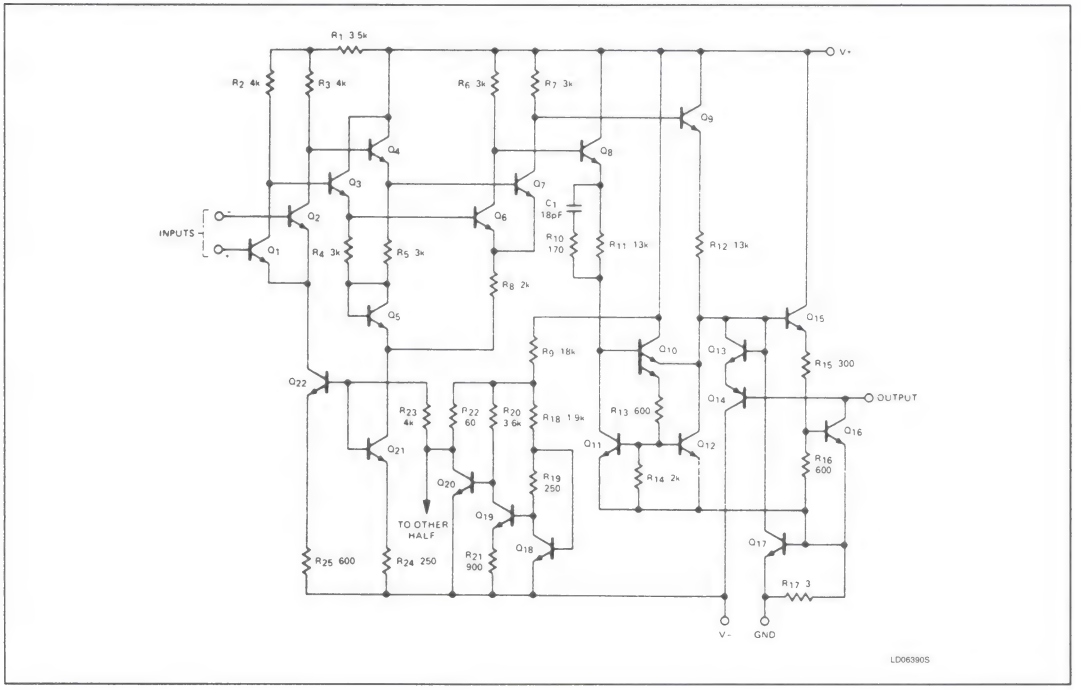
### PIN CONFIGURATION




### ORDERING INFORMATION

| PACKAGES | ORDER CODE |
|---|---|
| 14–Pin Ceramic DIP | LM119/BCA |

### EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_S$ | Total supply voltage | 36 | V |
| | Output to negative supply voltage | 36 | V |
| | Ground to negative supply voltage | 25 | V |
| | Ground to positive supply voltage | 18 | V |
| | Differential input voltage | ±5 | V |
| $V_{IN}$ | Input voltage[2] | ±15 | V |
| | Maximum power dissipation[3] | 500 | mA |
| | Output short–circuit duration | 10 | s |
| $T_A$ | Operating temperature range | –55 to +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_{SOLD}$ | Lead soldering temperature (10sec max) | 300 | °C |

## DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise specified.

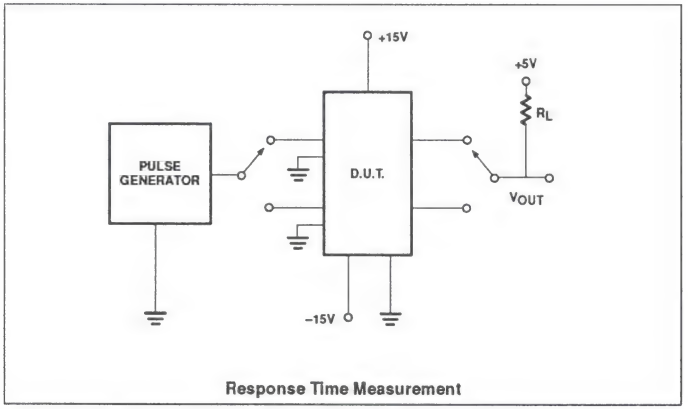
| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $V_{OS}$ | Input offset voltage[4, 5] | $R_S \leq 5k\Omega$ | | 0.7 | 4.0 | | 7.0 | mV |
| $I_{OS}$ | Input offset current[4, 5] | | | 30 | 75 | | 100 | nA |
| $I_B$ | Input bias current[5] | | | 150 | 500 | | 1000 | nA |
| $A_V$ | Voltage gain[6] | | 10 | 40 | | | | V/mV |
| $V_{OL}$ | Saturation voltage | $V_{IN}$[7] ≤ –5mV, $I_{OUT}$ = 25mA<br>V+ ≥ 4.5V, V– = 0<br>$V_{IN}$[7] ≤ –6mV, $I_{OUT}$ = 3.2mA<br><br>$T_A = 125°C$<br>$T_A = -55°C$ | | 0.75<br><br>0.23 | 1.5<br><br>0.4 | | <br><br>0.4<br>0.6 | V<br><br>V<br>V<br>V |
| $I_{OH}$ | Output leakage current | V– = 0V, $V_{IN} \geq 5mV$<br>$V_{OUT} = 35V$ | | 0.2 | 2 | | 10 | µA |
| $V_{IN}$ | Input voltage range | $V_S = \pm 15V$<br>V+ = 5V, V– = 0V | ±12<br>1 | ±13 | <br>3 | ±12<br>1 | <br>3 | V<br>V |
| $V_{ID}$ | Differential input voltage | | | | ±5 | | ±5 | V |
| I+ | Positive supply current | V+ = 5V, V– = 0V | | 4.3 | | | | mA |
| I+ | Positive supply current | $V_S = \pm 15V$ | | 8.0 | 11.5 | | | mA |
| I– | Negative supply current | $V_S = \pm 15V$ | | 3.0 | 4.5 | | | mA |

## AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_R$ | Response time[8] | $V_S = \pm 15V$, $T_A = 25°C$<br>$R_L = 500\Omega$ (see test figure) | | 80 | | ns |

**NOTES:**
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation at these or any other conditions above those indicated in the operational specifications is not implied.
2. For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
3. The absolute maximum junction temperature is 150°C. Device dissipation must be derated as 9.5mW/°C.
4. $V_{OS}$, $I_{OS}$ and $I_B$ specifications apply for a supply voltage range of $V_S = \pm 15V$ down to a single 5V supply.
5. The offset voltages and offset currents given are the maximum values required to drive the output to within 1V of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
6. This parameter is guaranteed, but not tested.
7. $V_{IN}$ value specified is the overdrive applied in addition to the specified $V_{OS}$ value.
8. The response time specified is for a 100mV step with 5mV overdrive.

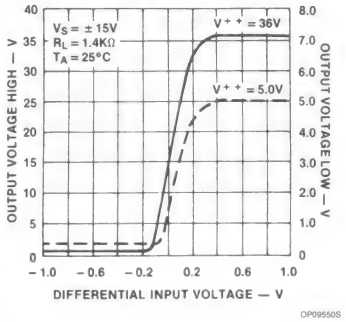
## TEST CIRCUIT



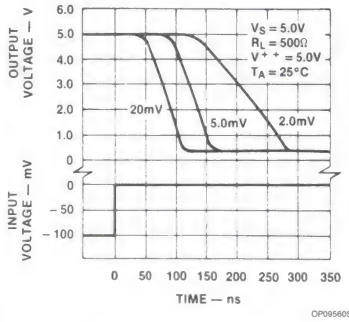

**Response Time Measurement**

## TYPICAL PERFORMANCE CHARACTERISTICS

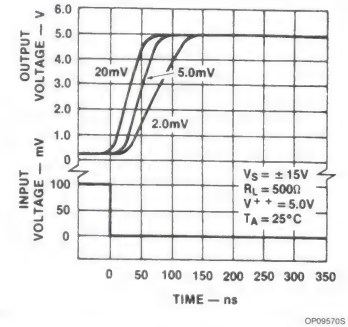
Transfer Function



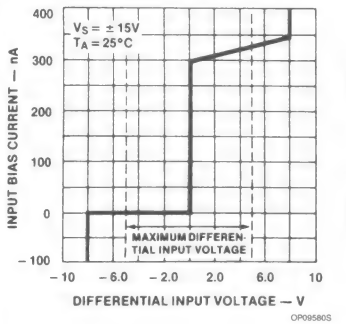

Response Time for Various Input Overdrives



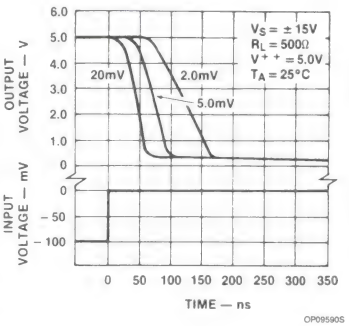

Response Time for Various Input Overdrives



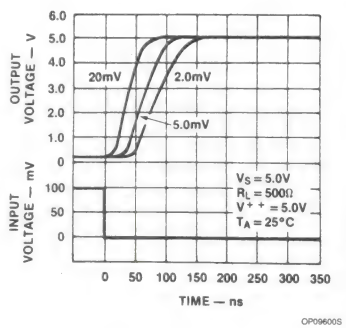

Input Characteristics



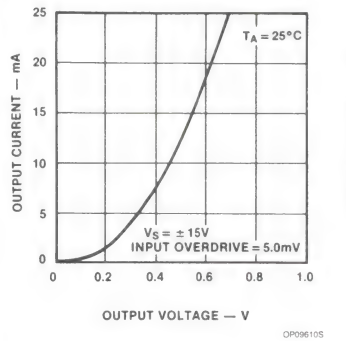

Response Time for Various Input Overdrives



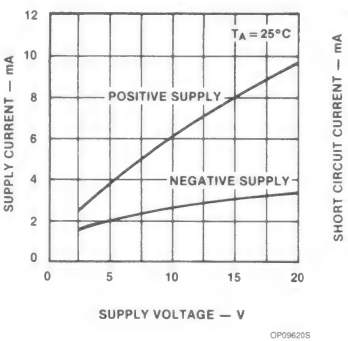

Response Time for Various Input Overdrives



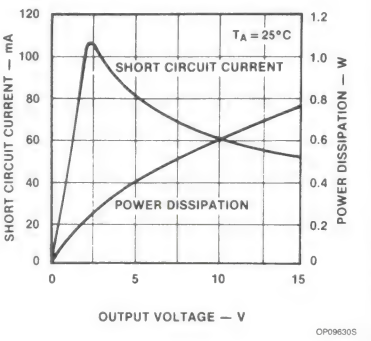

Output Saturation Voltage



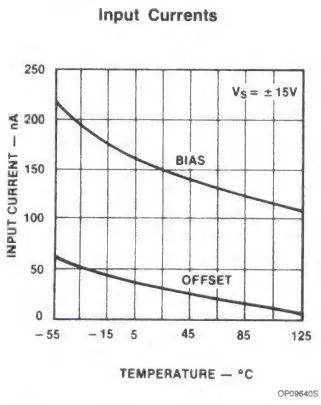

Supply Current

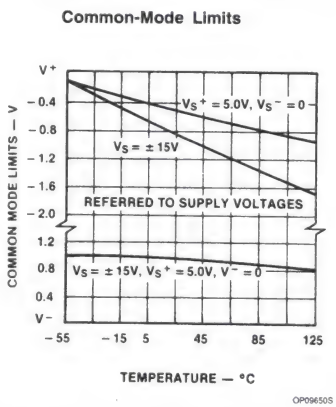


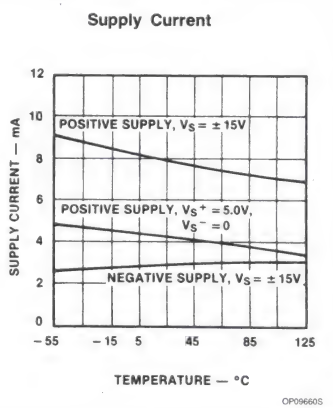

Output Limiting Characteristics



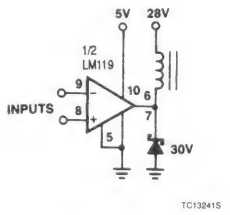
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



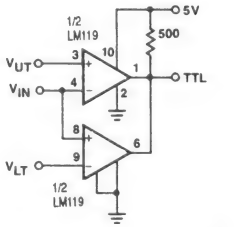




## TYPICAL APPLICATIONS

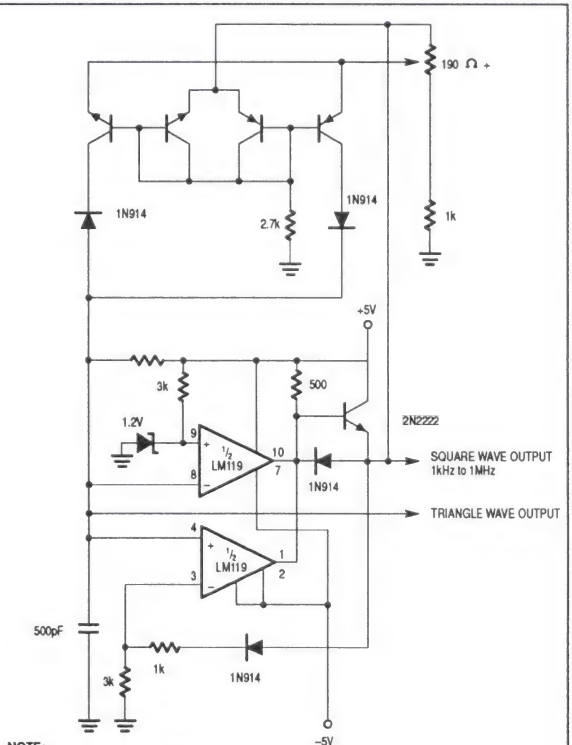



Relay Driver




Window Detector

NOTES:
$V_{OUT}$ = 5V for $V_{LT} < V_{IN} < V_{UT}$
$V_{OUT}$ = 0V for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$




NOTE:
Frequency adjust must be buffered for $R_L \leq 10\ \Omega$

Wide Range Variable Oscillator

Signetics

# LM 124

## Low Power Quad Op Amp

*Product Specification*

**Military Communications and Industrial Products**

### DESCRIPTION

The LM124 is an independent, high-gain, internally frequency-compensated operational amplifier designed specifically to operate from a single power supply over a wide range of voltages.

### UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage

The unity gain cross frequency is temperature compensated.

The input bias current is also temperature compensated.

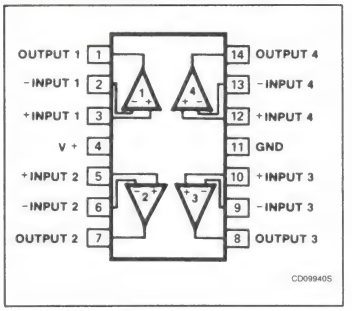
### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 14-Pin Ceramic DIP | LM124/BCA |

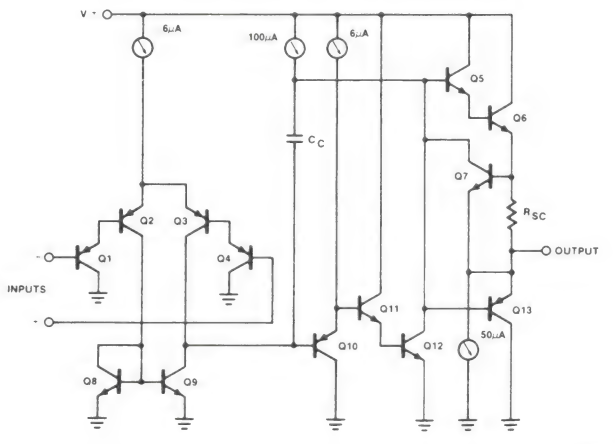
### FEATURES

- **Internally frequency compensated for unity gain**
- **Large DC voltage gain (100dB)**
- **Wide bandwidth (unity gain) — 1MHz (temperature compensated)**
- **Wide power supply range — Single supply ($3V_{DC}$ to $30V_{DC}$) or Dual supplies ($\pm1.5V_{DC}$ to $\pm15V_{DC}$)**
- **Very low supply current drain — essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)**
- **Low input biasing current ($45nA_{DC}$ temperature compensated)**
- **Low input offset voltage ($2mV_{DC}$) and offset current ($5nA_{DC}$)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage ($0V_{DC}$ to V+ — $1.5V_{DC}$ swing)**

### PIN CONFIGURATION




### EQUIVALENT SCHEMATIC (One circuit only)



## ABSOLUTE MAXIMUM RATINGS[6]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| V+ | Supply voltage | 32 or ±16 | $V_{DC}$ |
| $V_{DIFF}$ | Differential input voltage | 32 | $V_{DC}$ |
| $V_{IN}$ | Input voltage | –0.3 to +32 | $V_{DC}$ |
| $P_D$ | Power dissipation[1] | 900 | mW |
| $I_{SC}$ | Output short–circuit to GND<br>1 amplifier[2]<br>V+ < $15V_{DC}$ and $T_A$ = 25°C | Continuous | |
| $I_{IN}$ | Input current ($V_{IN}$ < –0.3V)[3] | 50 | mA |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS V+ = +5V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IO}$ | Input offset voltage[4] | $R_S$ = 0Ω | | 2 | 5 | | | 7 | mV |
| $\Delta V_{IO}/\Delta T$ | Input offset voltage drift | $R_S$ = 0Ω | | | | | 7 | | µV/°C |
| $I_{IB}$ | Input bias current[3] | $R_S$ = 10kΩ<br>$I_{IN}(+)$ or $I_{IN}(-)$ | | 45 | 150 | | | 300 | nA |
| $\Delta I_{IB}/\Delta T$ | Input bias drift | | | | | | 50 | | pA/°C |
| $I_{IO}$ | Offset current | $I_{IN}(+) - I_{IN}(-)$ | | 3 | 30 | | | 100 | nA |
| $\Delta I_{IO}/\Delta T$ | Offset current drift | | | | | | 10 | | pA/°C |
| $V_{ICR}$ | Common–mode voltage range | V+ = 30V | 0 | | V+ –1.5 | 0 | | V+ –2 | V |
| CMRR | Common–mode rejection ratio[5] | V+ = 30V | 70 | 85 | | 70 | | | dB |
| $V_O$ | Output voltage swing[7] | $R_L$ = 2kΩ, V+ = +30V | 26 | | | 26 | | | V |
| $V_{OH}$ | Output High voltage | $R_L \geq$ 10kΩ, V+ = 30V | 27 | 28 | | 27 | | | V |
| $V_{OL}$ | Output Low voltage | $R_L \geq$ 10kΩ | | 5 | 20 | | | 20 | mV |
| $I_{CC}$ | Supply voltage | $R_L$ = ∞, V+ = 30V<br>$R_L$ = ∞, V+ = 5.0V | | 1.5<br>0.7 | 3.0<br>1.2 | | | 3.0<br>1.2 | mA<br>mA |
| $A_V$ | Large signal voltage gain | V+ = +15V<br>(for large $V_O$ swing)<br>$R_L \geq$ 2kΩ | 50 | 100 | | 25 | | | V/mV |
| CS | Amplifier–to–amplifier coupling | f = 1kHz to 20kHz,<br>input referred | | 120 | | | | | dB |
| PSRR | Power supply rejection ratio | $R_S \leq$ 0Ω | 65 | 100 | | 65 | | | dB |
| $I_{OH}$ | Output current source | $V_{IN}$+ = +1V,<br>$V_{IN}$– = 0V, V+ = 15V | 20 | 40 | | 10 | | | mA |
| $I_{OL}$ | Output current sink | $V_{IN}$– = +1V, $V_{IN}$+ = 0V,<br>V+ = 15V, $V_O$ = 4.4V | 10 | 20 | | 5 | | | mA |
| | | $V_{IN}$+ = $0V_{DC}$,<br>$V_{IN}$– = $+1V_{DC}$,<br>$V_O$ = 200mV | 12 | 50 | | | | | µA |
| $I_{SC}$ | Short–circuit current[2] | V+ = 10V | –10 | –40 | –60 | | | | mA |
| $V_{IDR}$ | Differential input voltage[5] | | | | V+ | | | | V |

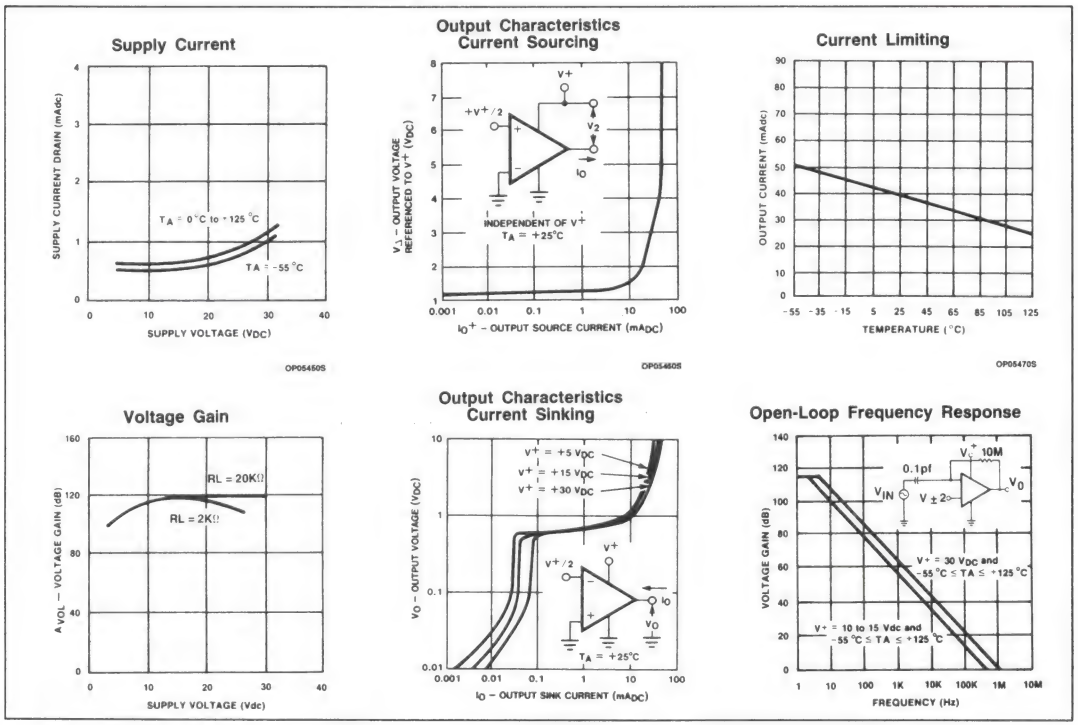
## AC ELECTRICAL CHARACTERISTICS V+ = +5V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| GBW | Unity gain bandwidth | | | 1 | | | | | MHz |
| S.R. | Slew rate | | | 0.3 | | | | | V/μs |
| Noise | Input noise voltage | f = 1kHz | | 40 | | | | | $nV/\sqrt{Hz}$ |

**NOTES:**

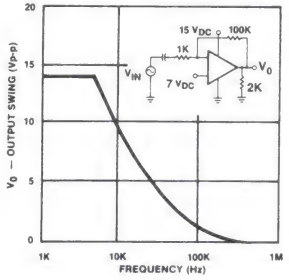
1. For operating at high temperatures, all devices must be derated based on a +150°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. the maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continuous short–circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the input lines.
4. $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from 5V to 30V and over full input common mode range ($0V_{DC}$+ to V+ –1.5V).
5. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common–mode voltage range is V+ –1.5, but either or both inputs can go to +32V without damage.
6. Operation beyond limits of this table may impair the useful life of the device.
7. For long term static operation above $V_{CC}$ = 18V , derate the output load resistance to 3.2kΩ minimum.

## TYPICAL PERFORMANCE CHARACTERISTICS

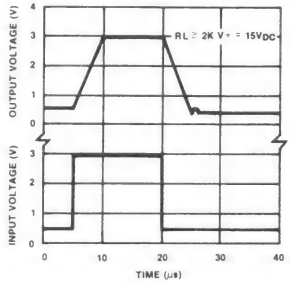


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

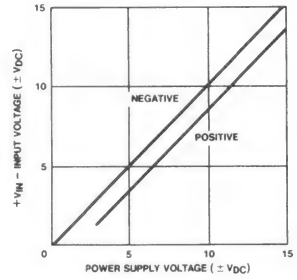
**Large-Signal Frequency Response**



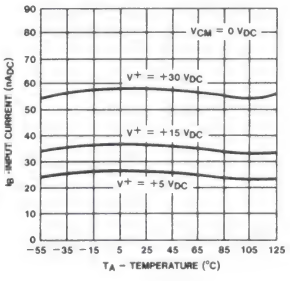

**Voltage-Follower Pulse Response**



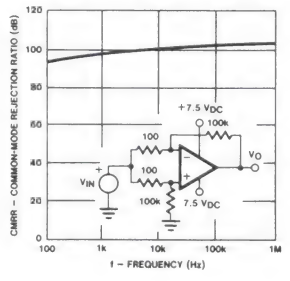

**Input Voltage Range**



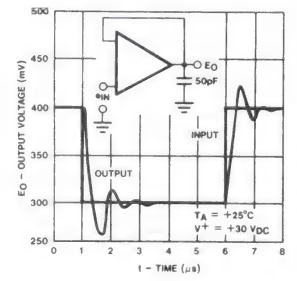

**Input Current**



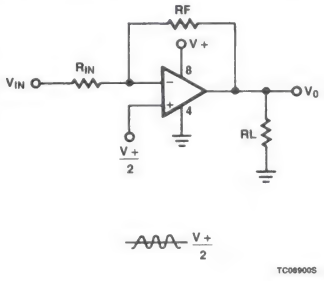

**Common-Mode Rejection Ratio**



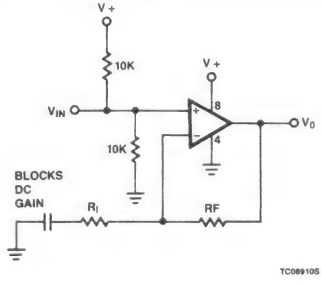

**Voltage-Follower Pulse Response (Small-Signal)**



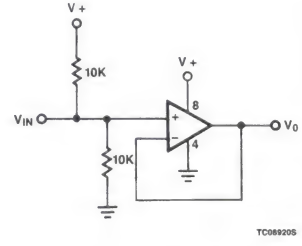

## TYPICAL APPLICATIONS




**Single Supply Inverting Amplifier**




**Non-Inverting Amplifier**




**Input Biasing Voltage-Follower**

Signetics

# LM139A/LM139
## Quad Voltage Comparator

*Product Specification*

**Military Communications and Industrial Products**

### DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for each comparator which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 14–Pin Ceramic DIP | LM139/BCA |
| 14–Pin Ceramic DIP | LM139A/BCA |

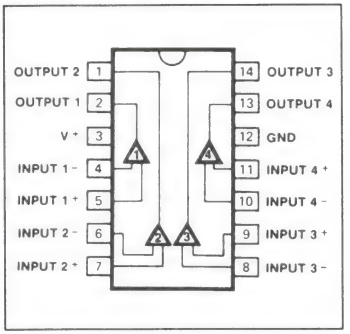
### FEATURES

- **Wide single supply voltage range 2.0$V_{DC}$ to 36$V_{DC}$ or dual supplies ±1.0$V_{DC}$ to ±18$V_{DC}$**
- **Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0$V_{DC}$)**
- **Low input biasing current 25nA**
- **Low input offset current and offset voltage**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

### APPLICATIONS

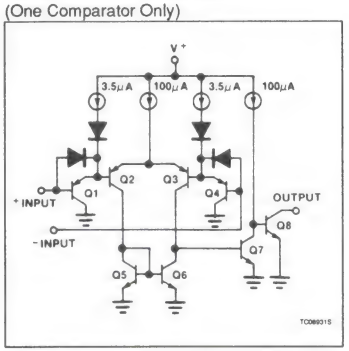
- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

### PIN CONFIGURATION




### EQUIVALENT CIRCUIT

(One Comparator Only)




### ABSOLUTE MAXIMUM RATINGS[9]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 36 or ±18 | V |
| $V_{DIFF}$ | Differential input voltage | 36 | V |
| $V_{IN}$ | Input voltage | –0.3 to +36 | V |
| $P_D$ | Power dissipation[1] | 900 | mW |
| $I_{SC}$ | Output short circuit to ground[2] | Continuous | |
| $I_{IN}$ | Input current ($V_{IN}$ < –0.3$V_{DC}$)[3] | 50 | mA |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

**NOTE:**

1. Operation beyond the limits of this table may impair the useful life of the device.

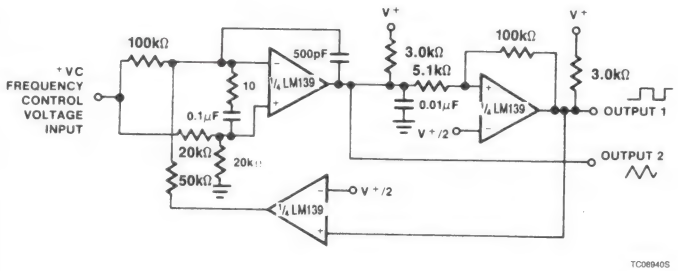
## DC ELECTRICAL CHARACTERISTICS V+ = +5V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IO}$ | Input offset voltage[5] | LM139A (only) | | 1.0 | 2.0 | | | 4.0 | mV |
| $V_{IO}$ | Input offset voltage[5] | LM139 (only) | | 2.0 | 5.0 | | | 9 | mV |
| $V_{ICR}$ | Common mode voltage range[6] | | 0 | | V+ –1.5 | 0 | | V+ –2.0 | V |
| $V_{IDR}$ | Differential input voltage[4] | Keep all $V_{IN} \geq 0V$ (or V– if need) | | | V+ | | | V+ | V |
| $I_{IB}$ | Input bias current[7] | $I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range | | 25 | 100 | | | 300 | nA |
| $I_{IO}$ | Input offset current | $I_{IN(+)} - I_{IN(-)}$ | | 3.0 | 25 | | | 100 | nA |
| $I_{OL}$ | Output sink current | $V_{IN(-)} \geq 1V$, $V_{IN}(+) = 0V$, $V_O \leq 1.5V$ | 6.0 | 16 | | 1.0 | | | mA |
| $I_{OH}$ | Output leakage current | $V_{IN(+)} \geq 1V$, $V_{IN}(-) = 0V$, $V_O = 5V$ | | 0.1 | | | | | nA |
| | | $V \leq 30V$ | | | 1.0 | | | 1.0 | µA |
| $I_{CC}$ | Supply current | V+ = 30V, $R_L = \infty$ | | 0.8 | 2.0 | | | 3.0 | mA |
| $A_V$ | Voltage gain | $R_L$ = 15kΩ, V+ = 15V | 50 | 200 | | | | | V/mV |
| $V_{OL}$ | Saturation voltage | $V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ | | 250 | 400 | | | 700 | mV |
| $t_{LSR}$ | Large signal response time | $V_{IN}$ = TTL logic swing, $V_{REF}$ = 1.4V, $V_{RL}$ = 5V, $R_L$ = 5.1kΩ | | 300 | | | | | ns |
| $t_R$ | Response time[8] | $V_{RL}$ = 5V, $R_L$ = 5.1kΩ | | 1.3 | | | | | µs |
| PSRR | Power supply rejection ratio | V+ = 5V to 30V LM139 | 65 | | | 65 | | | dB |
| PSRR | Power supply rejection ratio | V+ = 5V to 30V LM139A | 70 | | | 70 | | | dB |
| CMRR | Common mode rejection ratio | $R_L \geq 15k\Omega$, V+ = 30V $V_{CM}$ = 0V to 28.5V LM139 25°C | 65 | | | | | | dB |
| | | $V_{CM}$ = 0V to 28V LM139 temp | | | | 65 | | | dB |
| CMRR | Common mode rejection ratio | $R_L \geq 15k\Omega$, V+ = 30V $V_{CM}$ = 0V to 28.5V LM139A 25°C | 70 | | | | | | dB |
| | | LM139A temp $V_{CM}$ = 28.0V | | | | 70 | | | dB |

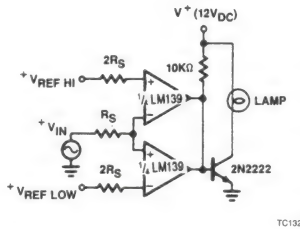
**NOTES:**

1. The LM139/139A must be derated on a 150°C max. junction temperature. The low power dissipation and the "On–Off" characteristics of the outputs keep the chip dissipation very small ($P_D \leq$ 100mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The max. output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re–establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.
4. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common–mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (or $0.3V_{DC}$ below the magnitude of the negative power supply, if used).
5. At output switch point, $V_O \cong 1.4V_{DC}$, $R_S$ = 100Ω with V+ from $5V_{DC}$ to $30V_{DC}$, and over the full input common–mode range ($0V_{DC}$ to V+ $-1.5V_{DC}$).
6. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. the upper end of the common–mode voltage range is V+ –1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
7. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
8. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained. See Typical Performance Characteristics section.
9. Operation beyond the limits of this table may impair the useful life of the device.

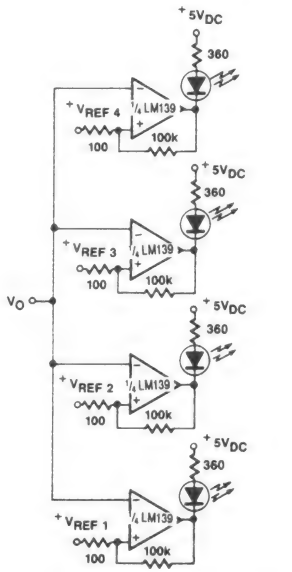
## TYPICAL APPLICATIONS



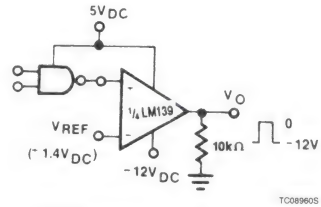

Two-Decade High-Frequency VCO



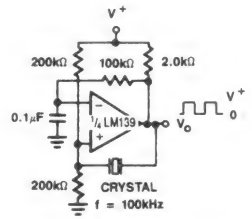

Limit Comparator




Visible Voltage Indicator




TTL-to-MOS Logic Converter

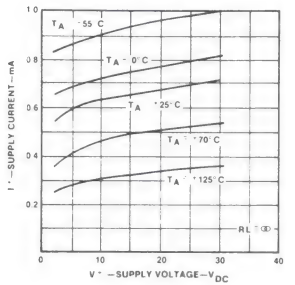



Crystal-Controlled Oscillator

**NOTE:**
Inputs of unused comparators should be grounded.

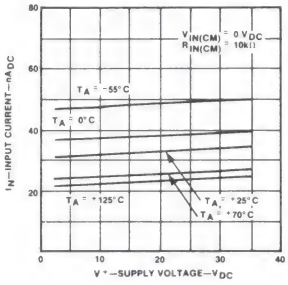
## TYPICAL PERFORMANCE CHARACTERISTICS

### Supply Current



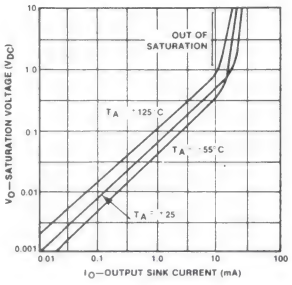

OP05570S

### Input Current



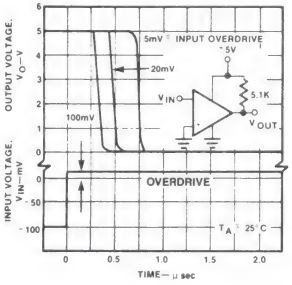

OP05580S

### Output Saturation Voltage



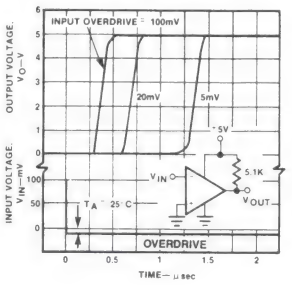

OP05590S

### Response Time for Various Input Overdrives — Negative Transition




OP05600S

### Response Time for Various Input Overdrives — Positive Transition




OP05610S

# 26LS31

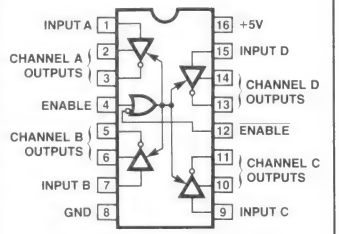
## Quad High Speed Differential Line Driver

***Product Specification***

### ORDERING INFORMATION

| PACKAGE | ORDER CODE |
|---|---|
| 16–Pin CERDIP | 26LS31/BEA |

### PIN CONFIGURATION




### ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{STG}$ | Storage temperature range | –65 | +150 | °C |
| $V_{CC}$ | Supply voltage | | 7.0 | V |
| $V_I$ | Input voltage | | 7.0 | V |
| $V_O$ | Output voltage | | 5.5 | V |

### RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $T_A$ | Operating temperature range | –55 | +125 | °C |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | Input High threshold voltage | 2.0 | | V |
| $V_{IK}$ | Input Low threshold voltage | | 0.8 | V |

### DC ELECTRICAL CHARACTERISTICS (Over recommended operating temperature and supply voltage range unless otherwise specified.)

| SYMBOL | PARAMETER | CONDITIONS | | LIMITS | | UNITS |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{OH}$ | Output High voltage | $V_{CC}$ = Min | $I_{OH}$ = –20mA | 2.5 | | V |
| $V_{OL}$ | Output Low voltage | $V_{CC}$ = Min | $I_{OL}$ = 20mA | | 0.5 | V |
| $V_{IH}$ | Input High voltage | $V_{CC}$ = Min | | 2.0 | | V |
| $V_{IL}$ | Input Low voltage | $V_{CC}$ = Max | | | 0.8 | V |
| $I_{IL}$ | Input Low current | $V_{CC}$ = Max | $V_{IN}$ = 0.4V | | –0.36 | mA |
| $I_{IH}$ | Input High current | $V_{CC}$ = Max | $V_{IN}$ = 2.7V | | 20 | µA |
| $I_I$ | Input reverse current | $V_{CC}$ = Max | $V_{IN}$ = 7.0V | | 0.1 | mA |
| $I_O$ | Off–state (high impedance) output current | $V_{CC}$ = Max | $V_O$ = 2.5V | | 20 | µA |
| | | | $V_O$ = 0.5V | | –20 | µA |
| $V_I$ | Input clamp voltage | $V_{CC}$ = Min | $I_N$ = –18mA | | –1.5 | V |
| $I_{SC}$ | Output short circuit current | $V_{CC}$ = Max | $V_{CC}$ = Max | –30 | –150 | mA |
| $I_{CC}$ | Power supply current | $V_{CC}$ = Max | All outputs disabled | | 80 | mA |

# Quad High Speed Differential Line Driver — 26LS31

## AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$

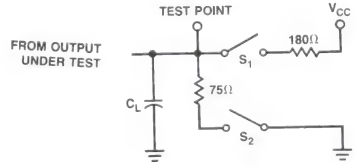
| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{PLH}$ | Propagation delay input to output | $V_{CC}$ = 5.0V | | 20 | ns |
| $t_{PHL}$ | | Load = 1/ | | 20 | ns |
| SKEW | Output to output | $V_{CC}$ = 5.0V, Load = 1/ | | 6.0 | ns |
| $t_{LZ}$ | Propagation delay enable to output | $V_{CC}$ = 5.0V | | 35 | ns |
| $t_{HZ}$ | | $C_L$ = 10pF | | 30 | ns |
| $t_{ZL}$ | Propagation delay enable to output | $V_{CC}$ = 5.0V | | 45 | ns |
| $t_{ZH}$ | | Load = 1/ | | 40 | ns |

## AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{PLH}$ | Propagation delay input to output | $V_{CC}$ = 5.0V | | 30 | ns |
| $t_{PHL}$ | | Load = 1/ | | 30 | ns |
| SKEW | Output to output | $V_{CC}$ = 5.0V, Load = 1/ | | 9.0 | ns |
| $t_{LZ}$ | Propagation delay enable to output | $V_{CC}$ = 5.0V | | 53 | ns |
| $t_{HZ}$ | | $C_L$ = 10pF | | 45 | ns |
| $t_{ZL}$ | Propagation delay enable to output | $V_{CC}$ = 5.0V | | 68 | ns |
| $t_{ZH}$ | | Load = 1/ | | 60 | ns |

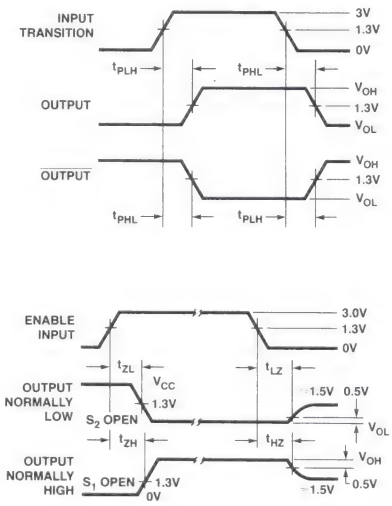
**NOTE:**
1/ $C_L$ = 30pF, $V_{IN}$ = 1.3V to $V_{OUT}$ 1.3V, $V_{PULSE}$ = 0V to +3.0V.

## EQUIVALENT AC TEST CIRCUIT




**NOTES:**
1. $C_L$ includes probe and JIG capacitance.
2. $S_1$ and $S_2$ are closed except where otherwise indicated in AC waveforms.

## AC WAVEFORMS




**NOTE:**
Pulse Generator for all Pulses: Rate ≤ 1.0MHz,
$Z_O$ = 50Ω, $t_r$ ≤ 15ns, $t_f$ ≤ 15ns.

Signetics

# 521

## High-Speed Dual Differential Comparator/Sense Amp

*Product Specification*

**Military Linear Products**

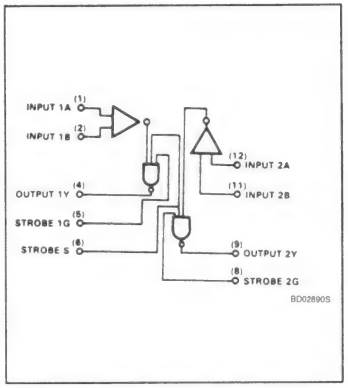
### FEATURES

- 12ns max. guaranteed propagation delay
- 20μA max. input bias current
- TTL compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages

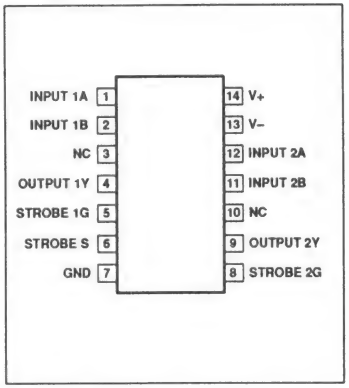
### APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

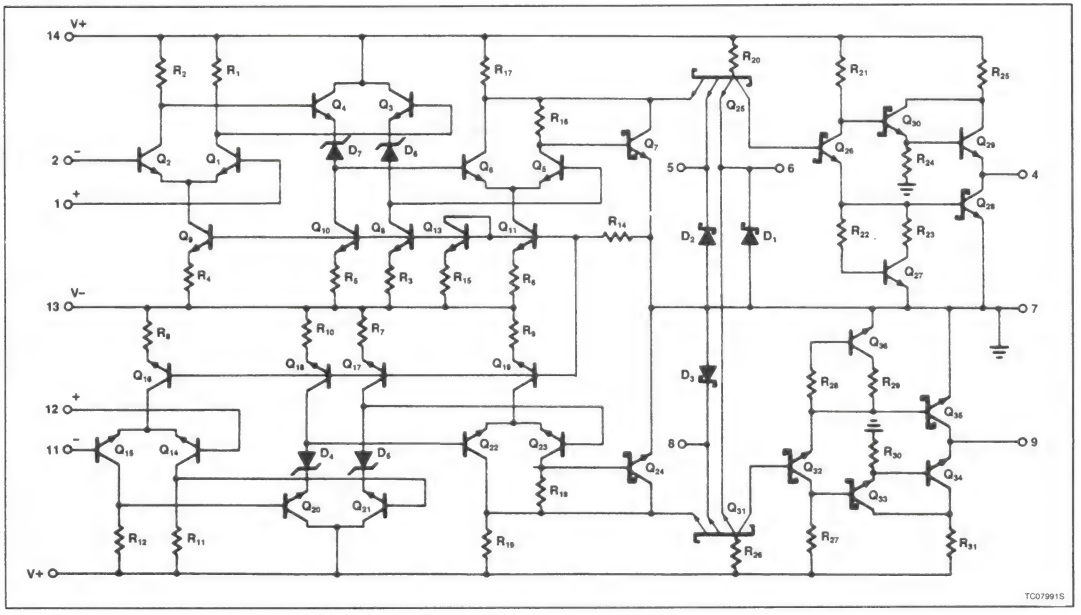
### BLOCK DIAGRAM




### PIN CONFIGURATION




### EQUIVALENT SCHEMATIC



# High-Speed Dual Differential Comparator/Sense Amp 521

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 14-Pin Ceramic DIP | 521/BCA |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| | Supply voltage | | |
| $V_+$ | Positive | +7 | V |
| $V_-$ | Negative | –7 | V |
| $V_{IDR}$ | Differential input voltage | ±6 | V |
| $V_I$ | Input voltage | | |
| | Common mode | ±5 | V |
| | Strobe/gate | +5.25 | V |
| $P_D$ | Power dissipation | 600 | mW |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $V_+ = +5V$, $V_- = -5V$, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **Input Characteristics** | | | | | | | | | |
| $V_{IO}$ | Input offset voltage | $V_+ = +4.5V$, $V_- = -4.5V$ | | 6 | 7.5 | | | 15 | mV |
| $I_{IB}$ | Input bias current | $V_+ = +5.5V$, $V_- = -5.5V$ | | 7.5 | 20 | | | 40 | µA |
| $I_{IO}$ | Input offset current | $V_+ = +5.5V$, $V_- = -5.5V$ | | 1.0 | 5 | | | 12 | µA |
| $V_{ICR}$ | Common mode voltage range | $V_+ = +4.5V$, $V_- = -4.5V$ | ±3 | | | ±3 | | | V |
| **Gate Characteristics** | | | | | | | | | |
| $V_{IL}$ | "0" input voltage | $V_+ = +4.5V$, $V_- = -4.5V$ | | | 0.8 | | | 0.7 | V |
| $V_{IH}$ | "1" input voltage | $V_+ = +4.5V$, $V_- = -4.5V$ | 2.0 | | | 2.0 | | | V |
| $I_{IH}$ | "1" input current | $V_+ = +5.5V$, $V_- = -5.5V$<br>$V_{IH} = 2.7V$<br>1G or 2G strobe<br>Common strobe S | | | <br><br>50<br>100 | | | <br><br>50<br>100 | <br><br>µA<br>µA |
| $I_{IL}$ | "0" Input current | $V_+ = +5.5V$, $V_- = -5.5V$<br>$V_{IL} = 0.5V$<br>1G or 2G strobe<br>Common strobe S | | | <br><br>−2.0<br>−4.0 | | | <br><br>−2.0<br>−4.0 | <br><br>mA<br>mA |
| $V_{OH}$<br>$V_{OL}$<br>$V_{OL}$ | Output voltage<br>"1" State<br>"0" State<br>"0" State | $V_{I(S)} = 2.0V$<br>$V_+ = +4.5V$, $V_- = -4.5V$, $I_{OH} = -1mA$<br>$V_+ = +4.5V$, $V_- = -4.5V$, $I_{OL} = 10mA$<br>$V_+ = +4.5V$, $V_- = -4.5V$, $I_{OL} - 20mA$ | <br>2.5 | <br>3.3 | <br><br>0.5<br>0.5 | <br>2.5 | | <br><br>0.5 | <br>V<br>V<br>V |
| $I_{SC}$ | Short–circuit output current | $V_+ = +5.5V$, $V_- = -5.5V$ | −35 | | −115 | −35 | | −115 | mA |
| **Power Supply Requirements** | | | | | | | | | |
| $V_+$<br>$V_-$ | Supply voltage<br>Positive<br>Negative | | <br>4.5<br>−4.5 | <br>5.0<br>−5.0 | <br>5.5<br>−5.5 | <br>4.5<br>−4.5 | | <br>5.5<br>−5.5 | <br>V<br>V |
| $I_{CC+}$<br>$I_{CC-}$ | Supply current<br>Positive<br>Negative | $V_+ = +5.5V$, $V_- = -5.5V$<br>$V_{STROBE} = 0V$ | | <br>27<br>−15 | <br>35<br>−28 | | | <br>50<br>−28 | <br>mA<br>mA |

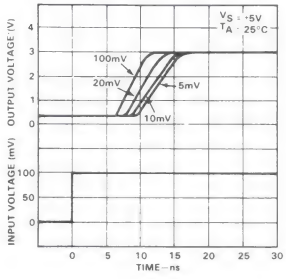
## AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $R_L = 280\Omega$, $C_L = 15pF$, $V_+ = +5V$, $V_- = -5V$

| SYMBOL | PARAMETER | FROM INPUT | TO OUTPUT | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **Large Signal Switching Speed Propagation Delay** | | | | | | | |
| $t_{PLH(D)}$<br>$t_{PHL(D)}$ | Low–to–high[2]<br>High–to–low[2] | Amp<br>Amp | Output<br>Output | | 8<br>6 | 12<br>9 | ns<br>ns |
| $t_{PLH(S)}$<br>$t_{PHL(S)}$ | Low–to–high[3]<br>High–to–low[3] | Strobe<br>Strobe | Output<br>Output | | 4.5<br>3.0 | 10<br>6 | ns<br>ns |

**NOTES:**
1. Operation beyond limits in this table may impair the useful life of the device.
2. Response time measured from 0V point of ± 100mV$_{P-P}$ 10MHz square wave to the 1.5 point of the output.
3. Response time measured from 1.5V point of input to 1.5V point of the output.

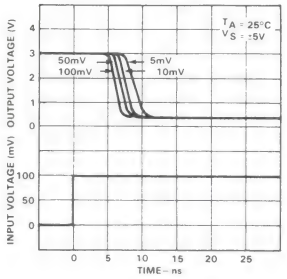
## TYPICAL PERFORMANCE CHARACTERISTICS

**Response Time for Various Input Overdrives**



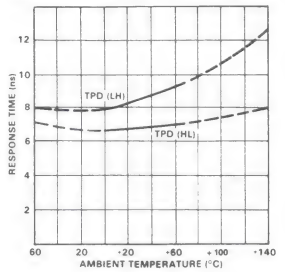

OP03890S

**Response Time for Various Input Overdrives**



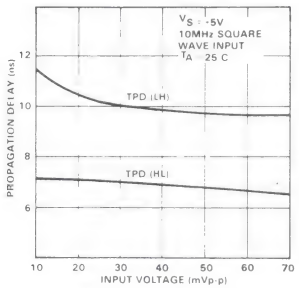

OP03900S

**Response Time vs Temperature**



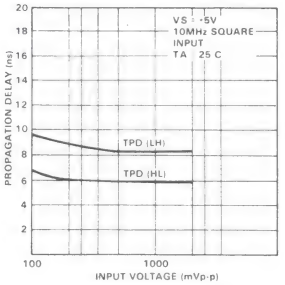

OP03910S

**Propagation Delay for Various Input Voltage**



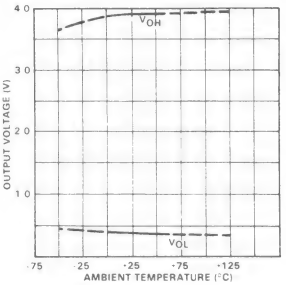

OP03920S

**Propagation Delay for Various Input Voltages**



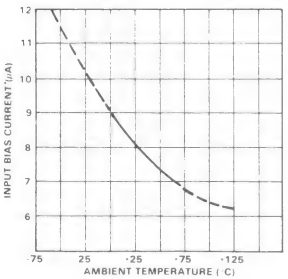

OP03930S

**Output Voltage vs Ambient Temperature**



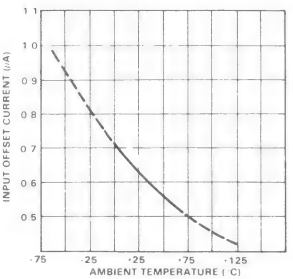

OP03940S

**Input Bias Current vs Ambient Temperature**




OP03950S

**Input Offset Current vs Ambient Temperature**




OP03960S

Signetics

# 522

## High-Speed Dual Differential Comparator/Sense Amp

*Product Specification*

**Military Linear Products**

### DESCRIPTION

The Dual Differential Comparator/Sense Amp is designed to convert line signals to TTL levels with a minimum addition propagation delay. Features include separate strobe output controls as well as a common output control.

### ORDERING INFORMATION

| PACKAGES | ORDER CODE |
|---|---|
| Ceramic DIP | 522/BCA |

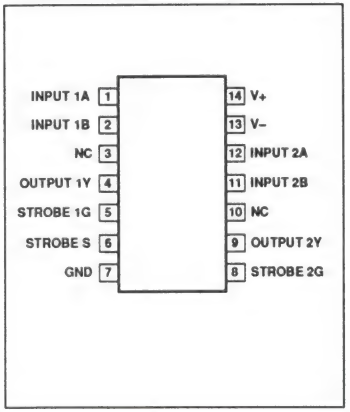
### FEATURES

- 12 ns max guaranteed propagation delay
- 20μA max. Input bias current
- TTL compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply
- Open collector outputs

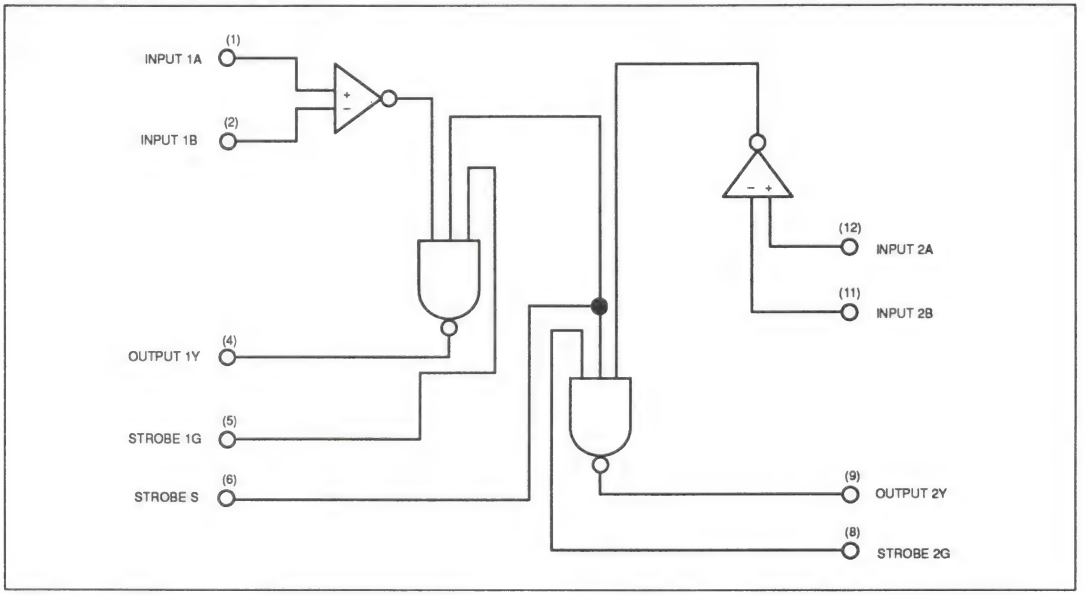
### APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

### PIN CONFIGURATION




### EQUIVALENT SCHEMATIC



# Comparator/Sense Amp 522

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| V+<br>V– | Supply voltage Positive<br>Supply voltage Negative | +7<br>–7 | V<br>V |
| $V_{IDR}$ | Differential input voltage | ±6 | V |
| $V_I$ | Input voltage<br>Common mode<br>Strobe/gate | <br>±5<br>+5.25 | <br>V<br>V |
| $P_D$ | Power dissipation | 600 | mW |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS V+ = +5V, V– = –5V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IO}$ | Input offset voltage | V+ = +4.5V, V– = –4.5V | | 6 | 7.5 | | | 15 | mV |
| $I_{IB}$ | Input bias current | V+ = +5.5V, V– = –5.5V | | 7.5 | 20 | | | 40 | µA |
| $I_{IO}$ | Input offset current | V+ = +5.5V, V– = –5.5V | | 1.0 | 5 | | | 12 | µA |
| $V_{ICR}$ | Common mode voltage range | V+ = +4.5V, V– = –4.5V | ±3 | | | ±3 | | | V |
| **Gate Characteristics** | | | | | | | | | |
| $V_{IL}$ | "0" input voltage | V+ = +4.5V, V– = –4.5V | | | 0.8 | | | 0.7 | V |
| $V_{IH}$ | "1" input voltage | V+ = +4.5V, V– = –4.5V | 2.0 | | | 2.0 | | | V |
| $I_{IH}$ | "1" input current | V+ = +5.5V,V– = –5.5V, $V_{IH}$ = 2.7V<br>1G or 2G strobe<br>Common strobe S | | | <br>50<br>100 | | | <br>50<br>100 | <br>µA<br>µA |
| $I_{IL}$ | "0" input current | V+ = +5.5V, V– = –5.5V, $V_{IL}$ = 0.5V<br>1G or 2G strobe<br>Common strobe S | | | <br>–2.0<br>–4.0 | | | <br>–2.0<br>–4.0 | <br>mA<br>mA |
| $V_{OL}$<br>$V_{OL}$ | Output voltage<br>"0" State<br>"0" State | $V_{I(S)}$ = 2.0V<br>V+ = +4.5V, V– = –4.5V, $I_{OL}$ = 10mA<br>V+ = +4.5V, V– = –4.5V, $I_{OL}$ = 20mA | | | <br><br>0.5 | | | <br><br>0.5 | <br>V<br>V |
| $I_{OH}$ | Output leakage current | V+ = +4.5V, V– = –4.5V, $V_{OUT}$ = 5.5V | | | 250 | | | 250 | µA |
| **Power Supply Requirements** | | | | | | | | | |
| V+<br>V– | Supply voltage Positive<br>Supply voltage Negative | | 4.5<br>–4.5 | 5.0<br>–5.0 | 5.5<br>–5.5 | 4.5<br>–4.5 | | 5.5<br>–5.5 | V<br>V |
| $I_{CC+}$<br>$I_{CC-}$ | Supply voltage Positive<br>Supply voltage Negative | V+ = +5.5V, V– = –5.5V<br>$I_{STROBE}$ = 0V | | 27<br>–15 | 35<br>–28 | | | 50<br>–28 | mA<br>mA |

## AC ELECTRICAL CHARACTERISTICS $T_A$ = 25°C, $R_L$ = 280Ω, $C_L$ = 15pF, V+ = +5V, V– = –5V.

| SYMBOL | PARAMETER | FROM INPUT | FROM OUTPUT | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **Large Signal Switching Speed Propagation Delay** | | | | | | | |
| $t_{PLH(D)}$<br>$t_{PHL(D)}$ | Low–to–High[2]<br>High–to–Low[2] | Amp<br>Amp | Output<br>Output | | 10<br>8 | 15<br>12 | ns<br>ns |
| $t_{PLH(S)}$<br>$t_{PHL(S)}$ | Low–to–High[3]<br>High–to–Low[3] | Strobe<br>Strobe | Output<br>Output | | 6<br>5 | 13<br>9 | ns<br>ns |

**NOTES:**
1. Operation beyond limits in this table may impair the useful life of the device.
2. Response time measured from 0V point of ±100mVp–p 10MHz square wave to the 1.5V point of the output.
3. Response time measured from 1.5V prompt of input to 1.5V point of the output.

Signetics

# 527
## Voltage Comparator

*Product Specification*

**Military Linear Products**

### DESCRIPTION

The 527 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high-speed $T^2L$ gates with a precision linear amplifier on a single monolithic chip. The 527 is similar in design to the Signetics 529 voltage comparator except that it incorporates an "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

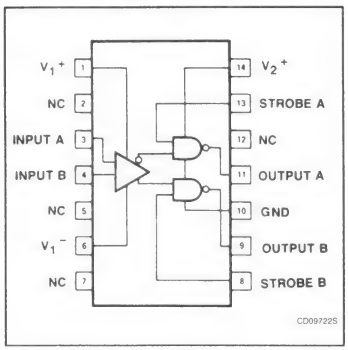
### FEATURES

- 15ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common mode and differential voltage range
- Typical gain of 5000

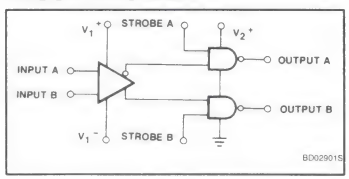
### APPLICATIONS

- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

### PIN CONFIGURATION



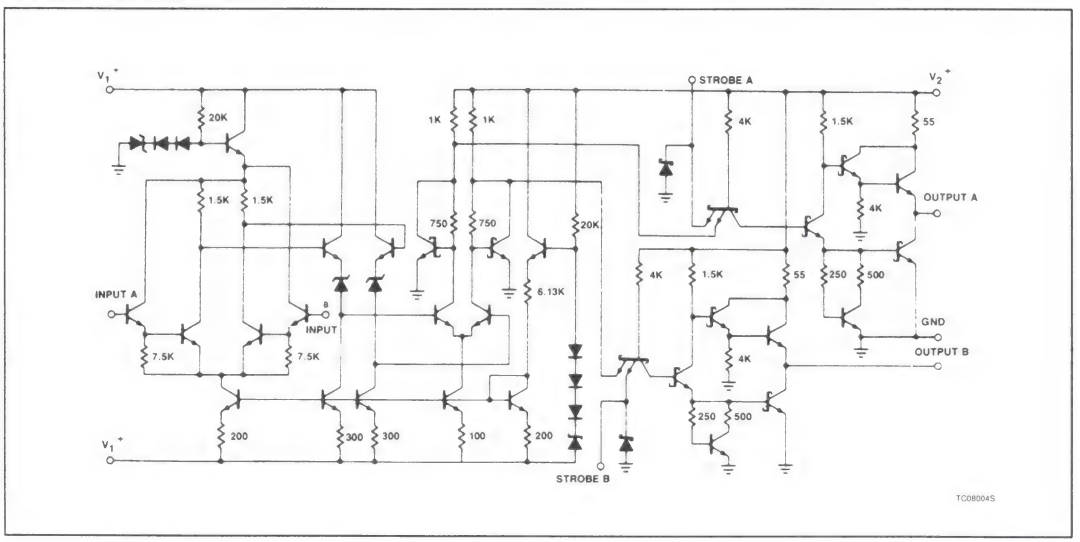

### BLOCK DIAGRAM




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 14-Pin Ceramic DIP | 527/BCA |

### EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_1+$ | Positive supply voltage | +15 | V |
| $V_1-$ | Negative supply voltage | –15 | V |
| $V_2+$ | Gate supply voltage | +7 | V |
| $V_O$ | Output voltage | +7 | V |
| $V_{ID}$ | Differential input voltage | ±5 | V |
| $V_{ICR}$ | Input common mode voltage | ±6 | V |
| $P_D$ | Power dissipation | 600 | mW |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $V_1+ = 10V$, $V_1- = -10V$, $V_2+ = +5.0V$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **Input Characteristics** | | | | | | | | | |
| $V_{IO}$ | Input offset voltage | | | | 4 | | | 6 | mV |
| $I_{IB}$ | Input bias current | | | | 2 | | | 4 | µA |
| $I_{IO}$ | Input offset current | $V_I = 0V$ | | | 0.5 | | | 1 | µA |
| $V_{ICR}$ | Common mode voltage range | | ±5 | | | ±5 | | | V |
| **Gate Characteristics** | | | | | | | | | |
| $V_{OH}$ | Output voltage "1" State | $V_2+ = 4.5V$, $I_{OH} = -1mA$ | 2.5 | 3.3 | | 2.5 | | | V |
| $V_{OL}$ | Output voltage "0" State | $V_2+ = 4.5V$, $I_{OL} = 10mA$ | | | 0.5 | | | 0.5 | V |
| $V_{IK}$ | Input clamp voltage | $I_{IK} = -18mA$, $V_2 = 4.5V$ | | | –1.5 | | | –1.5 | V |
| | Strobe inputs | | | | | | | | |
| $I_{IL}$ | Input current "0" | $V_2+ = 5.5V$, $V_{STROBE} = 0.5V$ | | | –2 | | | –2 | mA |
| $I_{IH}$ | Input current "1" | $V_2+ = 5.5V$, $V_{STROBE} = 2.7V$ | | | 50 | | | 200 | µA |
| $V_{IL}$ | Input voltage "0" | $V_2+ = 4.5V$ | | | 0.8 | | | 0.8 | V |
| $V_{IH}$ | Input voltage "1" | $V_2+ = 4.5V$ | 2.0 | | | 2.0 | | | V |
| | Short–circuit | | | | | | | | |
| $I_{SC}$ | Output current | $V_2+ = 5.5V$, $V_O = 0V$ | –18 | | –70 | –18 | | –70 | mA |
| **Power Supply Requirements** | | | | | | | | | |
| | Supply voltage | | | | | | | | |
| $V_1+$ | Comparator | | 5 | | 10 | 5 | | 10 | V |
| $V_1-$ | Comparator | | –6 | | –10 | –6 | | –10 | V |
| $V_2+$ | Gate | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| | Supply current | | | | | | | | |
| $I_1+$ | Comparator | $V_1+ = 10V$ | | | 5 | | | 5 | mA |
| $I_1-$ | Comparator | $V_1- = -10V$ | | | 10 | | | 10 | mA |
| $I_2+$ | Gate | $V_2+ = +5.5V$ | | | 20 | | | 20 | mA |

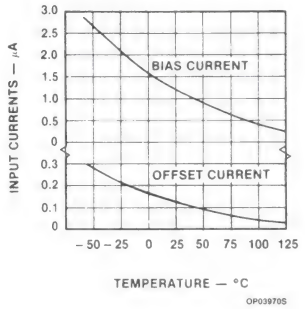
## AC ELECTRICAL CHARACTERISTICS $V_{1+}$ = 10V, $V_{1-}$ = −10V, $V_{2+}$ = 5.0V, unless otherwise specified.

| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = −55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| | Transient response propagation delay time | | | $V_1$ = ±100mV step | | | | | | | |
| $t_{PLH}$ | Low–to–high | Output | Input | $R_L$ = 390Ω | | 16 | 26 | | | | ns |
| $t_{PHL}$ | High–to–low | | | $C_L$ = 15pF | | 14 | 24 | | | | ns |
| Δt | Delay between output A and B | Output | Output | | | 2 | 5 | | | | ns |
| | Strobe delay time | | | | | | | | | | |
| $t_D$ | $t_{on}$ Turn–on time | Output | Strobe | | | 6 | | | | | ns |
| $t_D$ | $t_{off}$ Turn–off time | | | | | 6 | | | | | ns |

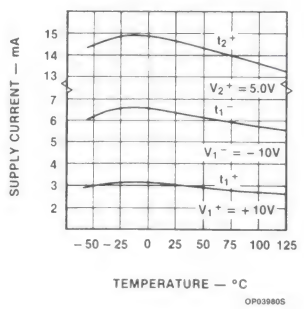
**NOTE:**
1. Operation beyond the limit in this table may impair useful life of the device.

## TYPICAL PERFORMANCE CHARACTERISTICS

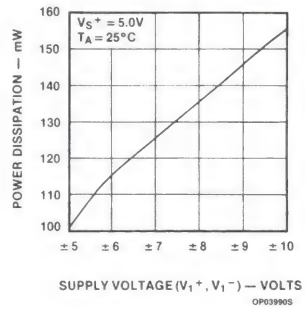
Input Currents vs Temperature



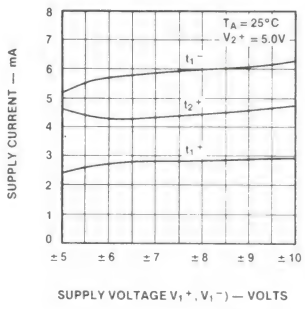

Supply Current vs Temperature



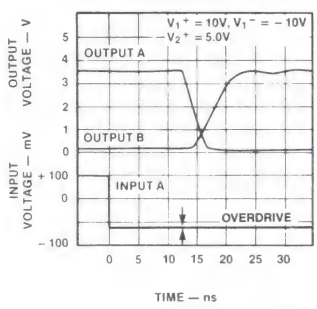

Power Dissipation vs Supply Voltage



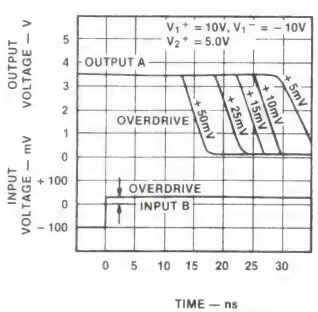

Supply Current vs Supply Voltage




Output Propagation Delays

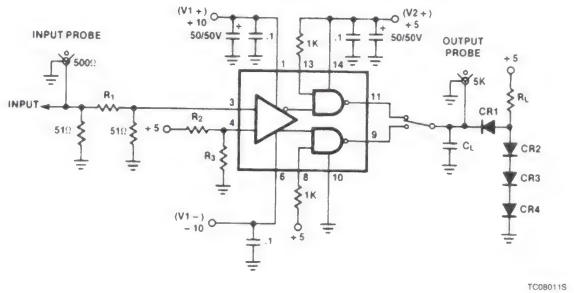



Response Time for Various Input Overdrives



# Voltage Comparator 527

## TYPICAL TIME TEST CIRCUIT




**NOTES:**
CR1 – CR4 = IN914
R1 selected for 15:1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
$P_W$ = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

Output
$R_L = 390\Omega$
$C_L$ = 25pF (including stray capacitance)

## 527 LOGIC FUNCTION

| $V_I$ ($A^+$, $B^-$) | STROBE A | STROBE B | OUTPUT A | OUTPUT B |
|---|---|---|---|---|
| $> V_O$ | X | h/l | H | l/h |
| $< -V_O$ | h/l | X | l/h | H |

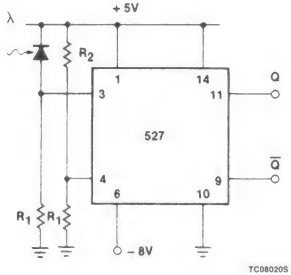
## APPLICATIONS

One of the main features of the device is that supply voltages (V+, V–) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V–) should always be at least 6V more than the ground terminal (Pin 6). Input Common–Mode range should be limited to values of 2V less than the supply voltages (V+ and V–) up to a maximum of ±6V as supply voltages are increased.

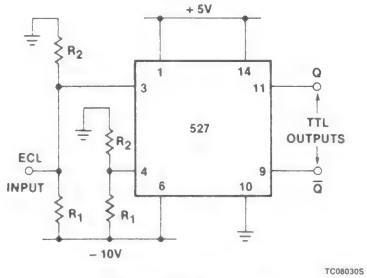
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

# Voltage Comparator 527

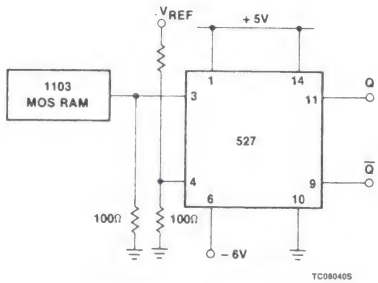
## TYPICAL APPLICATIONS



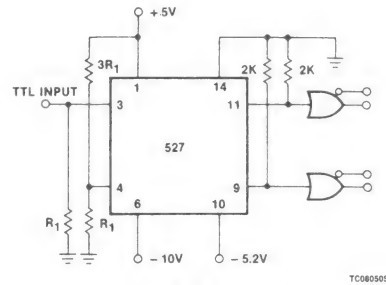

Photodiode Detector




ECL-to-TTL Interface




MOS Memory Sense AMP




TTL-to-ECL Interface

Signetics

# 529
## Voltage Comparator

*Product Specification*

**Military Linear Products**

### DESCRIPTION
The 529 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high-speed $T^2L$ gates with a precision linear amplifier on a single monolithic chip.

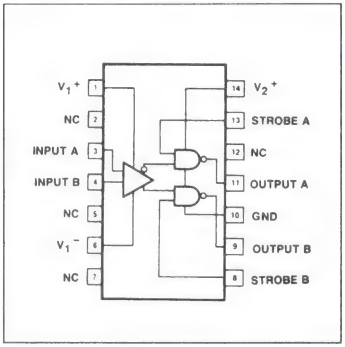
### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 14-Pin Ceramic DIP | 529/BCA |

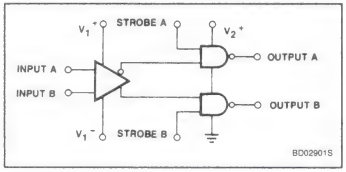
### FEATURES
- 10ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- Typical gain of 5000

### APPLICATIONS
- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

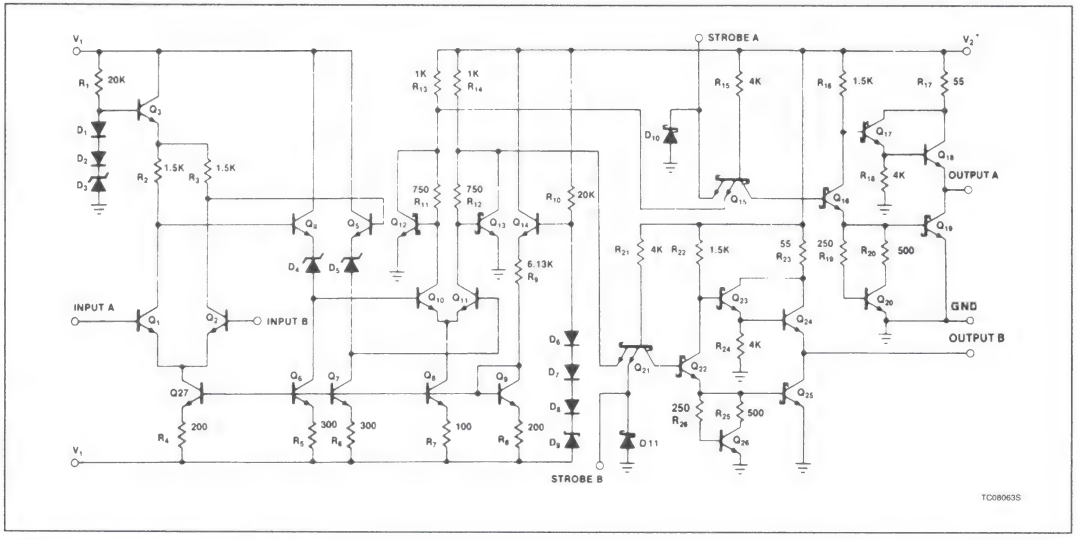
### PIN CONFIGURATION




### BLOCK DIAGRAM




### EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_1+$ | Positive supply voltage | +15 | V |
| $V_1-$ | Negative supply voltage | –15 | V |
| $V_2+$ | Gate supply voltage | +7 | V |
| $V_O$ | Output voltage | +7 | V |
| $V_{ID}$ | Differential input voltage | ±5 | V |
| $V_{ICR}$ | Input common mode voltage | ±6 | V |
| $P_D$ | Power dissipation | 600 | mW |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $V_1+ = +10V$, $V_1- = -10V$, $V_2+ = +5.0V$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **Input Characteristics** | | | | | | | | | |
| $V_{IO}$ | Input offset voltage | | | | 4 | | | 6 | mV |
| $V_{IB}$ | Input bias current | $V_1 = 0V$ | | 5 | 12 | | | 36 | µA |
| $I_{IO}$ | Input offset current | $V_1 = 0V$ | | 2 | 3 | | | 9 | µA |
| $V_{ICR}$ | Common mode voltage range | | ±5 | | | ±5 | | | V |
| **Gate Characteristics** | | | | | | | | | |
| $V_{OH}$ | Output voltage "1" State | $V_2+ = 4.5V$, $I_{OH} = -1mA$ | 2.5 | 3.3 | | 2.5 | | | V |
| $V_{OL}$ | Output voltage "0" State | $V_2+ = 4.5V$, $I_{OL} = 10mA$ | | | 0.5 | | | 0.5 | V |
| $V_{IK}$ | Input clamp voltage | $I_{IK} = -18mA$, $V_2+ = 4.5V$ | | | –1.5 | | | –1.5 | V |
| $I_{IL}$ | Strobe inputs "0" current[2] | $V_2+ = 5.5V$, $V_{STROBE} = 0.5V$ | | | –2 | | | –2 | mA |
| $I_{IH}$ | Strobe inputs "1" current | $V_2+ = 5.5V$, $V_{STROBE} = 2.7V$ | | | 50 | | | 200 | µA |
| $V_{IL}$ | Strobe inputs "0" voltage | $V_2+ = 4.5V$ | | | 0.8 | | | 0.8 | V |
| $V_{IH}$ | Strobe inputs "1" voltage | $V_2+ = 4.5V$ | 2.0 | | | 2.0 | | | V |
| $I_{SC}$ | Short–circuit output current | $V_2+ = 5.5V$, $V_O = 0V$ | –18 | | –70 | –18 | | –70 | mA |
| **Power Supply Requirements** | | | | | | | | | |
| $V_1+$ | Supply voltage comparator | | 5 | | 10 | 5 | | 10 | V |
| $V_1-$ | Supply voltage comparator | | –6 | | –10 | –6 | | –10 | V |
| $v_2+$ | Supply voltage gate | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_1+$ | Supply current comparator | $V_1+ = 10V$ | | | 5 | | | 5 | mA |
| $I_1-$ | Supply current comparator | $V_1- = -10V$ | | | 10 | | | 10 | mA |
| $I_2+$ | Supply current gate | $V_2+ = +5.5V$ | | | 20 | | | 20 | mA |

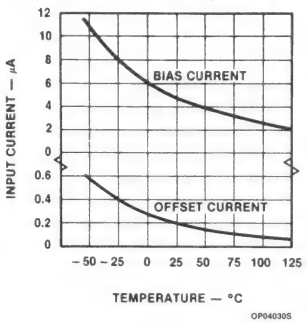
## AC ELECTRICAL CHARACTERISTICS $V_1+ = +10V$, $V_1- = -10V$, $V_2+ = +5.0V$, unless otherwise specified.

| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C$, $+125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| | Transient response propagation delay time | | | | | | | | | | |
| $t_{PLH}$ | Low–to–high | Output | Input | | | 12 | 22 | | | | ns |
| $t_{PHL}$ | High–to–low | | | $V_1 = \pm 100mV$ step | | 10 | 20 | | | | ns |
| $\Delta t$ | Delay between output A and B | Output | Output | $R_L = 390\Omega$ | | 2 | 5 | | | | ns |
| | Strobe delay time | Output | Strobe | $C_L = 15pF$ | | | | | | | |
| $t_D$ | $t_{on}$ Turn–on time | | | | | 6 | | | | | ns |
| $t_D$ | $t_{off}$ Turn–off time | | | | | 6 | | | | | ns |

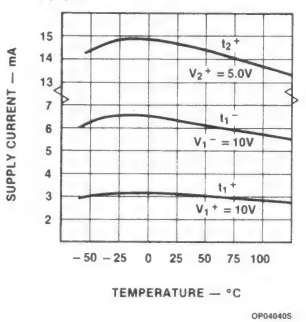
**NOTES:**
1. Operation beyond the limit in this table may impair useful life of the device.
2. See logic function table.

## TYPICAL PERFORMANCE CHARACTERISTICS

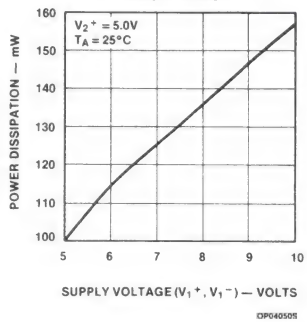
Input Currents vs Temperature



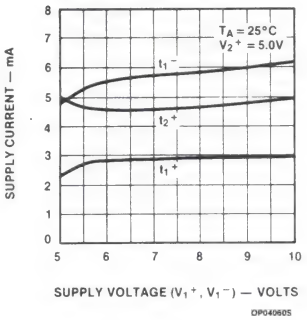

Supply Current vs Temperature



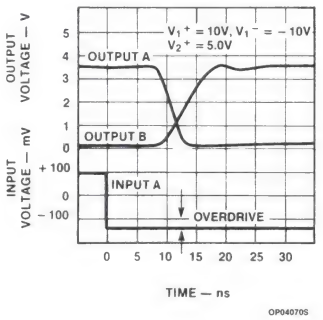

Power Dissipation vs Supply Voltage



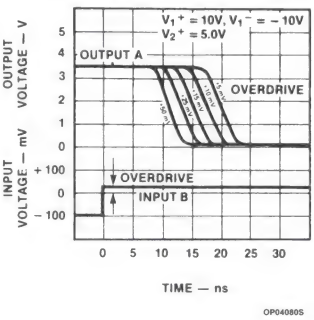

Supply Current vs Supply Voltage




Output Propagation Delays

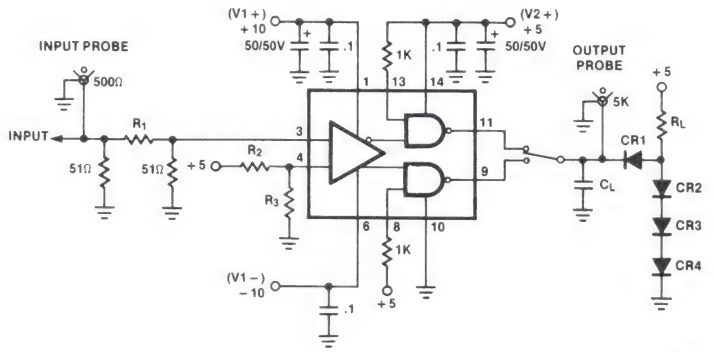



Response Time For Various Input Overdrives



# Voltage Comparator 529

## TYPICAL TIME TEST CIRCUIT




**NOTES:**
CR1 – CR4 = IN914
R1 selected for 15:1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
$P_W$ = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

$C_L$ = 25pF (including stray capacitance)

## 527 LOGIC FUNCTION

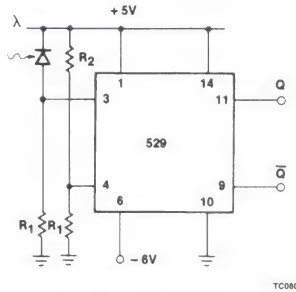
| $V_I$ ($A^+$, $B^-$) | STROBE A | STROBE B | OUTPUT A | OUTPUT B |
|---|---|---|---|---|
| $> V_O$ | X | h/l | H | l/h |
| $< -V_O$ | h/l | X | l/h | H |

## APPLICATIONS

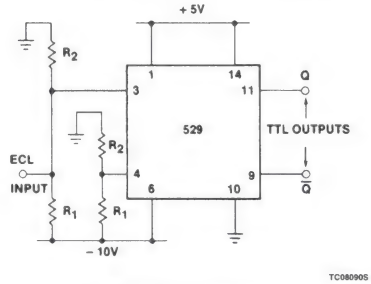
One of the main features of the device is that supply voltages (V+, V–) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V–) should always be at least 6V more than the ground terminal (Pin 6). Input Common–Mode range should be limited to values of 2V less than the supply voltages (V+ and V–) up to a maximum of ±6V as supply voltages are increased.

It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

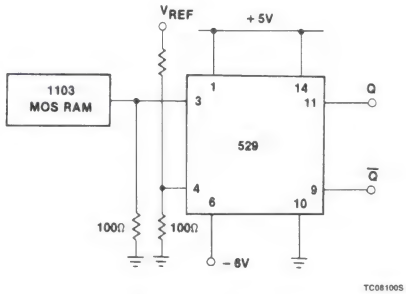
## TYPICAL APPLICATIONS



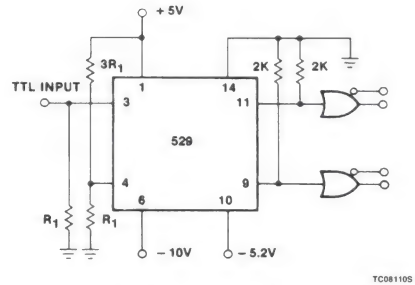

Photodiode Detector




ECL-to-TTL Interface




MOS Memory Sense AMP




TTL-to-ECL Interface

Signetics

# 555
## Timer

***Product Specification***

**Military Linear Products**

## DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

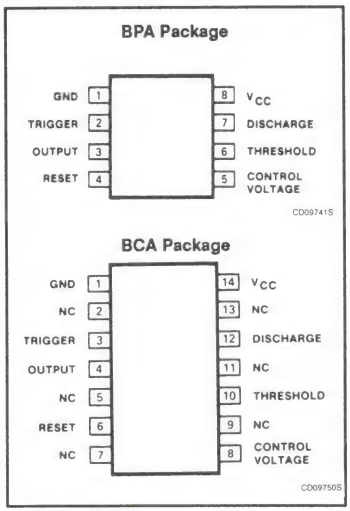
## FEATURES

- **Turn-off time less than 2μs**
- **Max. operating frequency greater than 500kHz**
- **Timing from microseconds to hours**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **TTL compatible**
- **Temperature stability of 0.005% per °C**

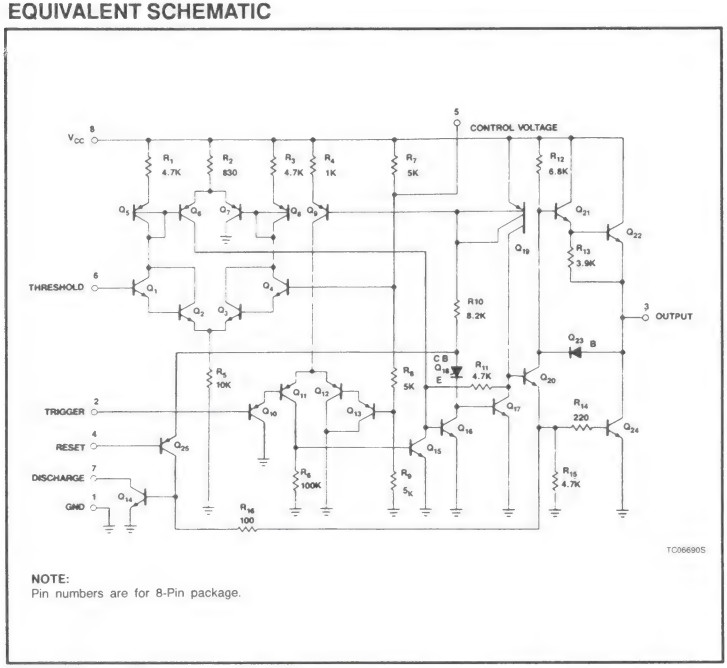
## APPLICATIONS

- **Precision timing**
- **Pulse generation**
- **Sequential timing**
- **Time delay generation**
- **Pulse width modulation**
- **Pulse position modulation**
- **Missing pulse detector**

## PIN CONFIGURATION

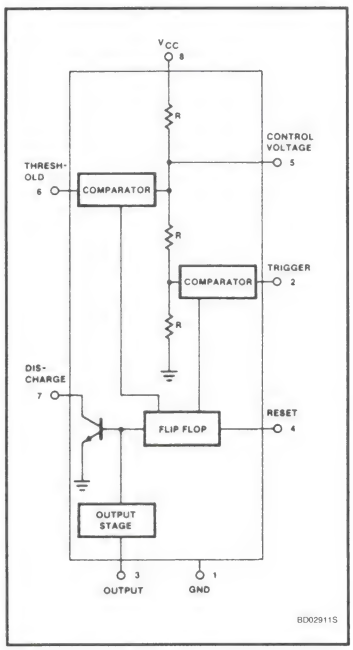



## EQUIVALENT SCHEMATIC




NOTE:
Pin numbers are for 8-Pin package.

## BLOCK DIAGRAM



## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 14–Pin Ceramic DIP | 555/BCA |
| 8–Pin Ceramic DIP | 555/BPA |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +18 | V |
| $P_D$ | Power dissipation | 600 | mW |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = +5V to $V_{CC}$ = +15V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | | 18 | 4.5 | | 18 | V |
| $I_{CC}$ | Supply current (low state)[2] | $V_{CC}$ = 5V, $R_L$ = ∞ | | 3 | 5 | | | 6 | mA |
| | | $V_{CC}$ = 15V, $R_L$ = ∞ | | 10 | 12 | | | 14 | mA |
| | Timing error (monostable) | $R_A$ = 2kΩ to 100kΩ | | | | | | | |
| $t_M$ | Initial accuracy[3] | C = 0.1µF | | 0.5 | 2.0 | | | 2.5 | % |
| $\Delta t_M/\Delta T$ | Drift with temperature[7,8] | | | | | | | 100 | ppm/°C |
| $\Delta t_M/\Delta V_S$ | Drift with supply voltage | | | 0.05 | 0.2 | | | 0.25 | %/V |
| | Timing error (astable) | $R_A$, $R_B$ = 1kΩ to 100kΩ | | | | | | | |
| $t_A$ | Initial accuracy[3] | C = 0.1µF | | 4 | 6 | | | 10.0 | % |
| $\Delta t_A/\Delta T$ | Drift with temperature[7] | $V_{CC}$ = 15V | | | | | | 500 | ppm/°C |
| $\Delta t_A/\Delta V_S$ | Drift with supply voltage[9] | | | 0.15 | 0.6 | | | 1.5 | %/V |
| $V_C$ | Control voltage level | $V_{CC}$ = +15V | 9.6 | 10.0 | 10.4 | 9.6 | | 10.4 | V |
| | | $V_{CC}$ = +5V | 2.9 | 3.33 | 3.8 | 2.9 | | 3.8 | V |
| $V_{TH}$ | Threshold voltage | $V_{CC}$ = +15V | 9.4 | 10.0 | 10.6 | 9.4 | | 10.6 | V |
| | | $V_{CC}$ = +5V | 2.7 | 3.33 | 4.0 | 2.4 | | 4.0 | V |
| $I_{TH}$ | Threshold current[4] | $V_{TH}$ = 10.6V | | 0.1 | 0.25 | | | 0.35 | µA |
| $V_{TRIG}$ | Trigger voltage | $V_{CC}$ = +15V | 4.8 | 5.0 | 5.2 | 4.5 | | 5.5 | V |
| | | $V_{CC}$ = +5V | 1.45 | 1.67 | 1.9 | 1.5 | | 2.2 | V |
| $I_{TRIG}$ | Trigger current | $V_{TRIG}$ = 0V | | 0.5 | 0.9 | | | 2.0 | µA |
| $V_{RESET}$ | Reset voltage[5] | | 0.4 | | 1.0 | 0.1 | | 1.3 | V |
| $I_{RESET}$ | Reset current | $V_{RESET}$ = 0.4V | | –0.1 | –0.4 | | | –0.6 | mA |
| $I_{RESET}$ | Reset current | $V_{RESET}$ = 0V | | –0.4 | –1.0 | | | –1.2 | mA |
| $V_{OL}$ | Output voltage (low)[10] | $V_{CC}$ = +15V | | | | | | | |
| | | $I_{SINK}$ = 10mA | | 0.1 | 0.15 | | | 0.25 | V |
| | | $I_{SINK}$ = 50mA | | 0.4 | 0.5 | | | 0.70 | V |
| | | $I_{SINK}$ = 100mA | | 2.0 | 2.2 | | | 2.6 | V |
| | | $V_{CC}$ = +5V | | | | | | | |
| | | $I_{SINK}$ = 8mA | | 0.1 | 0.25 | | | 0.43 | V |
| | | $I_{SINK}$ = 5mA | | 0.05 | 0.2 | | | 0.38 | V |
| $V_{OH}$ | Output voltage (high)[10] | $V_{CC}$ = +15V, $I_{SOURCE}$ = 100mA | 13.0 | 13.3 | | 12.5 | | | V |
| | | $V_{CC}$ = +5V, $I_{SOURCE}$ = 100mA | 3.0 | 3.3 | | 2.6 | | | V |
| $I_D$ | Discharge leakage current | | | 20 | 100 | | | 500 | nA |

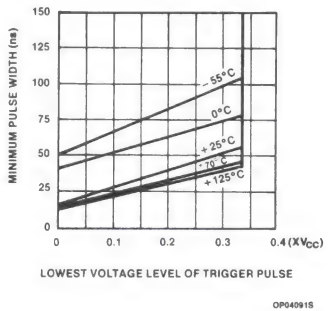
## AC ELECTRICAL CHARACTERISTICS $V_{CC}$ = +5V, $V_{CC}$ = +15V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{OFF}$ | Turn–off time[6, 7] | $V_{RESET} = V_{CC}$ | | 0.5 | 2.0 | | | | µs |
| $t_R$<br>$t_F$ | Rise time of output[7]<br>Fall time of output[7] | | | 100<br>100 | 200<br>200 | | | | ns<br>ns |

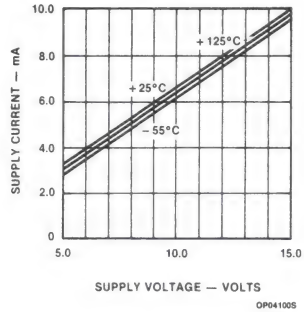
**NOTES:**
1. Operation beyond the limits in this table may impair the useful life of the device.
2. Supply current when output high typically 1mA less.
3. Tested at $V_{CC}$ = +5V and $V_{CC}$ = +15V.
4. This will determine the max. value of $R_A + R_B$, for 15V operation, the max. total R = 10MΩ, and for 5V operation, the max. total R = 3.4MΩ.
5. Specified with trigger input high.
6. Time measured from a positive going input pulse from 0 to 0.8 X $V_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.
7. This parameter is guaranteed but not tested.
8. Testing performed at $R_A$ = 100kΩ only.
9. Testing performed at $R_A = R_S$ = 1kΩ only.
10. For long term static operation, derate the sink and source currents to 50mA maximum.

## TYPICAL PERFORMANCE CHARACTERISTICS

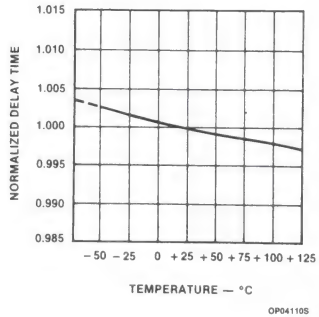
**Minimum Pulse Width Required for Triggering**



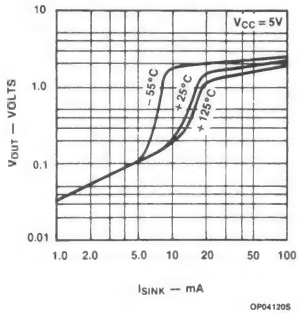

**Supply Current vs Supply Voltage**



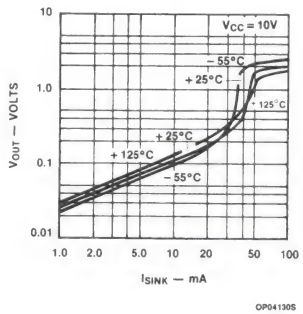

**Delay Time vs Temperature**



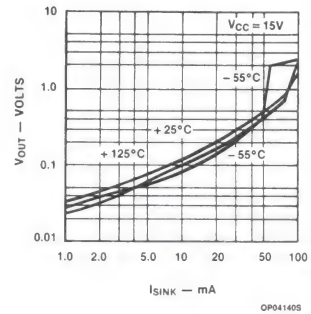

**Low Output Voltage vs Output Sink Current**



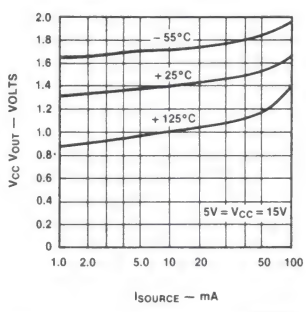

**Low Output Voltage vs Output Sink Current**



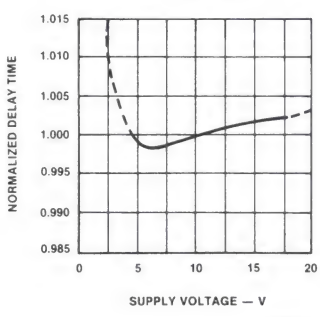

**Low Output Voltage vs Output Sink Current**



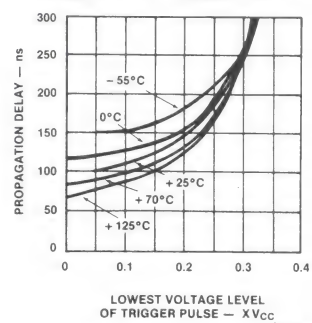

**High Output Voltage Drop vs Output Source Current**



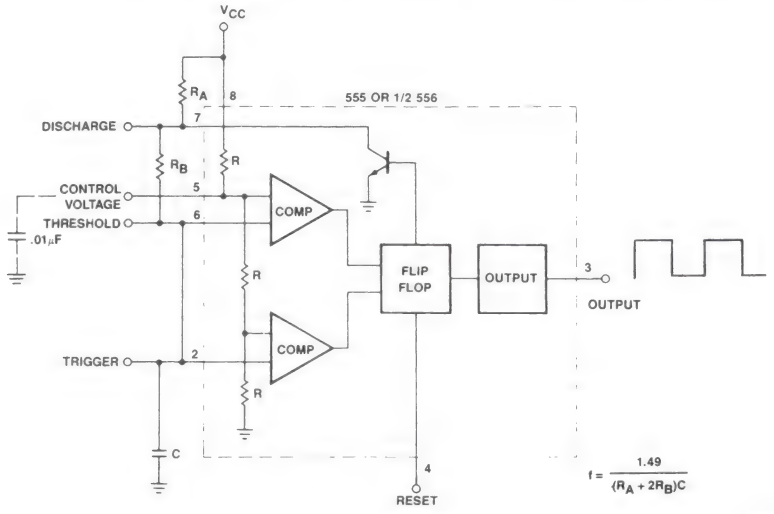

**Delay Time vs Supply Voltage**



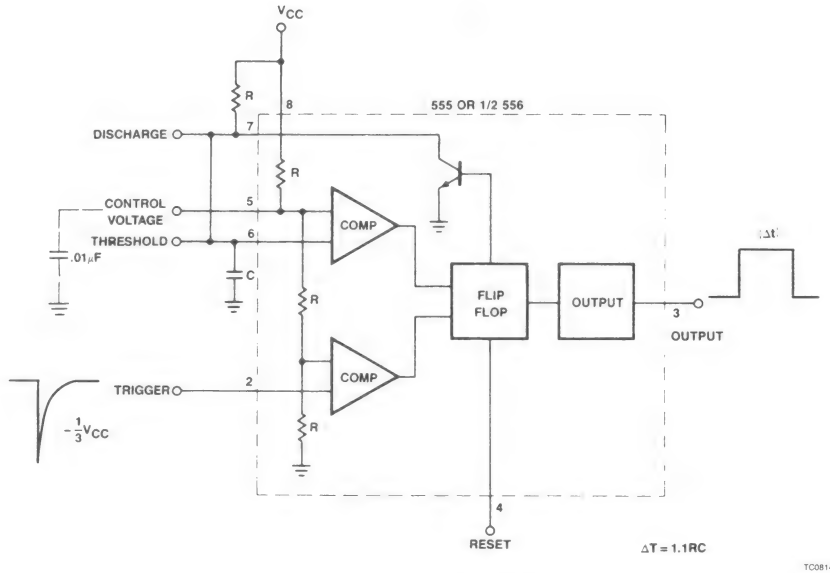

**Propagation Delay vs Voltage Level of Trigger Pulse**



## TYPICAL APPLICATIONS

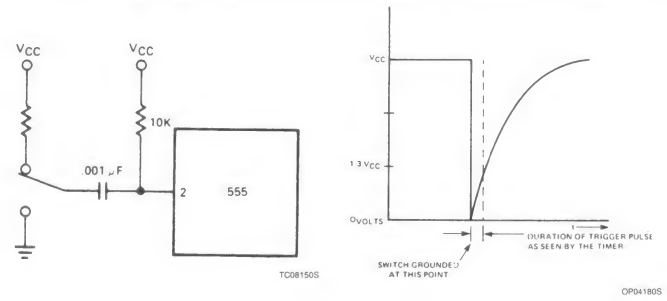



**Astable Operation**




**Monostable Operation**

## TYPICAL APPLICATIONS (Continued)




**NOTE:** All resistor values are in Ω.

**Figure 1. AC Coupling of the Trigger Pulse**

### Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger (see Figure 1), a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle, the output will remain in a high state for the duration of the low trigger signal without regard to the threshold comparator state. This is due to the predominance of $Q_{15}$ on the base of $Q_{16}$, controlling the state of the bistable flip–flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn–off time". This is the measurement of the amount of time required after the threshold reaches 2/3 $V_{CC}$ to turn the output low. To explain further, $Q_1$ at the threshold input turns on after reaching 2/3 $V_{CC}$, which then turns on $Q_5$, which turns on $Q_6$. Current from $Q_6$ turns on $Q_{16}$ which turns $Q_{17}$ off. This allows current from $Q_{19}$ to turn on $Q_{20}$ and $Q_{24}$ to give an output low. These steps cause the 2μs max. delay as stated in the data sheet.

Also, a delay comparable to the turn–off time is the trigger release time. When the trigger is low, $Q_{10}$ is on and turns on $Q_{11}$ which turns on $Q_{15}$. $Q_{15}$ turns off $Q_{16}$ and allows $Q_{17}$ to turn on. This turns off current to $Q_{20}$ and $Q_{24}$, which results in output high. When the trigger is released, $Q_{10}$ and $Q_{11}$ shut off, $Q_{15}$ turns off, $Q_{16}$ turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

Signetics

# 556-1
## Dual Timer

*Product Specification*

**Military Linear Products**

### DESCRIPTION

The 556-1 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556-1 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other, sharing only $V_{CC}$ and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

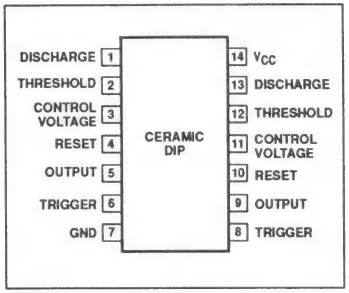
### FEATURES

- Turn-off time less than 2μs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

### APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Pulse position modulation
- Touch tone encoder

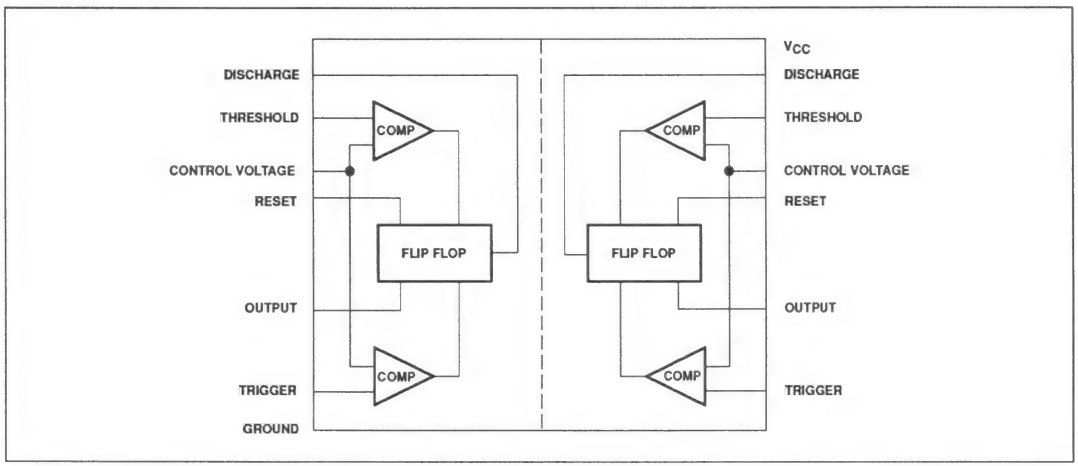
### PIN CONFIGURATION




### ORDERING INFORMATION

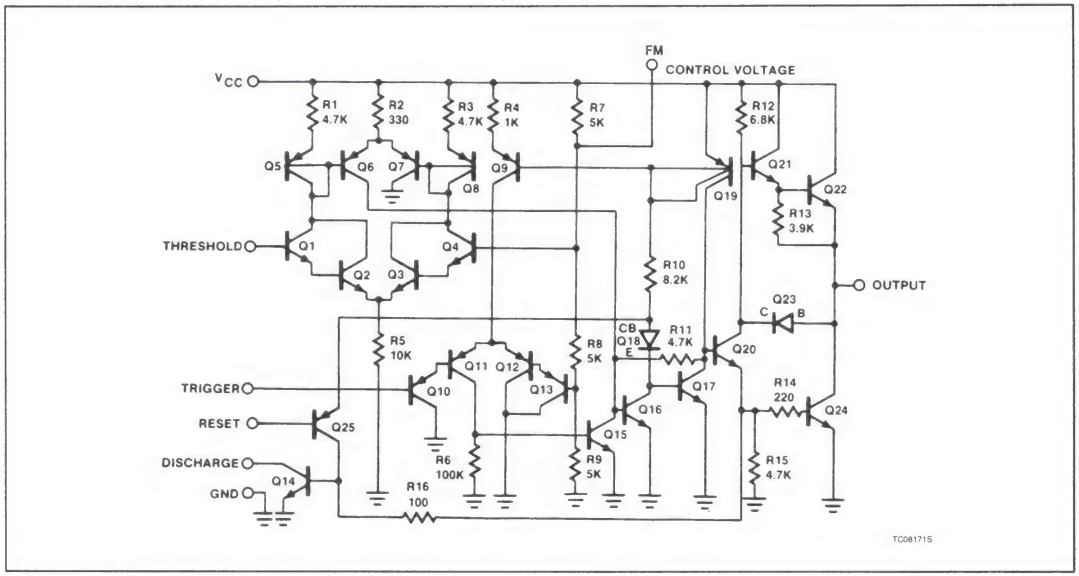
| DESCRIPTION | ORDER CODE |
|---|---|
| 14-Pin Ceramic DIP | 556-1/BCA |

### BLOCK DIAGRAM




®Touch-Tone is a registered trademark of AT&T

## EQUIVALENT SCHEMATIC (Shown for One Circuit Only)




## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +18 | V |
| $P_D$ | Power dissipation | 600 | mW |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

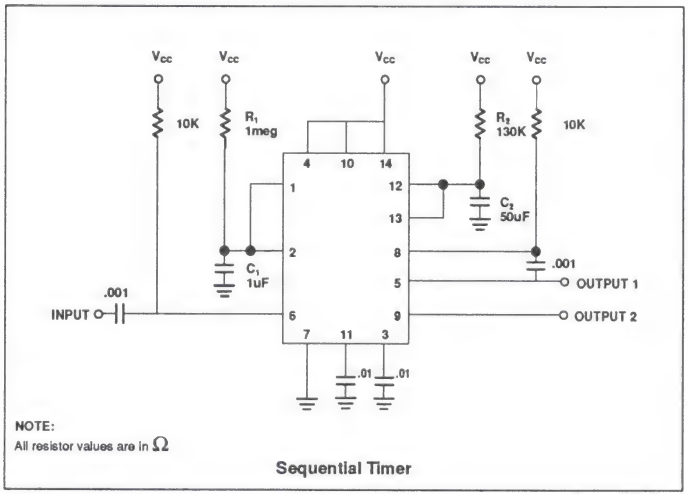
## DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | | 18 | 4.5 | | 18 | V |
| $I_{CC}$ | Supply current (low state)[2] | $V_{CC} = +5V$, $R_L = \infty$ | | 6 | 10 | | | 12 | mA |
| | | $V_{CC} = +15V$, $R_L = \infty$ | | 20 | 24 | | | 28 | mA |
| | Timing error (monostable) | $R_A = 2K\Omega$ to $100K\Omega$ | | | | | | | |
| $t_M$ | Initial accuracy[3] | C = 0.1µF | | 0.5 | 2.0 | | | 2.5 | % |
| $\Delta t_M/\Delta T$ | Drift with temperature[7,10] | T = 1.1 RC | | | | | | 100 | ppm/°C |
| $\Delta t_M/\Delta V_S$ | Drift with supply voltage | | | 0.05 | 0.2 | | | 0.25 | %/V |
| | Timing error (astable) | $R_A$, $R_B = 1k\Omega$ to $100k\Omega$ | | | | | | | |
| $t_A$ | Initial accuracy[3] | C = 0.1µF | | 4 | 6 | | | 10 | % |
| $\Delta t_A/\Delta T$ | Drift with temperature[7] | $V_{CC} = +15V$ | | | | | | 500 | ppm/°C |
| $\Delta t_A/\Delta V_S$ | Drift with supply voltage[9] | | | 0.15 | 0.6 | | | 1.5 | %/V |
| $V_C$ | Control voltage level | $V_{CC} = +15V$ | 9.6 | 10.0 | 10.4 | 9.6 | | 10.4 | V |
| | | $V_{CC} = +5V$ | 2.9 | 3.33 | 3.8 | 2.9 | | 3.8 | V |
| $V_{TH}$ | Threshold voltage | $V_{CC} = +15V$ | 9.4 | 10.0 | 10.6 | 9.4 | | 10.6 | V |
| | | $V_{CC} = +5V$ | 2.7 | 3.33 | 4.0 | 2.7 | | 4.0 | V |
| $I_{TH}$ | Threshold current[4] | $V_{TH} = 10.6V$ | | 0.03 | 0.25 | | | 0.35 | µA |
| $V_{TRIG}$ | Trigger voltage | $V_{CC} = +15V$ | 4.8 | 5.0 | 5.2 | 4.5 | | 5.5 | V |
| | | $V_{CC} = +5V$ | 1.45 | 1.67 | 1.9 | 1.5 | | 2.2 | V |
| $I_{TRIG}$ | Trigger current | $V_{TRIG} = 0V$ | | 0.5 | 0.9 | | | 2.0 | µA |
| $V_{RESET}$ | Reset voltage[5] | | 0.4 | 0.7 | 1.0 | 0.1 | | 1.3 | V |
| $I_{RESET}$ | Reset current | $V_{RESET} = 0.4V$ | | –0.1 | –0.4 | | | –1.6 | mA |
| $v_{OL}$ | Output voltage (low) | $V_{CC} = +15V$ | | | | | | | |
| | | $I_{SINK}$ = 10mA | | 0.1 | 0.15 | | | 0.25 | V |
| | | $I_{SINK}$ = 50mA | | 0.4 | 0.5 | | | 0.70 | V |
| | | $I_{SINK}$ = 100mA | | 0.8 | 1.2 | | | 1.6 | V |
| $V_{OL}$ | Output voltage (low) | $V_{CC} = +5V$ | | | | | | | |
| | | $I_{SINK}$ = 8mA | | 0.1 | 0.2 | | | 0.30 | V |
| | | $I_{SINK}$ = 5mA | | 0.05 | 0.15 | | | 0.20 | V |
| $V_{OH}$ | Output voltage (high) | $V_{CC} = +15V$ | | | | | | | |
| | | $I_{SOURCE} = -100mA$ | 13.0 | 13.3 | | 12.5 | | | V |
| | | $V_{CC} = +5V$ | | | | | | | |
| | | $I_{SOURCE} = -100mA$ | 3.0 | 3.3 | | 2.6 | | | V |
| $I_D$ | Discharge leakage current | | | 20 | 100 | | | 500 | nA |
| | Matching characteristics[7,8] | | | | | | | | |
| $\Delta t_D$ | Initial accuracy[3,7] | | | 0.5 | 1.0 | | | | % |
| $\Delta t_D/\Delta T$ | Drift with temperature[7] | | | | | | 10 | | ppm/°C |
| $\Delta t_D/\Delta V_S$ | Drift with supply voltage[7] | | | 0.1 | 0.2 | | | | %/V |

## AC ELECTRICAL CHARACTERISTICS $V_{CC}$ = +5V to +15V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{OFF}$ | Turn–off time[6, 7] | $V_{RESET} = V_{CC}$ | | 0.5 | 2.0 | | | | µs |
| $t_R$ | Rise time of output[7] | | | 100 | 200 | | | | ns |
| $t_F$ | Fall time of output[7] | | | 100 | 200 | | | | ns |

**NOTES:**
1. Operation beyond the limits in this table may impair the useful life of the device.
2. Supply current when output is high is typically 1.0mA less.
3. Tested at $V_{CC}$ = 5V and $V_{CC}$ = 15V.
4. This will determine the max value of $R_A + R_B$,. For 15V operation, the max total R = 10MΩ, and for 5V operation, the max total R = 3.4mΩ.
5. Specified with trigger input high.
6. Time measured from a positive going input pulse from 0 to 0.4 $V_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.
7. This parameter is guaranteed, but not tested.
8. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
9. Testing performed at $R_A = R_B$ = 100kΩ.
10. Testing performed at $R_A$ = 100kΩ only.




NOTE:
All resistor values are in Ω

**Sequential Timer**

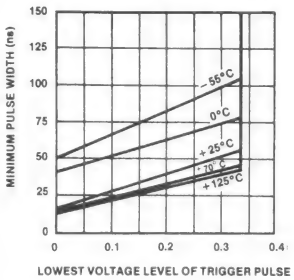
## TYPICAL APPLICATIONS

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001µfd coupling capacitor sequential timing may be obtained. Delay $t_1$ is determined by the first half and $t_2$ by the second half delay.

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed out (determined by $1.1R_1C_1$) the second half begins. Its duration is determined by $1.1R_2C_2$.

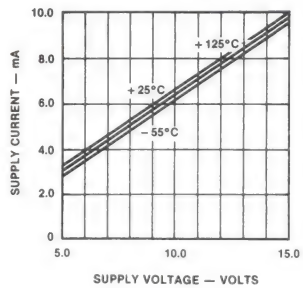
## TYPICAL PERFORMANCE CHARACTERISTICS

**Minimum Pulse Width Required for Triggering**



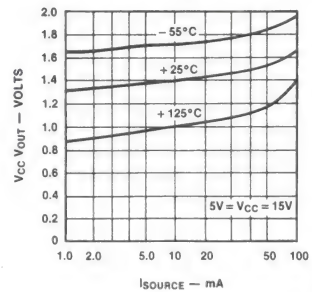

OP04191S

**Supply Current vs Supply Voltage**



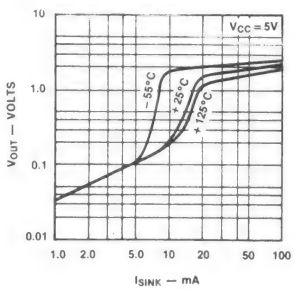

OP04200S

**High Output Voltage Drop vs Output Source Current**



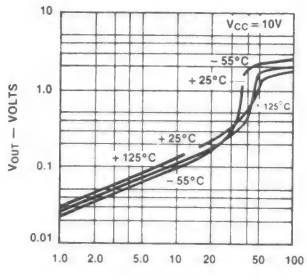

OP04210S

**Low Output Voltage vs Output Sink Current**



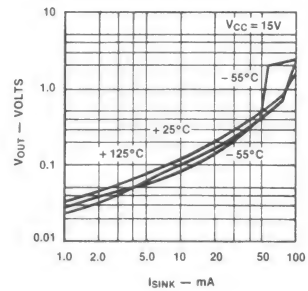

OP04220S

**Low Output Voltage vs Output Sink Current**



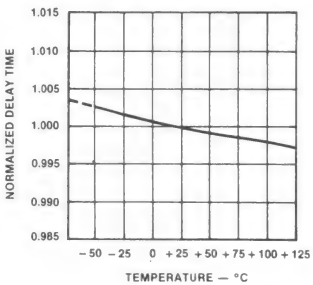

OP04230S

**Low Output Voltage vs Output Sink Current**



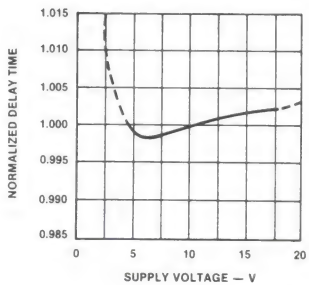

OP04240S

**Delay Time vs Temperature**



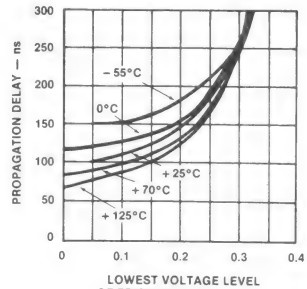

OP04250S

**Delay Time vs Supply Voltage**




OP04260S

**Propagation Delay vs Voltage Level of Trigger Pulse**




OP04270S

Signetics

# 567
## Tone Decoder/Phase-Locked Loop

*Product Specification*

**Military Communications and Industrial Products**

### DESCRIPTION

The 567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

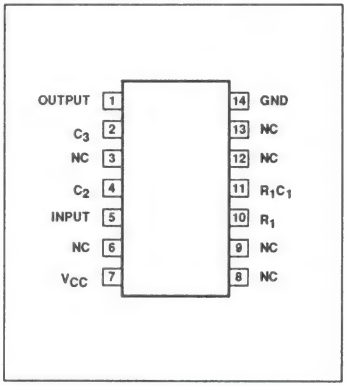
### FEATURES

- Wide frequency range (0.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor

### APPLICATIONS

- Touch Tone® decoding
- Carrier-current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

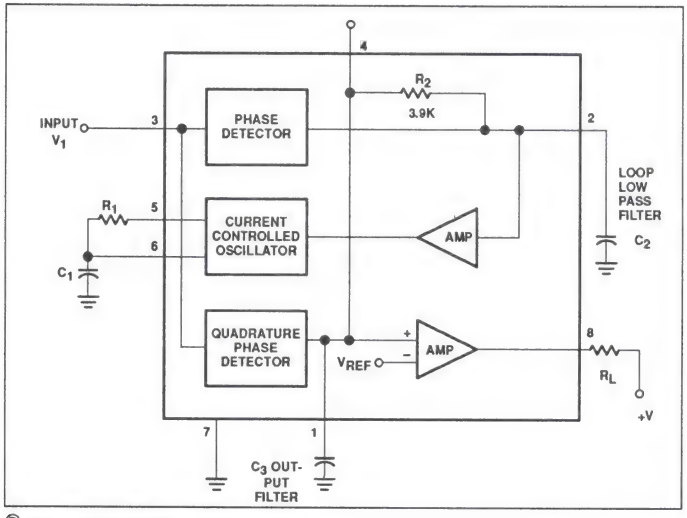
### PIN CONFIGURATION




### ORDERING INFORMATION

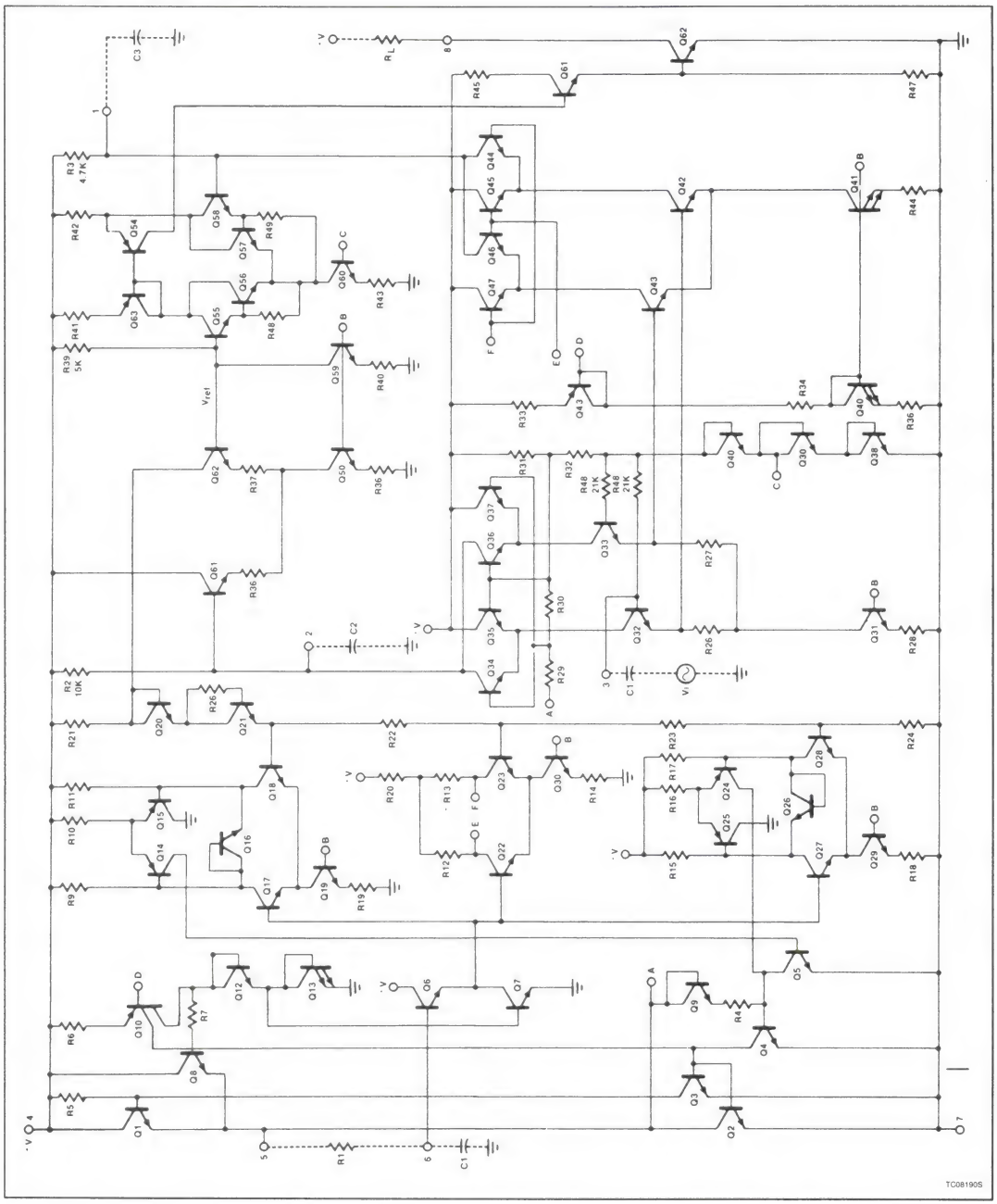
| DESCRIPTION | ORDER CODE |
|---|---|
| 14-Pin Ceramic DIP | 567/BCA |

### BLOCK DIAGRAM




®Touch Tone is a registered trademark of AT & T.

## EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 10 | V |
| $V_I$ | Positive voltage at input | 0.5 + $V_S$ | V |
| $V_I$ | Negative voltage at input | –10 | $V_{DC}$ |
| $V_O$ | Output voltage (collector of output transistor) | 15 | $V_{DC}$ |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $P_D$ | Power dissipation | 300 | mW |

## DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = +5V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125oC | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **Center Frequency[2]** | | | | | | | | | |
| $f_o$ | Highest center frequency | | | 500 | | | | | kHz |
| $\Delta f_o/\Delta T$ | Center frequency stability with temperature[3] | | | | | | 35<br>±140 | | ppm/°C |
| $\Delta f_o$ | Center frequency distribution | $f_o$ = 100kHz ≃ $1.1/R_1C_1$ | –10 | 0 | +10 | –10 | | +10 | % |
| $\Delta f_o/\Delta V_S$ | Center frequency shift with supply voltage | $f_o$ = 100kHz ≃ $1.1/R_1C_1$ | | 0.5 | 1 | | | | %/V |
| **Detection Bandwidth** | | | | | | | | | |
| DBW | Largest detection bandwidth | $f_o$ = 100kHz ≃ $1.1/R_1C_1$ | 12 | 14 | 16 | 7 | | 19 | % of $f_o$ |
| ΔDBW | Largest detection bandwidth skew | | | 2 | 4 | | | 4 | % of $f_o$ |
| ΔDBW/ ΔT | Largest detection bandwidth–variation with temperature | $V_I$ = 300m$V_{RMS}$ | | | | | ±0.1 | | %/°C |
| ΔDBW/ $\Delta V_{CC}$ | Largest detection bandwidth–variation with supply voltage | $V_I$ = 300m$V_{RMS}$ | | ±2 | | | | | %/V |
| **Input** | | | | | | | | | |
| $R_{IN}$ | Input resistance[5] | | 15 | 20 | 25 | | | | kΩ |
| $V_{IN}$ | Smallest detectable input voltage | $I_L$ = 100mA, $f_i = f_o$ | | 20 | 25 | | | 50 | $mV_{RMS}$ |
| $V_{IN}$ | Largest no–output input voltage | $I_L$ = 100mA, $f_i = f_o$ | 7 | 15 | | 5 | | | $mV_{RMS}$ |
| $V_{OB}/V_{IB}$ | Greatest simultaneous outband signal–to–inband signal ratio | | | +6 | | | | | dB |
| $V_{1MIN/EN}$ | Minimum input signal to wideband noise ratio | $B_n$ = 140kHz | | –6 | | | | | dB |
| **Output** | | | | | | | | | |
| $I_{OH}$ | Fastest on–off cycling rate | | | $f_o/20$ | | | | | |
| $V_{OL}$ | "1" output leakage current | $V_B$ = 15V | | 0.01 | 25 | | | 50 | µA |
| | "0" output voltage[6] | $I_L$ = 30mA | | 0.2 | 0.4 | | | 0.4 | V |
| | | $I_L$ = 100mA | | 0.6 | 1.0 | | | 1.2 | V |
| $t_f$ | Output fall time[4] | $R_L$ = 50Ω | | 30 | | | | | ns |
| $t_r$ | Output rise time[4] | $R_L$ = 50Ω | | 150 | | | | | ns |

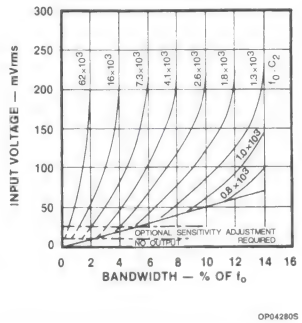
## DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = +5V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **Power Supply** | | | | | | | | | |
| $V_{CC}$ | Operating voltage range | | 4.75 | | 9.0 | 4.75 | | 9.0 | V |
| $I_{CC}$ | Supply current quiescent | | | 6 | 8 | | | 9.8 | mA |
| | Supply current – activated | $R_L$ = 20kΩ | | 11 | 13 | | | 14.5 | mA |
| $P_D$ | Quiescent power dissipation | | | 30 | | | | | mW |

**NOTES:**
1. Operation beyond limits in this table may impair the useful life of the device.
2. Frequency determining resistor $R_1$ should be between 2 and 20kΩ.
3. Applicable over 4.75V to 5.75V. See graphs for more detailed information.
4. Pin 8 to Pin 1 feedback $R_L$ network selected to eliminate pulsing during turn–on and turn–off.
5. Guaranteed, but not tested.
6. For long term static operation, derate the sink current to 85mA maximum.

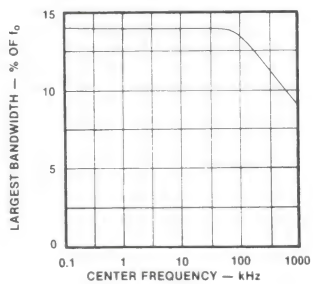
## TYPICAL PERFORMANCE CHARACTERISTICS

Bandwidth vs Input Signal Amplitude



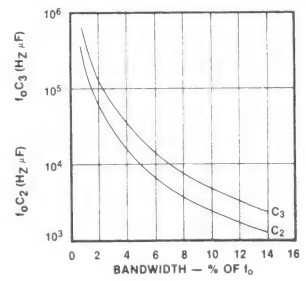

OP04280S

Largest Detection Bandwidth vs Operating Frequency




OP04290S

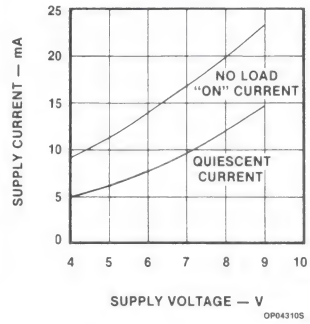
Detection Bandwidth as a Function of $C_2$ and $C_3$



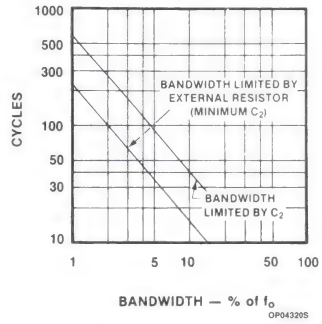

OP04300S

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

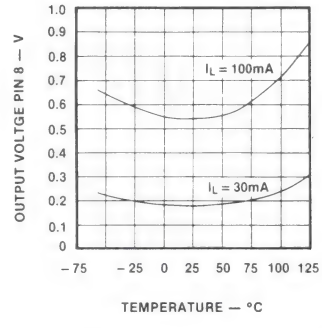
Typical Supply Current vs Supply Voltage



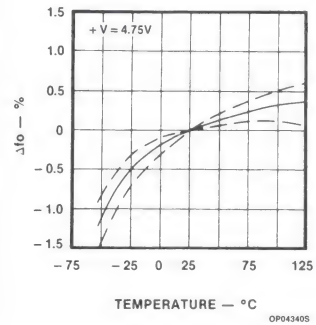

Greatest Number of Cycles Before Output



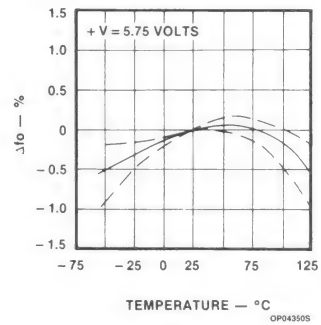

Typical Output Voltage vs Temperature



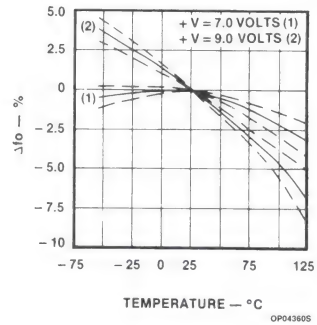

Typical Frequency Drift With Temperature (Mean and SD)



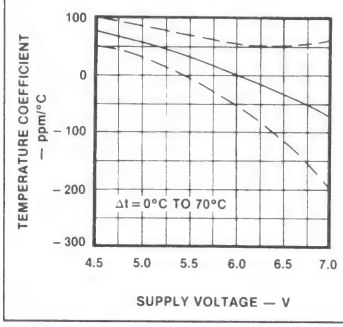

Typical Frequency Drift With Temperature (Mean and SD)



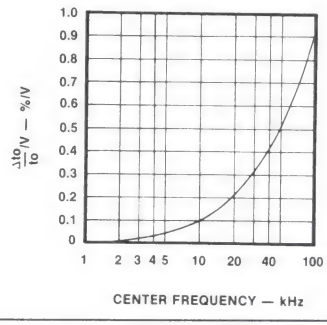

Typical Frequency Drift With Temperature (Mean and SD)



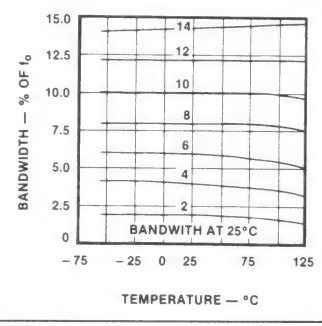

Center Frequency Temperature Coefficient (Mean and SD)




Center Frequency Shift With Supply Voltage Change vs Operating Frequency




Typical Bandwidth Variation Temperature



## DESIGN FORMULAS

$$f_o \cong \frac{1.1}{R_1 C_1}$$

$$BW \simeq 1070 \sqrt{\frac{V_1}{f_o C_2}} \text{ in \% of } f_o,$$
$$V_1 \leq 200mV_{RMS}$$

Where

$V_1$ = Input Voltage ($V_{RMS}$)
$C_2$ = Low–Pass Filter Capacitor (μF)

## PHASE–LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (fo)

The free–running frequency of the current–controlled oscillator (CCO) in the absence of an input signal.

### Detection Bandwidth (BW)

The frequency range, centered about $f_o$, within which an input signal above the threshold voltage (typically $20mV_{RMS}$) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

### Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

### Detection Band Skew

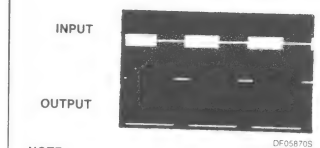
A measure of how well the detection band is centered about the frequency, $f_o$. The skew is defined as $(f_{MAX} + f_{MIN} - 2f_o)/2f_o$ where $f_{MAX}$ and $f_{MIN}$ are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

## OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three–step procedure will be sufficient for choosing the external components $R_1$, $C_1$, $C_2$ and $C_3$.

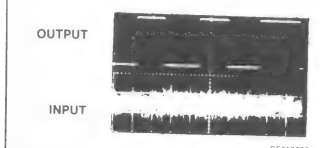
1. Select $R_1$ and $C_1$ for the desired center frequency. for best temperature stability, $R_1$ should be between 2kΩ and 20kΩ, and the combined temperature coefficient of the $R_1C_1$ product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low pass capacitor, $C_2$, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of $f_oC_2$ necessary to give the desired bandwidth may be found. Conversely, an are of operation may be selected on this graph and theinput level and $C_2$ may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above $200mV_{RMS}$. The bandwidth, as noted on the graph, is then controlled solely by the $f_oC_2$ product ($F_o$ (Hz), $C_2$ (μfd)).
3. The value of $C_3$ is generally non–critical. $C_3$ sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If $C_3$ is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn–on transient. If $C_3$ is too large, turn–on and turn–off of the output stage will be delayed until the voltage on $C_3$ passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical min. value for $C_3$ is $2C_2$.
4. Optional resistor $R_2$ sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of $10mV_{RMS}$ min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

## TYPICAL RESPONSE




NOTE:
$R_L = 100Ω$

**Response to $100mV_{RMS}$ Tone Burst**




NOTES:
S/N = –6dB
$R_L = 100Ω$
Noise Bandwidth = 140Hz

**Response to Same Input Tone Burst With Wideband Noise**

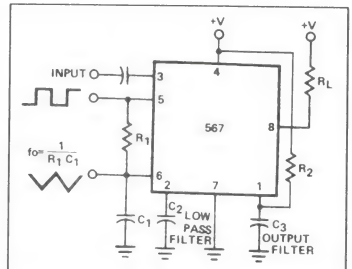



**Figure 1**

## AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, Pin 8. When an in–band input signal is present, this transistor saturates; its collector voltage being less than 1.0V (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 $f_o$ with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{BE}) \approx (+V - 1.4V)$ having a DC average of +V/2. A 1kΩ load may be driven from Pin 5. Pin 6 is an exponential triangle of $1V_{P-P}$ with an average DC level of +V/2. Only high impedance loads may be connected to Pin 6 without affecting the CCO duty cycle or temperature stability.

## OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in–band signal amplitude. The input stage is now limiting, however, so that out–band signals or high noise levels can cause an apparent bandwidth reduction as the in–band signal is suppressed. Also, the limiting action will create in–band components from sub–harmonic signals, so the 567 becomes sensitive to signals at $f_o/3$, $f_o/5$, etc.
2. The 567 will lock onto signals near $(2n + 1)$ $f_o$, and will give an output for signals near $(4n + 1)$ $f_o$ where n = 0, 1, 2, etc. Thus, signals at $5f_o$ and $9f_o$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and output band signals is afforded in the low input level (below 200mV$_{RMS}$) and reduced bandwidth operating mode. However, decreased loop damping causes the worse–case lockup time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a min. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn–on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow–band systems sufficiently to cause momentary loss of lock. the result is a low–frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

## SPEED OF OPERATION

Min. lock–up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn–on transient. Thus, max. operating speed is obtained when $C_2$ is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock–up transient is at its worst and the theoretical minimum lock–up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of $C_2$ and $C_3$ which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn–on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}\ \mu F$$

$$C_3 = \frac{260}{f_o}\ \mu F$$

In cases where turn–off time can be sacrificed to achieve fast turn–on, the optional sensitivity adjustment circuit can be used to move the quiescent $C_3$ voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

## OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

## SENSITIVITY ADJUSTMENT (Figure 3)

When operated as a very narrow band detector (less than 8%), both $C_2$ and $C_3$ are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to Terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

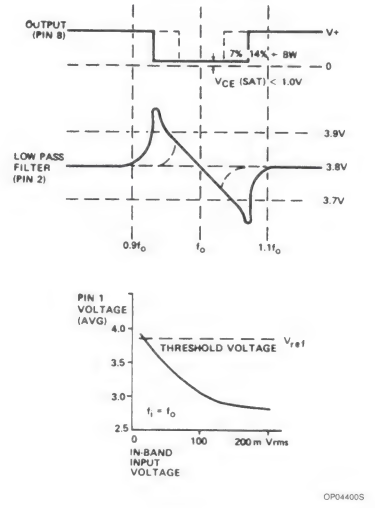



Figure 2

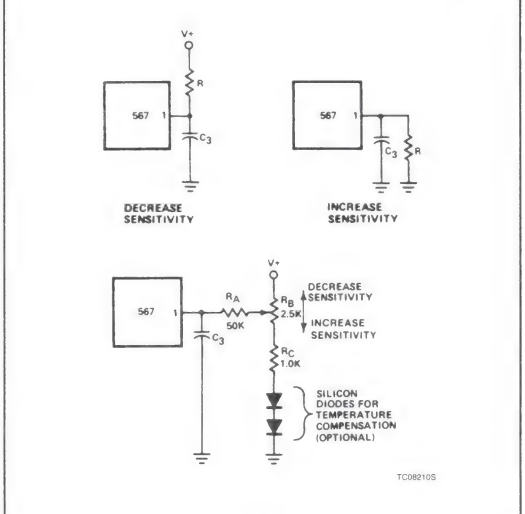



Figure 3

By adding current to Terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, $C_2$ and $C_3$ are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in–band harmonics (of lower–frequency signals) is also improved.

## CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when $C_3$ is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making $C_3$ large, the feedback circuit will enable faster operation of the 567 by allowing $C_3$ to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

## DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT (Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown in Figure 5 can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since $R_B$ also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

## ALTERNATE METHOD OF BANDWIDTH REDUCTION (Figure 6)

Although a large value of $C_2$ will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow–band conditions. Note that the reduced impedance level at Terminal 2 will require that a larger value of $C_2$ be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of $R_B$ and $R_C$ can be eliminated and the $R_A$ resistors connected together. A capacitor between this junction and ground may be required to shunt high–frequency components.

## OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

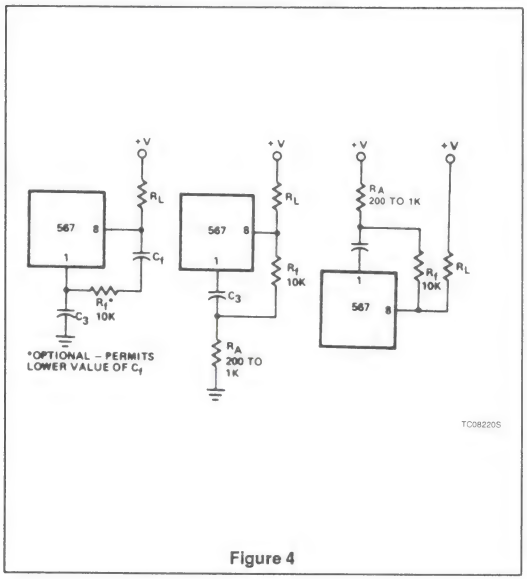



Figure 4

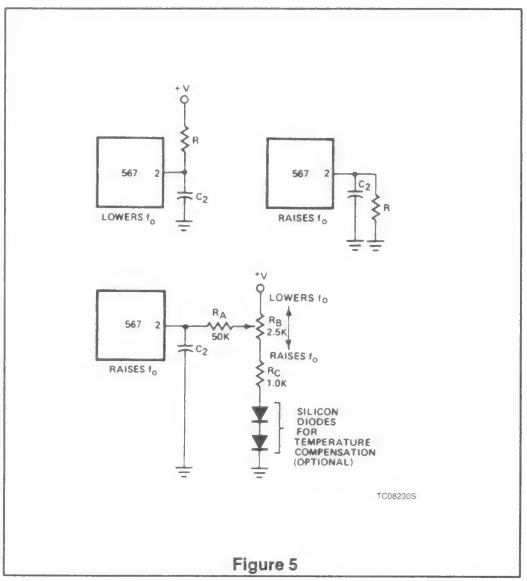


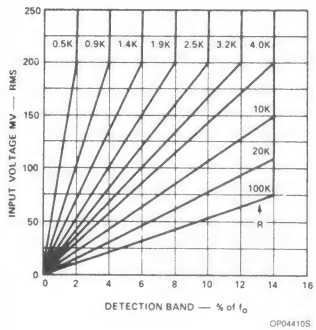

Figure 5

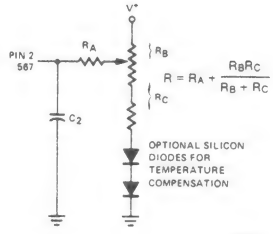
## REDUCTION OF C1 VALUE (Figure 8)

For precision very low–frequency applications, where the value of $C_1$ becomes large, an overall cost savings may be achieved by inserting a voltage follower between the $R_1$ $C_1$ junction and Pin 6, so as to allow a higher value of $R_1$ and a lower value of $C_1$ for a given frequency.

## PROGRAMMING

To change the center frequency, the value of $R_1$ can be changed with a mechanical or solid–state switch, or additional $C_1$ capacitors may be added by grounding them through saturating npn transistors.



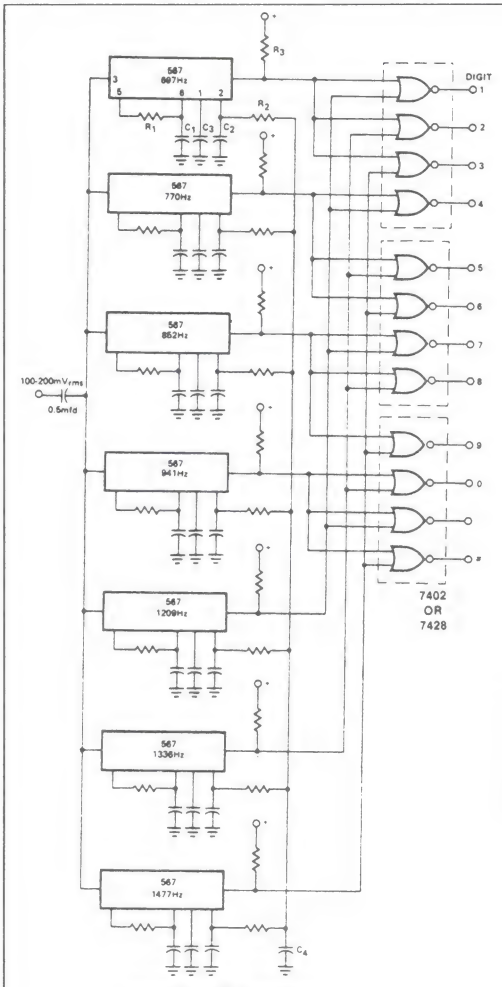




$$\frac{130}{f_O}\left(\frac{10k+R}{R}\right) < C_2 < \frac{1300}{f_O}\left(\frac{10k+R}{R}\right)$$

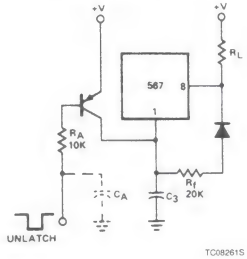
Adjust control for symmetry of detection band edges about $f_O$.

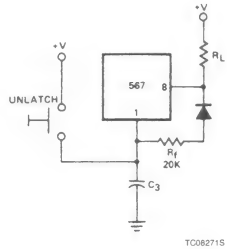
**NOTE:**
Adjust control for symmetry of detection band edges about $f_O$.

**Figure 6**




**Touch-Tone® Decoder**




**NOTE:**
$C_A$ prevents latch-up when power supply is turned on.

**Figure 7. Output Latching**

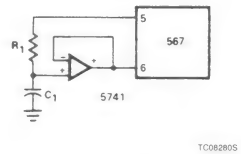
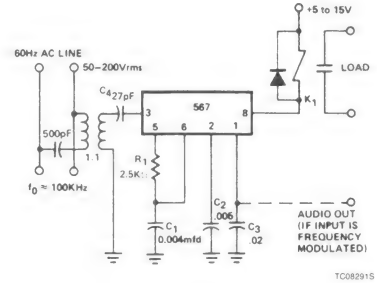
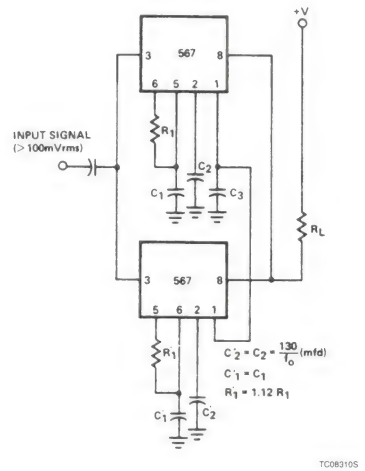



**Figure 8. Precision VLF**

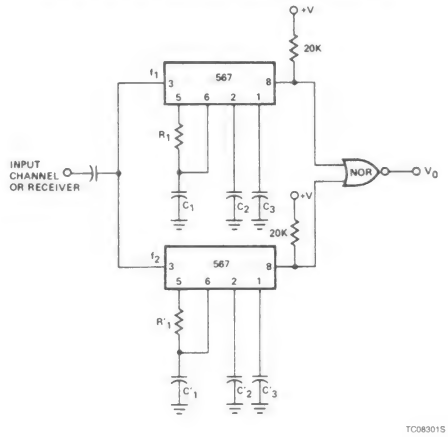
## TYPICAL APPLICATIONS



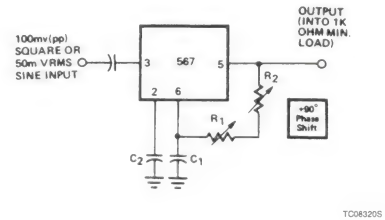

**Carrier-Current Remote Control or Intercom**




**24% Bandwidth Tone Decoder**




**Dual-Tone Decoder**

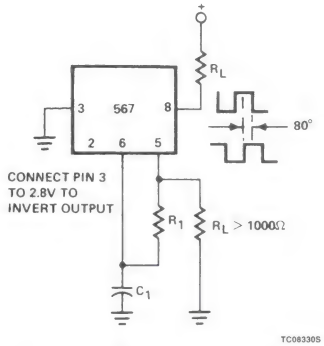



**NOTES**
$R_2 = R_1/5$
Adjust $R_1$ so that $\phi = 90°$ with control midway.

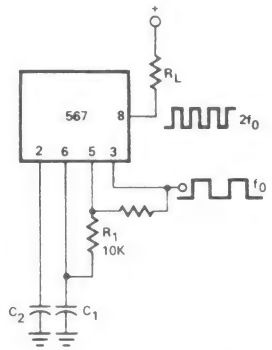
**0° to 180° Phase Shifter**

**NOTES:**
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If $C_3$ is made large so as to delay turn-on of the top 567, decoding of sequential ($f_1$ $f_2$) tones is possible.

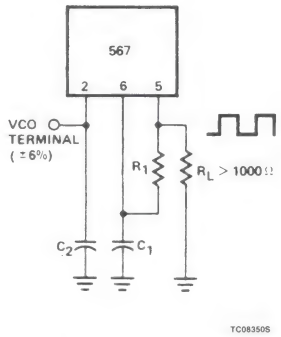
## TYPICAL APPLICATIONS (Continued)



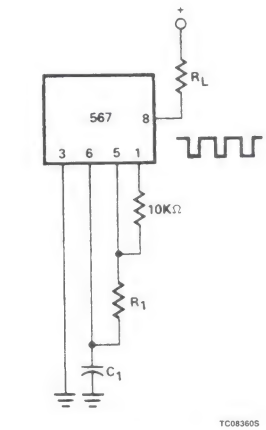

Oscillator With Quadrature Output



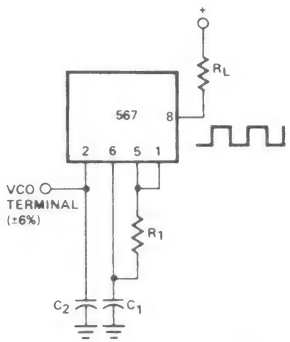

Oscillator With Double Frequency Output



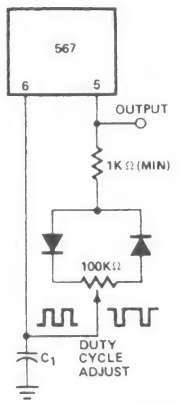

Precision Oscillator With 20ns Switching




Pulse Generator With 25% Duty Cycle




Precision Oscillator to Switch 100mA Loads




Pulse Generator

Signetics

# 592
## Video Amplifier

*Product Specification*

**Military Linear Products**

### DESCRIPTION

The 592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

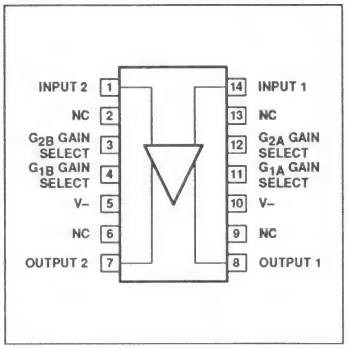
### FEATURES

- 120MHz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components

### APPLICATIONS

- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

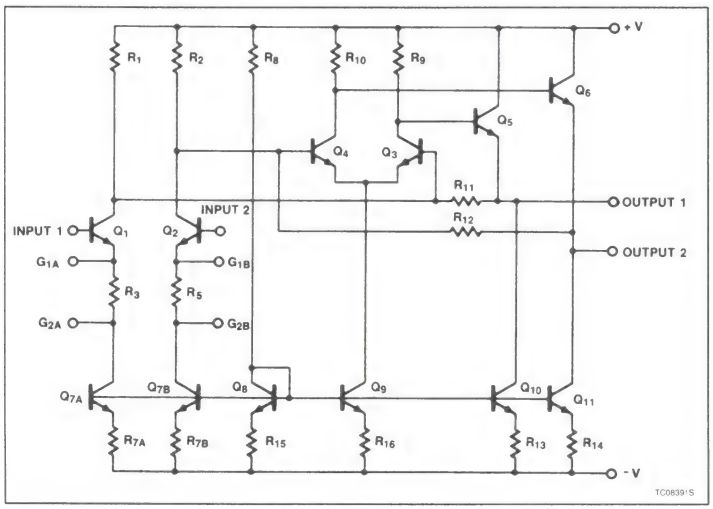
### PIN CONFIGURATION




### ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | ±8 | V |
| $V_{ICD}$ | Differential input voltage | ±5 | V |
| $V_{ICR}$ | Common mode input voltage range | ±6 | V |
| $I_O$ | Output current | 10 | mA |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $P_D$ | Power dissipation | 500 | mW |

### EQUIVALENT SCHEMATIC




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 14-PIN Ceramic DIP | 592/BCA |

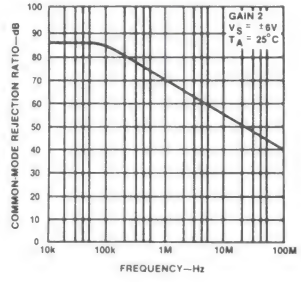
## ELECTRICAL CHARACTERISTICS $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | Differential voltage gain, standard part | | | | | | | | |
| $A_{DIF1}$ | Gain 1[2] | $R_L = 2k\Omega$, $V_{IN} = \pm 5mV$ | 300 | 400 | 500 | 200 | | 600 | V/V |
| $A_{DIF2}$ | Gain 2[3] | $R_L = 2k\Omega$, $V_{IN} = \pm 25mV$ | 90 | 100 | 110 | 80 | | 120 | V/V |
| | Bandwidth | | | | | | | | |
| $BW_1$ | Gain 1[2] | $V_O = 1V_{p-p}$ | | 40 | | | | | MHz |
| $BW_2$ | Gain 2[3] | | | 90 | | | | | MHz |
| | Rise time | | | | | | | | |
| $t_{R1}$ | Gain 1[2] | $V_O = 1V_{p-p}$ | | 10.5 | | | | | ns |
| $t_{R2}$ | Gain 2[3] | | | 4.5 | | | | | ns |
| | Propagation delay | | | | | | | | |
| $t_{PD1}$ | Gain 1[2] | $V_O = 1V_{p-p}$ | | 7.5 | | | | | ns |
| $t_{PD2}$ | Gain 2[3] | | | 6.0 | 10 | | | | ns |
| | Input resistance | | | | | | | | |
| $R_{IN1}$ | Gain 1[2] | | | 4.0 | | | | | kΩ |
| $R_{IN2}$ | Gain 2[3, 5] | | 20 | 30 | | 8 | | | kΩ |
| $C_{IN}$ | Input capacitance[3] | Gain 2 | | 2.0 | | | | | pF |
| $I_{IO}$ | Input offset current | | | 0.4 | 3.0 | | | 5.0 | μA |
| $I_{IB}$ | Input bias current | | | 9.0 | 20 | | | 40 | μA |
| $E_N$ | Input noise voltage | BW 1kHz to 10MHz | | 12 | | | | | μVrms |
| $V_{ICR}$ | Input voltage range | | ±1.0 | | | ±1.0 | | | V |
| | Common mode rejection ratio | | | | | | | | |
| $CMRR_2$ | Gain 2 | $V_{CM} \pm 1V$ | 60 | 86 | | 50 | | | dB |
| $CMRR_2$ | Gain 2 | $V_{CM} \pm 1V$, f = 5MHz | | 60 | | | | | dB |
| | Supply voltage rejection ratio | | | | | | | | |
| PSRR | Gain 2 | $\Delta V_S = \pm 0.5V$ | 50 | 70 | | 50 | | | dB |
| | Output offset voltage | $R_S = 50\Omega$, $R_L = \infty$ | | | | | | | |
| $V_{IO1}$ | Gain 1 | | | | 1.5 | | | 1.5 | V |
| $V_{IO2}$ | Gain 2 | | | | 1.0 | | | 1.2 | V |
| $V_{IO3}$ | Gain 3[4] | | | 0.35 | 0.75 | | | 1.0 | V |
| $V_{OCM}$ | Output common mode voltage | $R_S = 50\Omega$, $R_L = \infty$ | 2.4 | 2.9 | 3.4 | | | | V |
| $I_{SINK}$ | Output sink current | | 2.5 | | | 2.2 | | | mA |
| $V_{ODIF}$ | Output voltage swing differential | $R_L = 2k\Omega$ | 3.0 | 4.0 | | 2.5 | | | V |
| $R_O$ | Output resistance | | | 20 | | | | | Ω |
| $I_S$ | Power supply current | $R_L = \infty$ | | 18 | 24 | | | 27 | mA |

**NOTES:**
1. Operation beyond limits in the table may impair the useful life of the devices.
2. Gain select Pins $G_{1A}$ and $G_{1B}$ connected together.
3. Gain select Pins $G_{2A}$ and $G_{2B}$ connected together.
4. All gain pins open.
5. Guaranteed, but not tested.

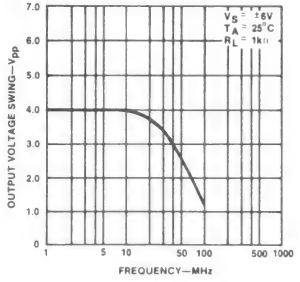
## TYPICAL PERFORMANCE CHARACTERISTICS

### Common-Mode Rejection Ratio as a Function of Frequency



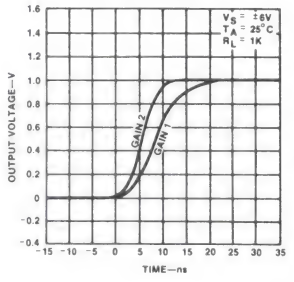

OP04421S

### Output Voltage Swing as a Function of Frequency



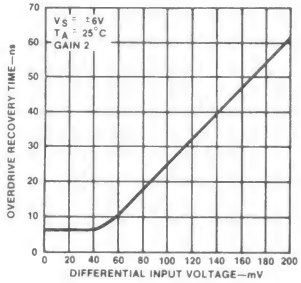

OP04430S

### Pulse Response



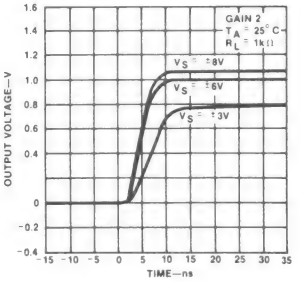

OP04440S

### Differential Overdrive Recovery Time



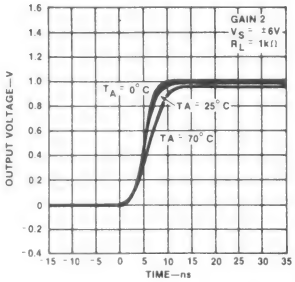

OP04450S

### Pulse Response as a Function of Supply Voltage



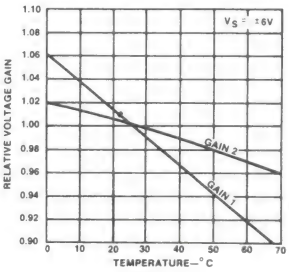

OP04460S

### Pulse Response as a Function of Temperature



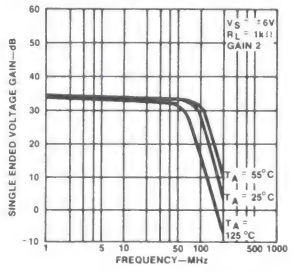

OP04470S

### Voltage Gain as a Function of Temperature



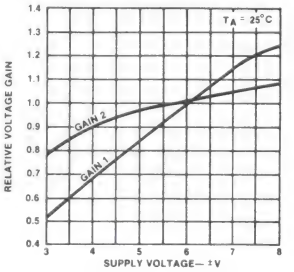

OP04480S

### Gain vs Frequency as a Function of Temperature




OP04490S

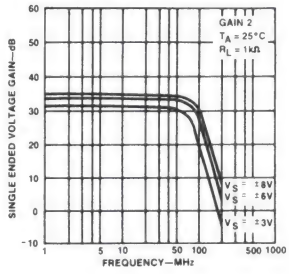
### Voltage Gain as a Function of Supply Voltage




OP04500S

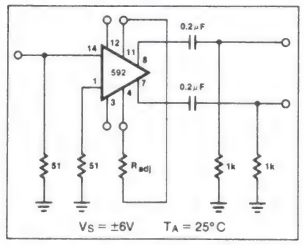
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

**Gain vs Frequency as a Function of Supply Voltage**



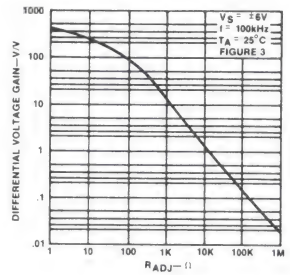

OP04510S

**Voltage Gain Adjust Circuit**



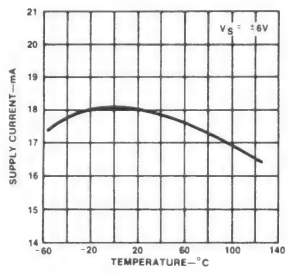

OP04521S

**Voltage Gain as a Function of RADJ (Figure 3)**



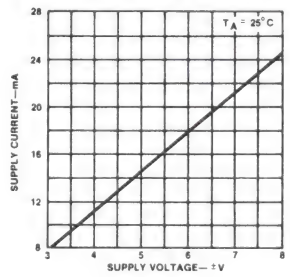

OP04530S

**Supply Current as a Function of Temperature**



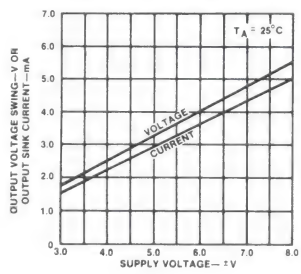

OP04540S

**Supply Current as a Function of Supply Voltage**



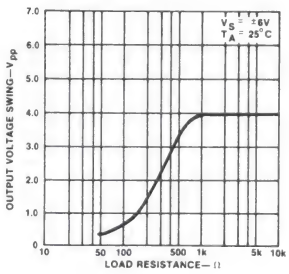

OP04550S

**Output Voltage and Current Swing as a Function of Supply Voltage**



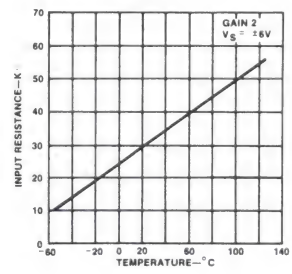

OP04560S

**Output Voltage Swing as a Function of Load Resistance**



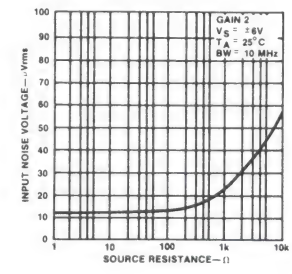

OP04570S

**Input Resistance as a Function of Temperature**




OP04580S

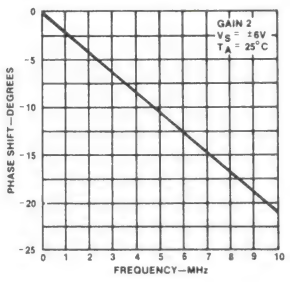
**Input Noise Voltage as a Function of Source Resistance**




OP04590S

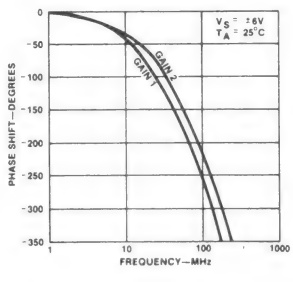
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Phase Shift as a Function of Frequency



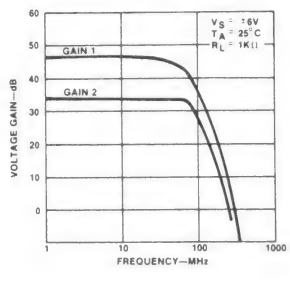

OP04600S

Phase Shift as a Function of Frequency



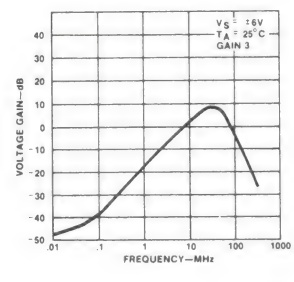

OP04610S

Voltage Gain as a Function of Frequency



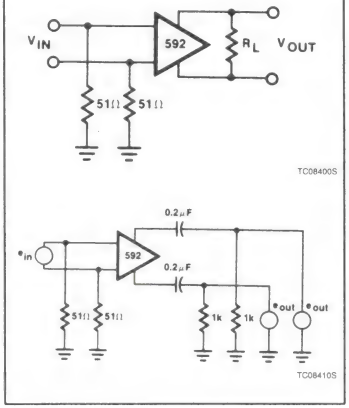

OP04620S

Voltage Gain as a Function of Frequency (All Gain Select Pins Open)

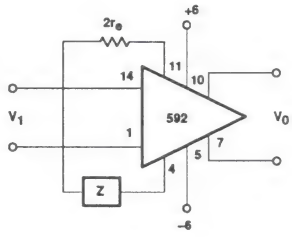



OP04630S

## TEST CIRCUITS

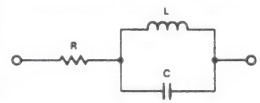


# Video Amplifier 592




$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

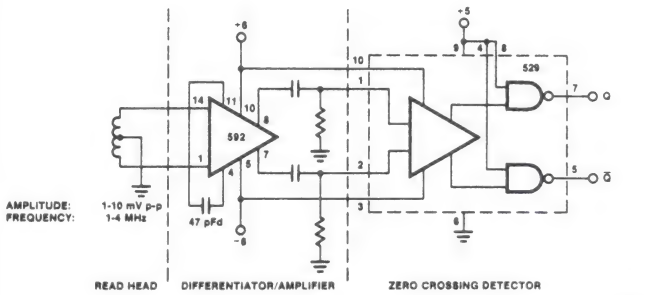
$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

| Z NETWORK | FILTER TYPE | $V_0$ (s) TRANSFER $V_1$ (s) FUNCTION |
|---|---|---|
| | LOW PASS | $\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$ |
| | HIGH PASS | $\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$ |
| | BAND PASS | $\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\ s + 1/LC}\right]$ |
|  | BAND REJECT | $\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$ |

TC08422S

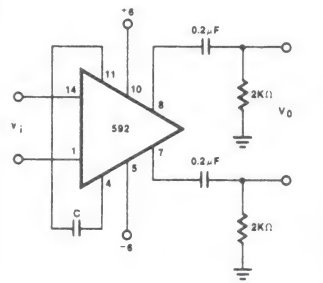
**NOTES:**
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

**Filter Networks**




TC08430S

**DISC/Tape Phase Modulated Readback Systems**




TC08440S

**NOTE:**
For frequency $F_1 << 1/2\pi(32)C$

$V_0 \cong 1.4 \times 10^4 C\frac{dVi}{dT}$

**Differentiation With High Common Mode Noise Rejection**

Signetics

# 602
## Double-Balanced Mixer and Oscillator

*Product Specification*

**Military Linear Products**

### DESCRIPTION

The 602 is a low-power VHF monolithic double-balanced mixer with input amplifier, on board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the 602 make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 14dB of grain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the 602 a superior choice for high-performance batter operated equipment.

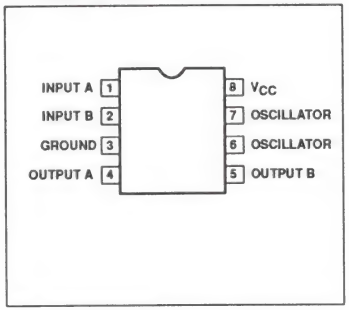
### FEATURES

- **Low current consumption: 2.4mA typical**
- **High operating frequency**
- **Excellent gain, Intercept and sensitivity**
- **Excellent noise figure: <5.0dB typical at 45MHz**
- **Low external parts count; suitable for crystal/ceramic filters**

### APPLICATIONS

- **Cellular radio mixer/oscillator portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LANs**

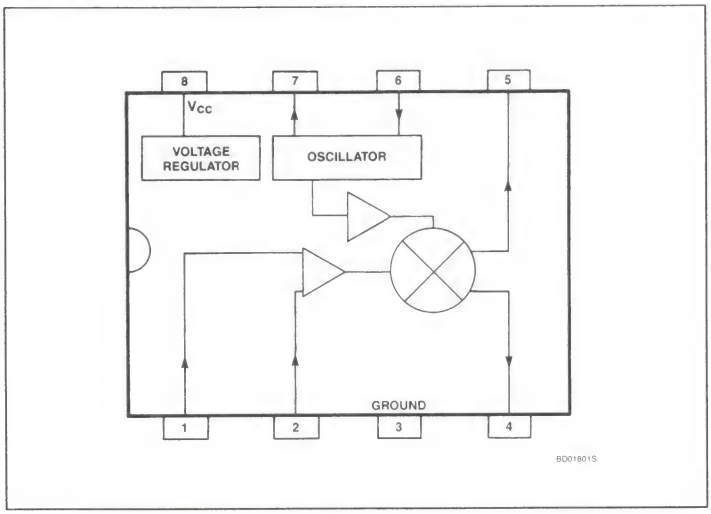
### PIN CONFIGURATION




### ORDERING INFORMATION

| PACKAGES | ORDER CODE |
|---|---|
| 8-Pin Ceramic DIP | 602/BPA |

### BLOCK DIAGRAM



# Double–Balanced Mixer and Oscillator 602

## ABSOLUTE MAXIMUM RATINGS[3]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Maximum operating voltage | 8 | V |
| $T_{STG}$ | Storage temperature | –65 to +150 | °C |
| $T_A$ | Operating ambient temperature range | –55 to +125 | °C |

## AC/DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = 6V, –55°C ≤ $T_A$ ≤ +125°C, Figure 1

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| $V_{CC}$ | Power supply voltage range | | 4.5 | | 7.0 | V |
| $I_{CC}$ | DC current drain | | | 2.5 | 4.0 | mA |
| $f_{IN}$ | Input signal frequency | | | 500 | | MHz |
| $f_{OSC}$ | Oscillator frequency | | | 500 | | MHz |
| NF | Noise figured at 45MHz | | | 5.0 | | dB |
| | Third–order intercept point | $RF_{IN}$ = –45dBm: $f_1$ = 45.0, $f_2$ = 45.06 | | –16 | –32 | dBm |
| A | Conversion gain at 45MHz | | 8 | 14 | | dB |
| $R_{IN}$ | RF input resistance[2] | | 1.5 | 3.5 | | kΩ |
| $C_{IN}$ | RF input capacitance[2] | | | 3 | 3.5 | pF |
| $R_O$ | Mixer output resistance | (Pin 4 or 5) | | 1.5 | | kΩ |

**NOTES:**

4. All typical values are at +25°C only and $V_{CC}$ = 6.0V
5. This parameter is guaranteed but not tested.
6. Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations section or this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DESCRIPTION OF OPERATION

The 602 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The 602 is designed for optimum low power performance. When used with the 604A as a 45MHz cellular radio 2nd IF and demodulator, the 602 is capable of receiving –119dBm signals with a 12dB S/N ratio. Third–order intercept is typically –15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be congnizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small–signal or signal–to–noise issues not critical, the input to the 602 should be appropriately scaled.

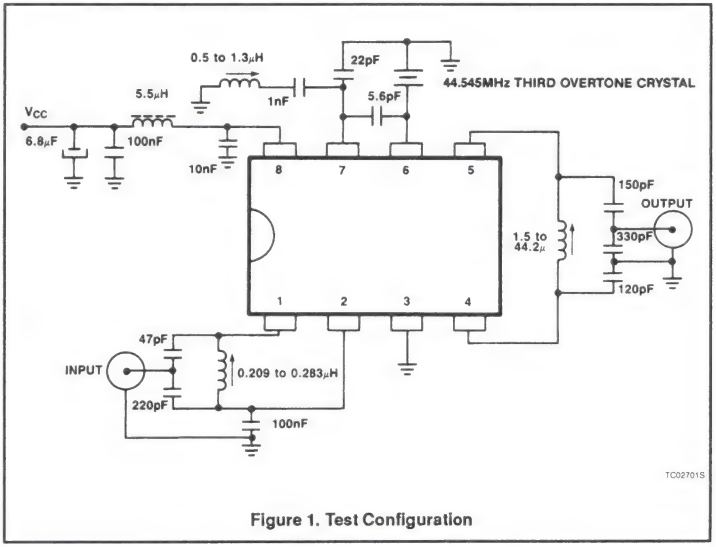



**Figure 1. Test Configuration**

# Double–Balanced Mixer and Oscillator 602

Besides excellent low power performance well into VHF, the 602 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k ll 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations. The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be at least 200m$V_{p-p}$.

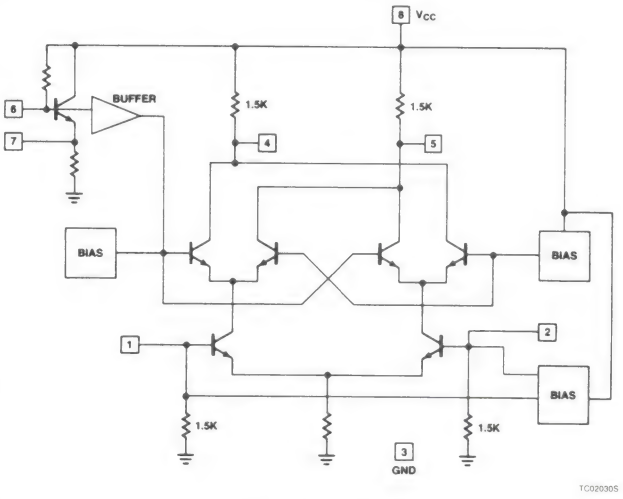
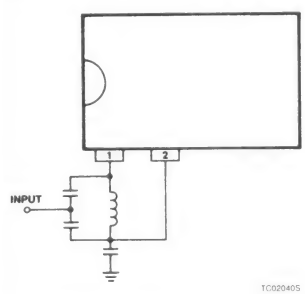



Figure 2. Equivalent Circuit

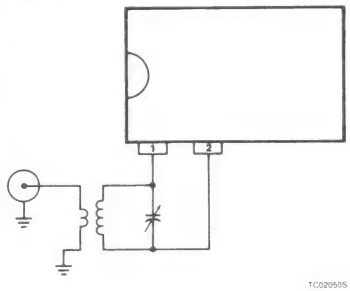
Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer–controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual–gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non–critical applications. The resistive divider in the emitter–follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

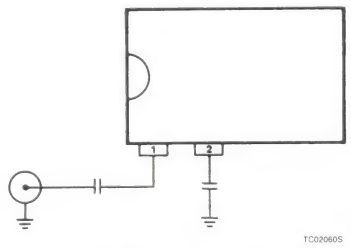
When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. 22kΩ will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided..




a. Single-Ended Tuned Input

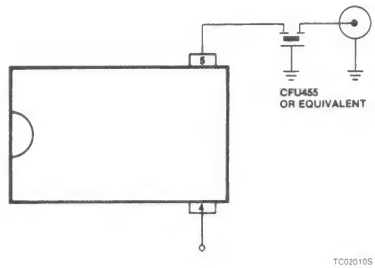



b. Balanced Input (For Attenuation of Second-Order Products)

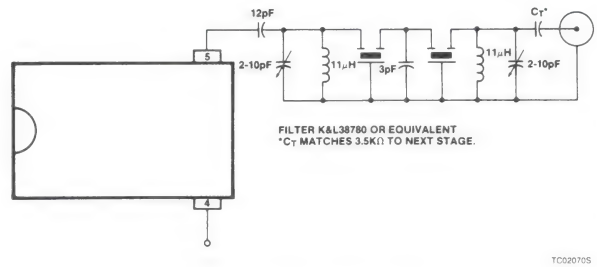



c. Single-Ended Untuned Input

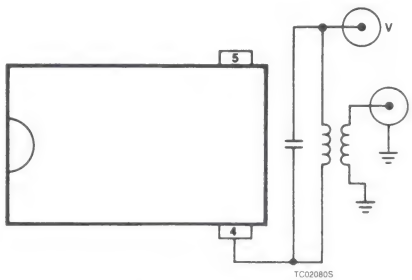
Figure 3. Input Configuration



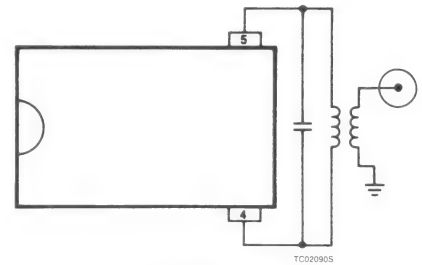

a. Single-Ended Ceramic Filter




b. Single-Ended Crystal Filter

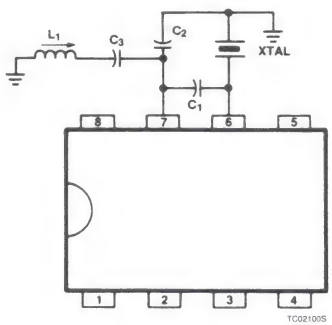



c. Single-Ended IFT

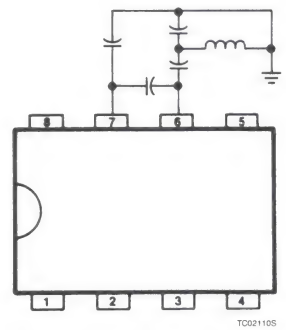



d. Balanced Output

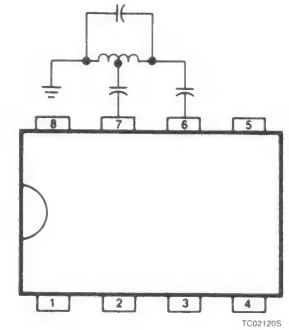
Figure 4. Output Configuration




a. Colpitts Crystal Oscillator (Overtone Mode)




b. Colpitts L/C Tank Oscillator




c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

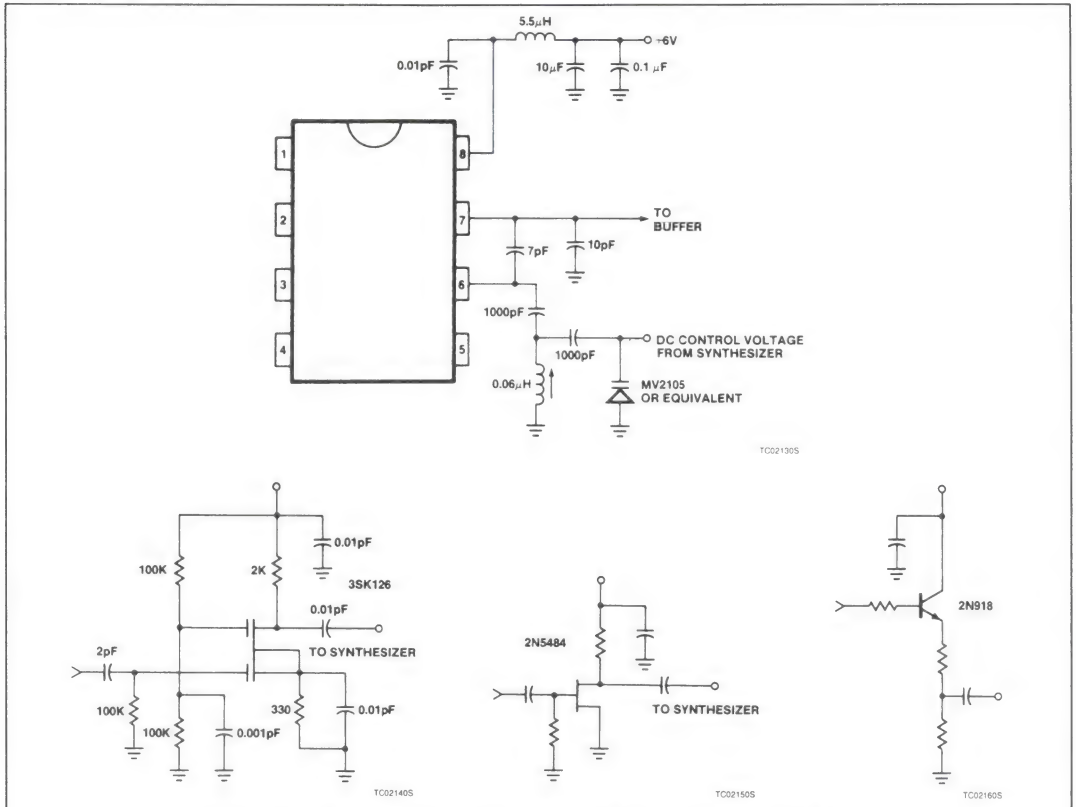



Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

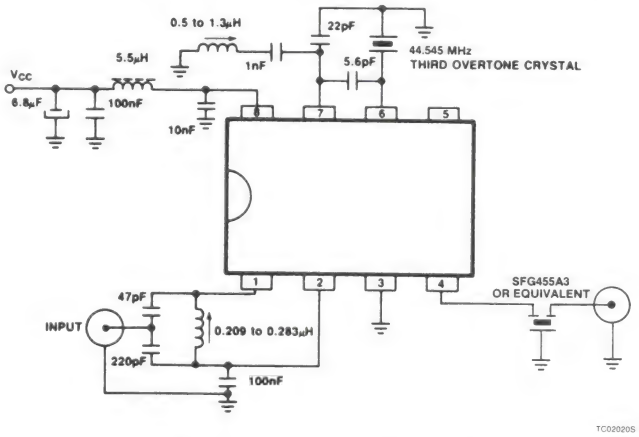



Figure 7. Typical Application for Cellular Radio

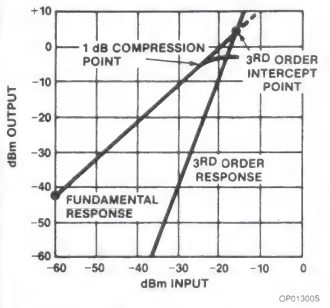



Figure 8. 602 Third-Order Intermod and 1dB Compression Point Performance

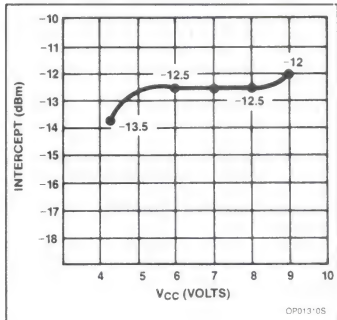



Figure 9. Input Third-Order Intercept Point vs $V_{CC}$

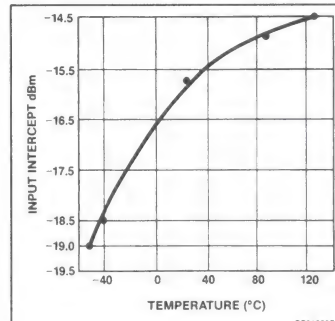
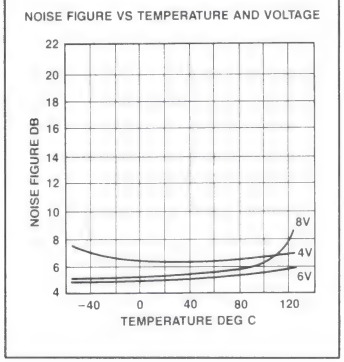
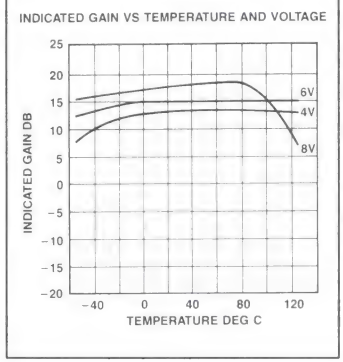
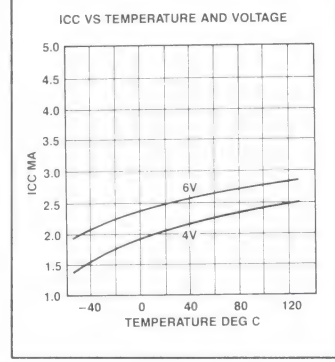



Figure 10. Third-Order Intercept Point vs Temperature



Signetics

# 604A

## High-Performance Low-Power FM IF System

*Product Specification*

Military Linear Products

### DESCRIPTION

The 604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator.

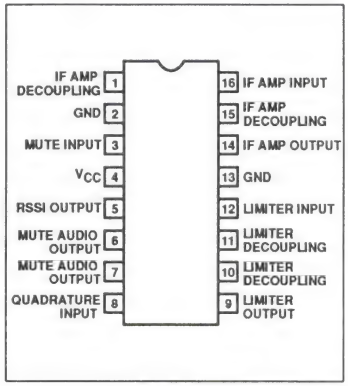
### FEATURES

- Low-Power consumption 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs — muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- 604A meets cellular radio specifications

### APPLICATIONS

- Cellular Radio FM IF
- High Performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

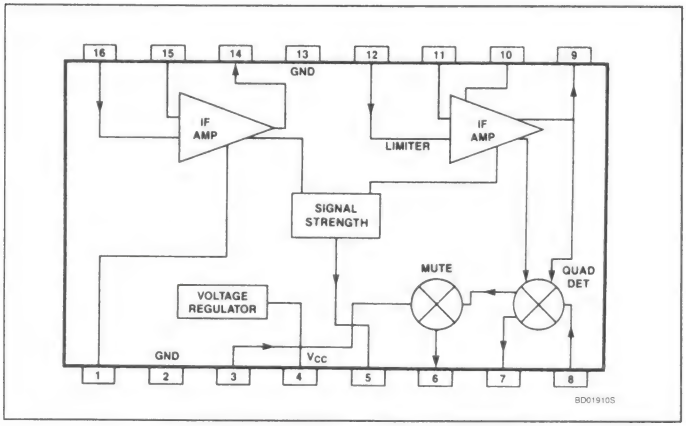
### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 16-Pin Ceramic DIP | 604A/BEA |

### BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | 9 | V |
| $T_{STG}$ | Storage Temperature Range | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS |
|---|---|---|
| $V_{CC}$ | Power Supply Voltage | 6V |
| $T_A$ | Operating Temperature Range | –55°C to 125°C |

## DC ELECTRICAL CHARACTERISTICS –55°C to 125°C, $V_{CC}$ = +6V, unless otherwise stated.

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| | Power Supply Voltage Range | | 4.5 | | 8.0 | V |
| | DC Current Drain ICC | | | 3.3 | 4.2 | mA |
| | Mute Switch Input Threshold ON | | 1.7 | | | V |
| | Mute Switch Input Threshold OFF | | | | 1.0 | V |

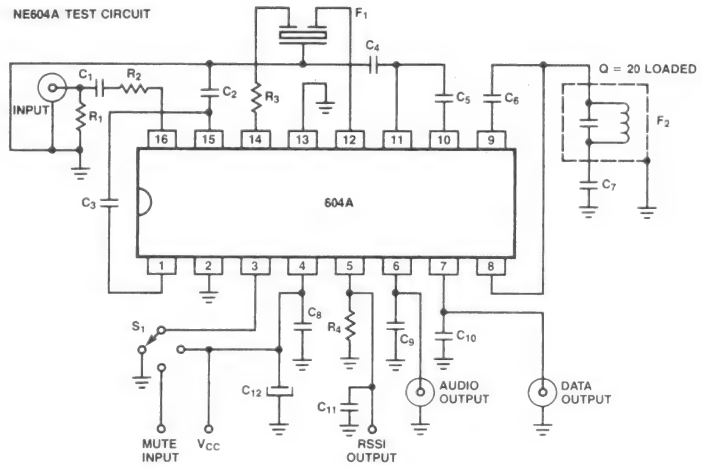
## AC ELECTRICAL CHARACTERISTICS

At –55°C to 125°C $V_{CC}$ = +6V, unless otherwise stated. IF frequency = 455kHz; IF level = –47dBm, FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C–message weighted filter and de–emphasis capacitor. Test Circuit Figure 1. The Parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| | Input limiting | Test at Pin 16 | | –91 | | dBM |
| | AM rejection | 80% AM 1kHz | –20 | –32 | | dB |
| | Recovered audio level | 15nF de–emphasis | 60 | 160 | | mVrms |
| | Recovered data level | 150pF de–emphasis | | 520 | | mVrms |
| | SINAD sensitivity | RF level –97dBm | | 14 | | dB |
| | THD | | –25 | –38 | | dB |
| | Signal–to–noise ratio | No modulation for noise | | 72 | | dB |
| | | RF level = –97dBm | 0 | 240 | 600 | mV |
| | | RF level = –47dBm | 1.8 | 2.65 | 3.2 | V |
| | | RF level = +3dBm | 3.5 | 4.85 | 5.5 | V |
| | RSSI range | $R_4$ = 100k Pin 5 | | 90 | | dB |
| | RSSI accuracy | $R_4$ = 100k Pin 5 | | ±1.5 | | dB |
| | IF input impedance | Note 1 | 1.5 | | | kΩ |
| | IF output impedance | Note 1 | 1.0 | | | kΩ |
| | Limited output impedance | Note 1 | 1.5 | | | kΩ |
| | Unmuted audio output impedance | | | 55 | | kΩ |
| | Muted audio output impedance | | | 55 | | kΩ |

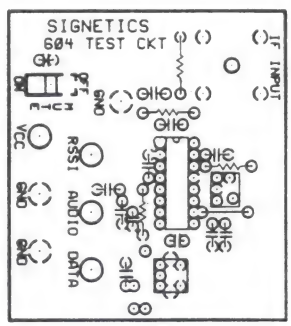
**NOTES:**

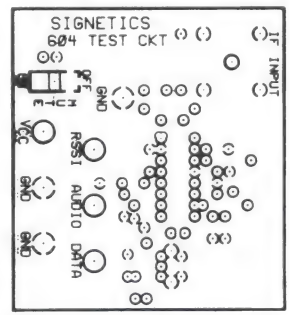
1. This parameter is guaranteed but not tested.
2. All typical values at $V_{CC}$ = +6.0V, $T_A$ = 25°C.




**NOTES:**

C1 10nF +80 – 20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V
C3 100nF ± 10% 50V
C4 100nF ± 10% 50V
C5 100nF ± 10% 50V
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V
C8 100nF ± 10% 50V
C9 15nF ± 10% 50V
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8uF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ± 1% ¼W Metal Film
R2 1500Ω ± 1% ¼W Metal Film
R3 1500Ω ± 5% ⅛W Carbon Composition
R4 100kΩ ± 1% ¼W Metal Film



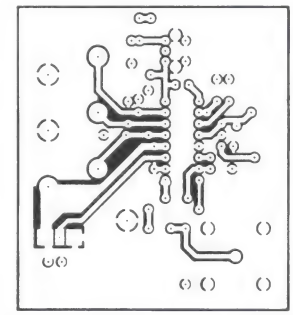




**Figure 1. 604A Test Circuit**

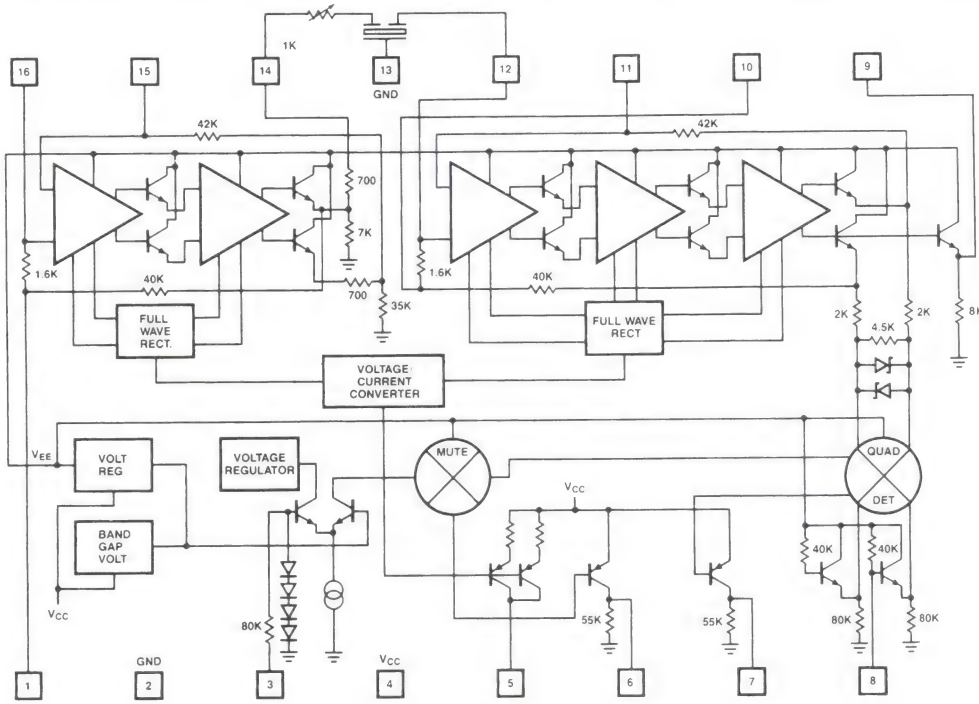



**Figure 2. Equivalent Circuit**

## CIRCUIT DESCRIPTION

The 604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The 604A can not be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The 604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub–systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

## IF AMPLIFIERS

The IF amplifier section consists of two log–limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

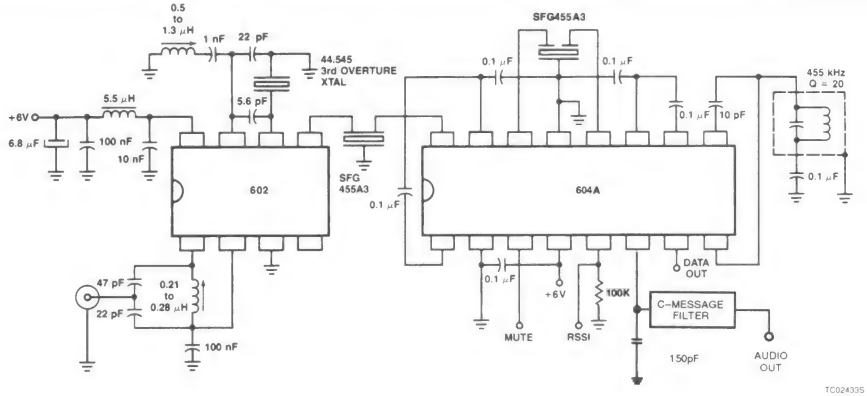
Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2 the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including the RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1) The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are

shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the 604A IF amplifiers, which is not specified is low phase shift. The 604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.



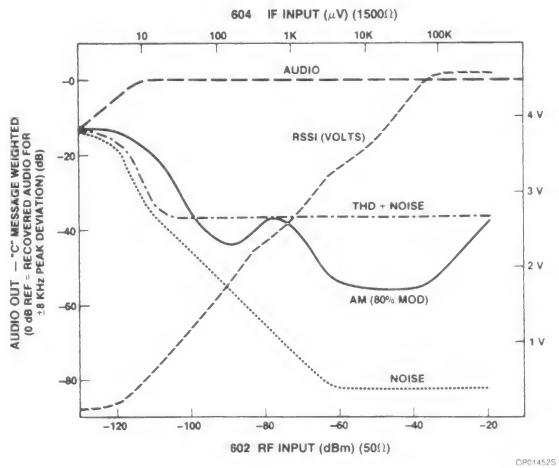




**Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)**

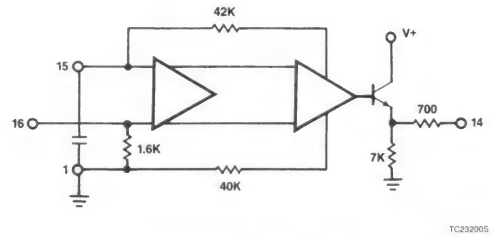



Figure 4. First Limiter Bias

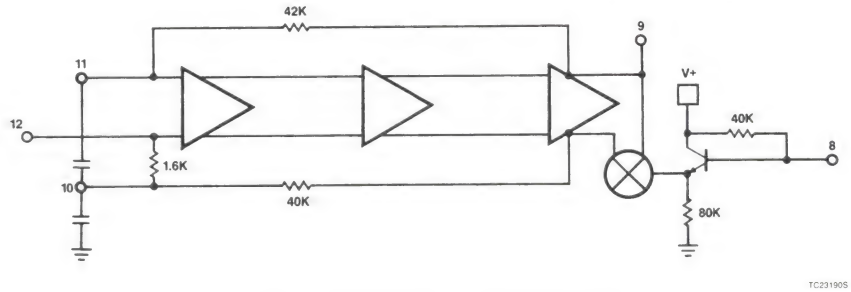



Figure 5. Second Limiter and Quadrature Detector

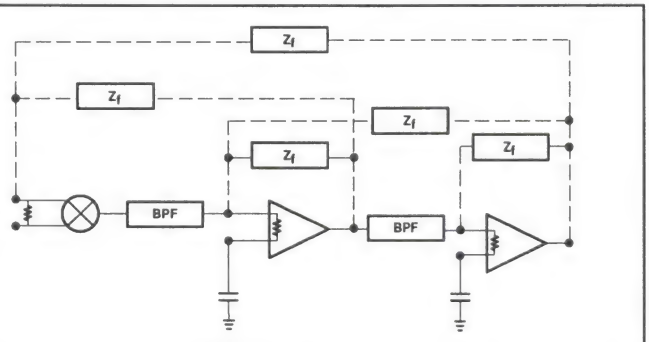
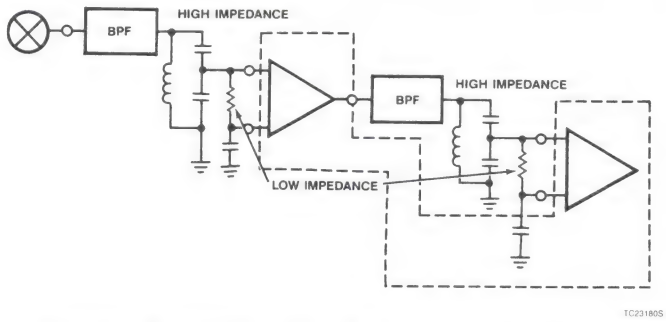


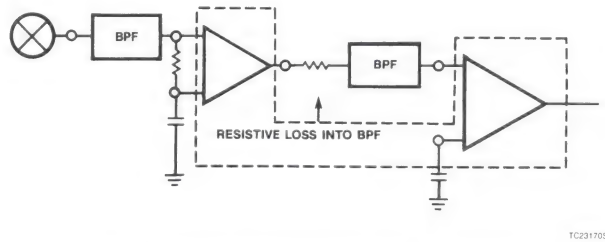

Figure 6. Feedback Paths

## Stability Considerations

The high gain and bandwidth of the 604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground,. 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1µF monolithic right




7a. Terminating High Impedance Filters with Transformation to Low Impedance




7b. Low Impedance Termination and Gain Reduction

**Figure 7. Practical Termination**

at the $V_{CC}$ pin, and a 6.8µF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz a 1µF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters t the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters.

The input filter is a crystal type for narrow–band selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

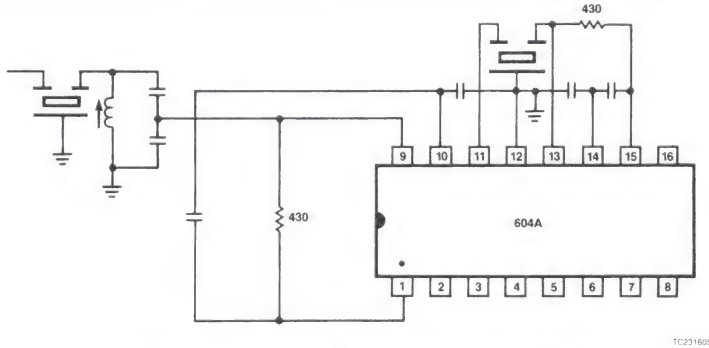



**Figure 8. Crystal Input Filter with Ceramic Interstage Filter**

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non–existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

## Quadrature Detector

Figure 5 shows an equivalent circuit of the 604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is differentially applied single ended to an external capacitor at Pin 9.

There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the nonlinearity of the curve increases (distortion), and with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first order effects only.

## Frequency discriminator design equations for 604A

$$V_O = \frac{C_S}{C_P + C_S} \bullet \qquad (1a)$$

$$\frac{1}{1 + \frac{\omega_1}{Q_1 S}\left(\frac{\omega_1}{S}\right)^2} \bullet \; V_{IN}$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L\,(C_p + C_S)}} \qquad (1b)$$

$$Q_1 = R\,(C_p + C_S)\;\omega_1 \qquad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across $C_S$ will be:

$$\phi = \angle V_O - \angle V_N = tg^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1-\left(\frac{\omega_1}{\omega}\right)^2}\right] \qquad (2)$$

Figure 10. Is the plot of $\phi$ vs $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of

$$\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}.$$

The signal $V_O$ would have a phase shift of

$$\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$$ with respect to the $V_{IN}$.

$$\text{If } V_{IN} = A \text{ Sin } \omega t \qquad (3)$$

$$\rightarrow V_O = A \text{ Sin } \left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \text{ Sin } \omega t \bullet \qquad (4)$$

$$\text{Sin } \left[\omega t + \frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right]$$

after low pass filtering

$$\rightarrow V_{OUT} = \frac{1}{2} A^2 \bullet \qquad (5)$$

$$\text{COS}\left[\frac{\pi}{2} - \left(\frac{2Q_1}{\omega_1}\right)\omega\right] = \frac{1}{2} A^2 \text{ Sin } \left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \left(\frac{\omega}{\omega_1}\right) = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \qquad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is the discriminated FM output.

NOTE: $\Delta\omega$ is the deviation frequency from the carrier $\omega_1$.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p.311. Example: At 455kHz IF, with ±5kHz FM deviation. The max/min normalized frequency will be

$$\frac{455 \pm 5\text{kHz}}{455} = 1.010 \text{ or } 0.990$$

Go to the $\phi$ vs. normalized frequency curves (Figure 10) and draw a vertical

straight line at $\left(\frac{\omega}{\omega_1}\right) = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discrimination FM signal. (Eq. 6)

→ Choose a Q = 20.

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174\text{pF}$ and $L = 0.7\text{mH}$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S$ = 10pF and $C_P$ = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S$ = 1pF is recommended.)

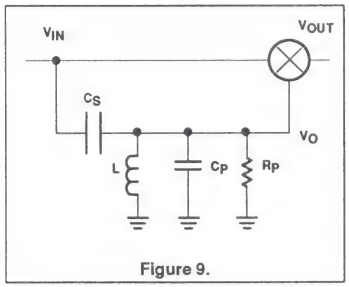



Figure 9.

## Audio Outputs

Two audio outputs are provided. Both are PNP current–to–voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. This response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Since the output structure is a current–to–voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two outputs differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no–signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be the logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

## RSSI

The Received Signal Strength Indicator, or RSSI, of the 604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indicator of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6Ω resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an inband signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 10kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current–to–voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

## Additional Circuitry

Internal to the 604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

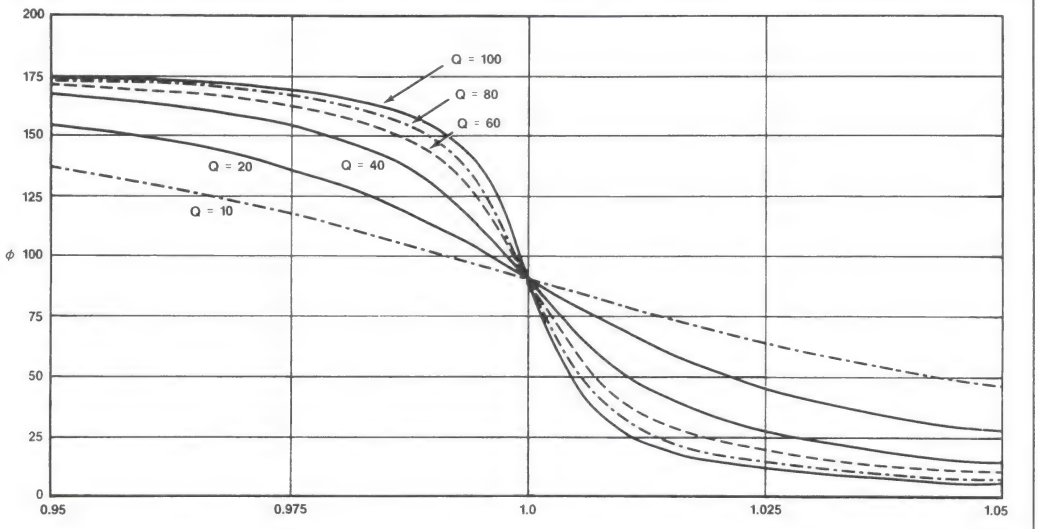



**Figure 10. Phase vs. Normalized IF Frequency**

# Signetics

# 605

## High-Performance Low-Power FM IF System

*Objective Specification*

**Military Communications and Industrial Products**

### DESCRIPTION

The 605 is a high-performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The 605 combines the functions of Signetics 602 and 604A, but features higher mixer input intercept, higher IF bandwidth (21MHz) and temperature compensated RSSI and limiters permitting higher performance application. The 605 is available in 20-lead dual-in-line 300mil–package.

### FEATURES

- **Low–Power consumption 5.7mA typical at 6V**
- **Mixer input to >500MHz**
- **Mixer conversion power gain of 13dB at 45MHz**
- **Mixer noise figure of 4.6dB at 45MHz**
- **XTAL oscillator effective to 150MHz (L.C. oscillator to GHz local oscillator can be injected)**
- **102dB of limiter gain**
- **21MHz limiter small signal bandwidth**
- **Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Two audio outputs – muted and unmuted**
- **Low external component count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz**
- **ESD hardened**

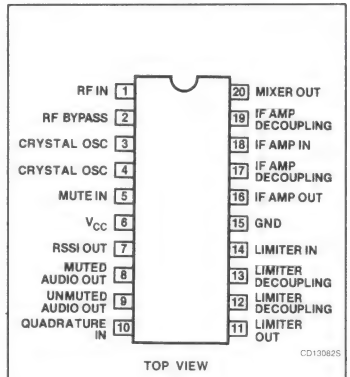
### APPLICATIONS

- **Cellular Radio FM IF**
- **High Performance communications receivers**
- **Single conversion VHF/UHF receivers**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **FSK and ASK data receivers**
- **Log amps**
- **Wideband low current amplification**

### ORDERING INFORMATION

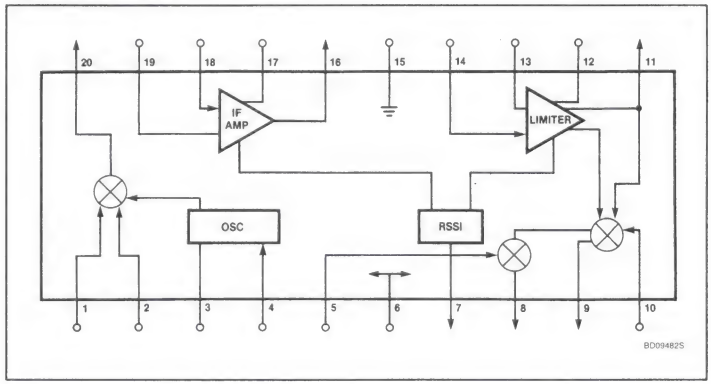
| DESCRIPTION | ORDER CODE |
|---|---|
| 20–Pin DIP | 605/BRA |

### PIN CONFIGURATION




TOP VIEW

### BLOCK DIAGRAM



# High–Performance Low–Power Mixer FM IF System 605

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Maximum operating voltage | 9 | V |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## AC ELECTRICAL CHARACTERISTICS

At –55°C to 125°C $V_{CC}$ = +6V, unless otherwise stated. IF frequency = 455kHz; IF level = –47dBm, FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C–message weighted filter and de–emphasis capacitor. Test Circuit Figure 1. The Parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Mixer/Osc section (ext LO = 300mV)** | | | | | | |
| $f_{IN}$ | Input signal frequency | | | 500 | | MHz |
| $f_{OSC}$ | Crystal oscillator frequency | | | 150 | | MHz |
| | Noise figure at 45MHz | | | 5.0 | | dB |
| | Third-order intercept point | f1 = 45.0; f2 = 45.06mHz | | –10 | | dBm |
| | Conversion power gain | Matched 14.5dBV step-up | 10 | 13 | 15 | dB |
| | | 50Ω source | | –1.7 | | dB |
| | RF input resistance | Single-ended input | 3.0 | 4.7 | | kΩ |
| | RF input capacitance | | | 3.5 | 4.0 | pF |
| | Mixer output resistance | (Pin 20) | 1.25 | 1.5 | | kΩ |
| **IF section** | | | | | | |
| | IF amp gain | 50Ω source | | 39.7 | | dB |
| | Limiter gain | 50Ω source | | 62.5 | | dB |
| | Input limiting –3dB, $r_{17}$ = 5.1k | Test at Pin 18 | | –113 | | dBm |
| | AM rejection | 80% AM 1kHz | 29 | 34 | 43 | dB |
| | Audio level, $R_{10}$ = 100K | 15nF de-emphasis | 80 | 175 | 260 | $mV_{RMS}$ |
| | Unmuted audio level, $R_{11}$ = 100k | 100pF de-emphasis | | 530 | | $mV_{RMS}$ |
| | SINAD sensitivity | RF level –118dB | | 16 | | dB |
| THD | Total harmonic distortion | | –34 | –42 | | dB |
| S/N | Signal-to-noise ratio | No modulation for noise | | 73 | | dB |
| | IF RSSI output, $R_9$ = 100k[1] | IF level = –118dBm | 0 | 160 | 650 | mV |
| | 1.5k input | IF level = –68dBm | 1.9 | 2.5 | 3.1 | V |
| | | IF level = –18dBm | 4.0 | 4.8 | 5.6 | V |
| | RSSI range | $R_9$ = 100kΩ Pin 16 | | 90 | | dB |
| | RSSI accuracy | $R_9$ = 100kΩ Pin 16 | | ±1.5 | | dB |
| | IF input impedance | | 1.40 | 1.6 | | kΩ |
| | IF output impedance | | 0.85 | 1.0 | | kΩ |
| | Limiter input impedance | | 1.40 | 1.6 | | kΩ |
| | Unmuted audio output resistance | | | 58 | | kΩ |
| | Muted audio output resistance | | | 58 | | kΩ |
| **RF/IF section (int LO)** | | | | | | |
| | Unmuted audio level | 4.5V = $V_{CC}$, RF level = –27dBm | | 480 | | $mV_{RMS}$ |
| | System RSSI output | 4.5V = $V_{CC}$, RF level = –27dBm | | 480 | | $mV_{RMS}$ |

**NOTE:**

1. 604A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.
   –118dBm
   –68dBm
   –18dBm
   The 605 and 604A are both derived from the same basic die. The 605 performance plots are directly applicable to the 604A.

# High–Performance Low–Power Mixer FM IF System



## CIRCUIT DESCRIPTION

The 605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dBV of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dBV of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5Ω source applications. The overall system is well–suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third order intercept of 10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations, either Harley or Colpitts. For crystal oscillators, the Colpitts configuration is used up to 150MHz.

The output of the mixer is internally loaded with a 1.5Ω resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5Ω. With most 455Hz ceramic filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dBV insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dBV insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC–coupled to a tuned quadrature network. This signal, which now has a 90% phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal atenuation with the mute activated is greater than 60dB. the mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

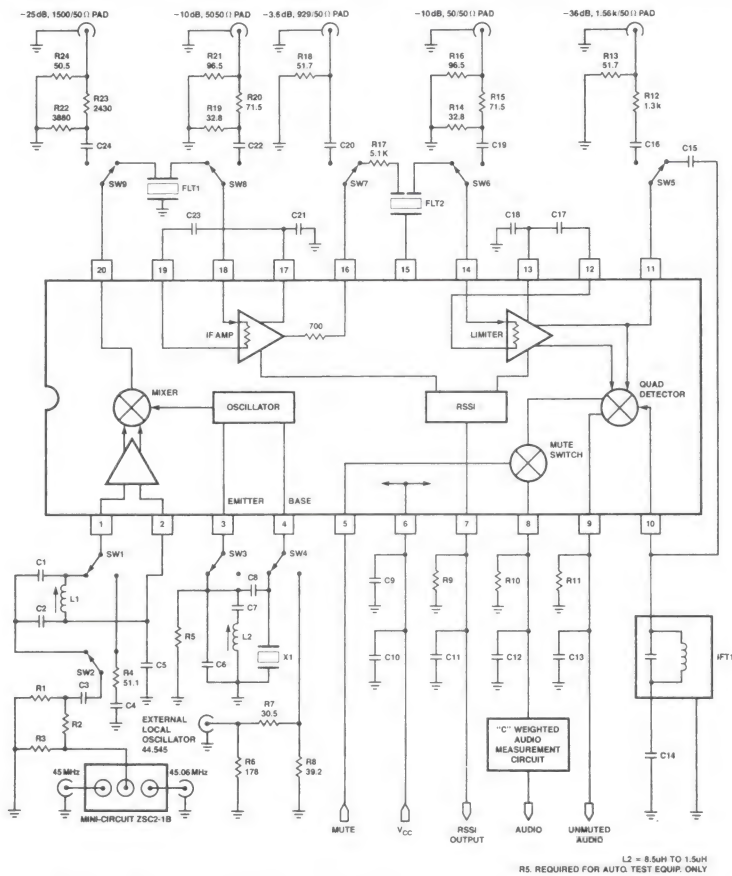



**Figure 1. 605 45MHz Test Circuit and Application Circuit (Relays as shown)**

## APPLICATION COMPONENT LIST

| | | | | | |
|---|---|---|---|---|---|
| C1 | 100pF NPO Ceramic | C14 | 100nF ±10% Monolithic Ceramic | L2 | 0.5-1.3uH, 800nH nominal |
| C2 | 390pF NPO Ceramic | C15 | 10pF NPO Ceramic | | Coilcraft UNI-10/143-16J12S |
| C5 | 100nF ±10% monolithic Ceramic | C17 | 100nF ±10% Monolithic Ceramic | | Coilcraft SLOTTEN-04-01 |
| C6 | 22pF NPO Ceramic | C18 | 100nF ±10% Monolithic Ceramic | | Toko 113KN-2K353HM |
| C7 | 1nF Ceramic | C21 | 100nF ±10% Monolithic Ceramic | X1 | 44.545MHz Crystal ICM4712701 |
| C8 | 5.6pF NPO Ceramic (minimum) | C23 | 100nF ±10% Monolithic Ceramic | R9 | 100k ±1% 1/4W Metal Film |
| C9 | 100nF ±10% Monolithic Ceramic | Flt1 | Ceramic Filter Murata SFG455A3 or equiv | R17 | 5.1k ±5% 1/4W Carbon Composition |
| C10 | 15uF Tantalum (minimum) | Flt2 | Ceramic Filter Murata SFG455A3 or equiv | R5 | Not Used in Application |
| C11 | 100nF ±10% Monolithic Ceramic | IFT1 | 455kHz (Ce = 180pF) RMC–2A6597H | R10 | 100k ±1% 1/4W Metal Film (optional) |
| C12 | 15nF ±10% Ceramic | L1 | 147-160nH Coilcraft UNI-10/142-04J08S | R11 | 100k ±1% 1/4W Metal Film (optional) |
| C13 | 150pF ±2% N1500 Ceramic | | | | |

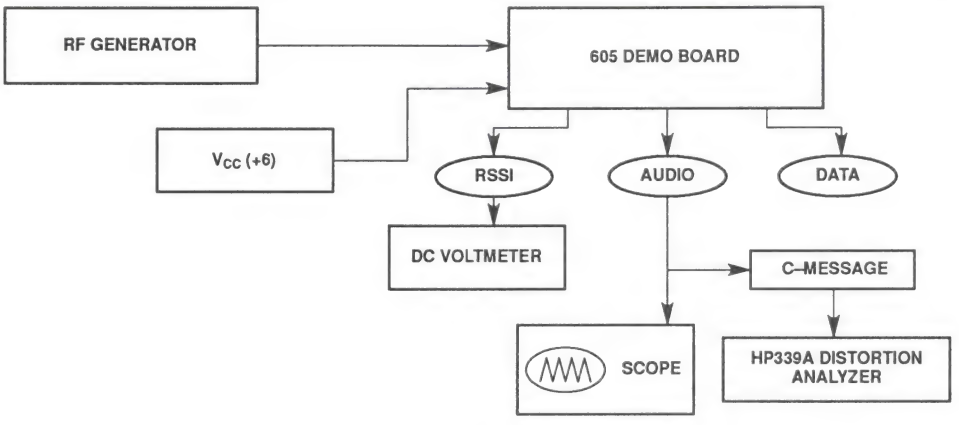



**Figure 2. 605 Application Circuit Set Up**

**NOTES:**

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz frequency deviation if you sue 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22µV or –120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and desigh. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case the receiver sensitivity will be bad.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10–15uF or higher value tantalum capacitor on the supply pin, and grounded near the 44.545 MHz oscillator improves sensitivity by 2–3dB.

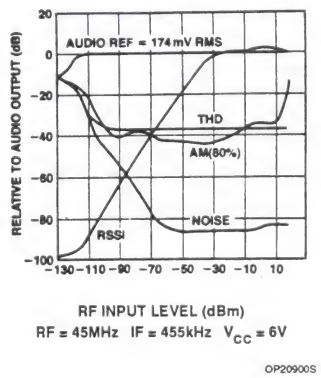



**Figure 3. 605 Application Board at 25°C**

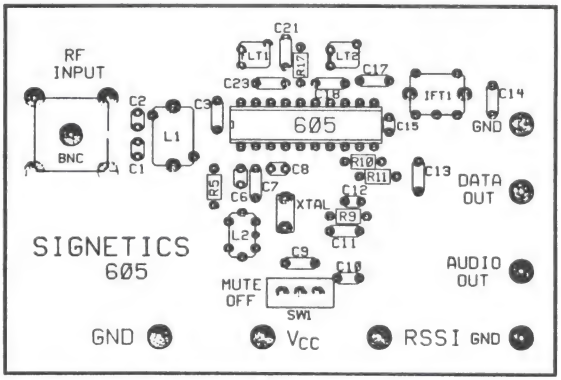



**Figure 4. Component Placement for 605 Application Circuit**

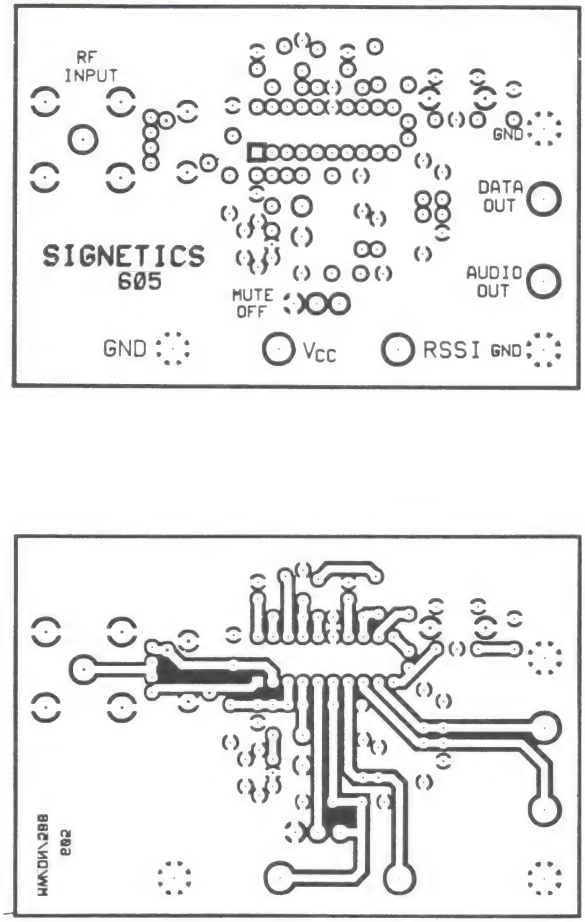



Figure 5. Layout for 605 Test and Application Board

# Signetics

# 5018

## 8-Bit μP-Compatible D/A Converter

*Product Specification*

**Military Linear Products**

## DESCRIPTION

The 5018 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

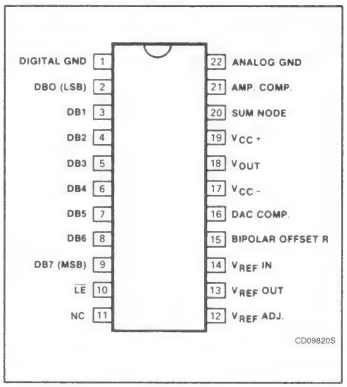
## FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to $\pm$ $^1/_2$ LSB (0.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 6800 and many other μPs

## APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

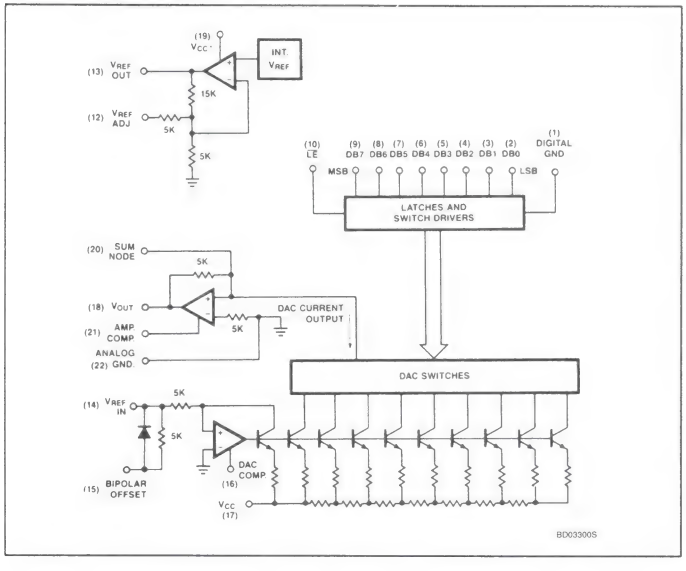
## PIN CONFIGURATION




## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 22-Pin Ceramic DIP | 5018/BWA |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_{CC}+$ | Positive supply voltage | 18 | V |
| $V_{CC}-$ | Negative supply voltage | -18 | V |
| $V_I$ | Logic input voltage | 0 to 18 | V |
| $V_{REF}IN$ | Voltage at $V_{REF}$ input | 12 | V |
| $V_{REF}ADJ$ | Voltage at $V_{REF}$ adjust | 0 to $V_{REF}$ | V |
| $V_{SUM}$ | Voltage at sum node | 12 | V |
| $I_{REFSC}$ | Short-circuit current to ground at $V_{REF}$ OUT | Continuous | |
| $I_{OUTSC}$ | Short-circuit current to ground or either supply at $V_{OUT}$ | Continuous | |
| $P_D$ | Power dissipation | 1000 | mW |

## DC ELECTRICAL CHARACTERISTICS $V_{CC}+ = +15V$, $V_{CC}- = -15V$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS[2] | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | Resolution | | 8 | 8 | 8 | 8 | | 8 | Bits |
| | Monotonicity | | 8 | 8 | 8 | 8 | | 8 | Bits |
| ΔFS | Relative accuracy | | | | ±0.19 | | | ±0.19 | %FS |
| $V_{CC}+$ | Positive supply voltage | | +11.4 | +15 | | +11.4 | +15 | | V |
| $V_{CC}-$ | Negative supply voltage | | -11.4 | -15 | | -11.4 | -15 | | V |
| $V_{IH}$ | Logic "1" input voltage | Pin 1 = GND | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | Logic "0" input voltage | Pin 1 = GND | | | 0.8 | | | 0.8 | V |
| $I_{IH}$ | Logic "1" input current | Pin 1 = GND, $2V < V_1 < 18V$ | | 0.1 | 10 | | | 10 | μA |
| $I_{IL}$ | Logic "0" input current | Pin 1 = GND, $-5V < v_1 < 0.8V$ | | -2.0 | -10 | | | -10 | μA |
| $V_{FS}$ | Full scale output voltage | Unipolar operation $V_{REF\ IN} = 5.000V$ | 9.50 | 9.961 | 10.50 | | | | V |
| $V_{FS}$ | Full scale output voltage | Bipolar operation | 4.5 | 4.961 | 5.5 | | | | V |
| | | $V_{REF\ IN} = 5.000V$ | -5.25 | -5.000 | -4.75 | | | | V |
| $V_{ZS}$ | Zero scale voltage | Bipolar operation | -30 | 5 | +30 | -30 | | +30 | mV |
| $I_{SC}$ | Output short circuit current | $V_O = 0V$ | | 15 | 40 | | | | mA |
| $PSR+_{(out)}$ | Output power supply rejection (+) | $V_{CC}- = -15V$, $13.5V \leq V_{CC}+ \leq 16.5V$ external $V_{REF\ IN} = 5.000V$ | | 0.001 | 0.01 | | | 0.01 | %FS/%VS |
| $PSR-_{(out)}$ | Output power supply rejection (-) | $V_{CC}+ = -15V$, $-13.5V \leq V_{CC}- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$ | | 0.001 | 0.01 | | | 0.01 | %FS/%VS |
| $TC_{FS}$ | Full scale temperature coefficient | $V_{REF\ IN} = 5.000V$ | | | | | 20 | | ppm/°C |
| $TC_{ZS}$ | Zero scale temperature coefficient | | | | | | 5 | | ppm/°C |
| $I_{REF}$ | Reference output current[9] | $V_{REF\ OUT} = 0V$ | | | 3 | | | | mA |
| $I_{REFSC}$ | Reference short circuit current | | | 15 | 30 | | | | mA |
| $PSR+_{(REF)}$ | Reference power supply rejection (+) | $V_{CC}- = -15V$ $13.5V \leq V_{CC}+ \leq 16.5V$, $I_{REF} = 1.0mA$ | | 0.003 | 0.01 | | | 0.01 | %FR/%VS |
| $PSR-_{(REF)}$ | Reference power supply rejection (-) | $V_{CC}+ = -15V$, $-13.5V \leq V_{CC}- \leq 16.5V$, $I_{REF} = 1.0\ mA$ | | 0.003 | 0.01 | | | 0.01 | %FR/%VS |
| $V_{REF}$ | Reference voltage | $I_{REF} = 1.0mA$ | 4.9 | 5.0 | 5.25 | | | | V |
| $\Delta Y_{REF}/\Delta T$ | Reference voltage temperature coefficient | $I_{REF} = 1.0mA$ | | | | | 60 | | ppm/°C |
| $Z_{IN}$ | DAC $V_{REF}$ IN input impedance | $I_{REF} = 1.0mA$ | 4.15 | 5.0 | 5.85 | | | | kΩ |
| $I_{CC}+$ | Positive supply current | $V_{CC}+ = 15V$ | | 7 | 14 | | | 14 | mA |
| $I_{CC}-$ | Negative supply current | $V_{CC}- = -15V$ | | -10 | -15 | | | -15 | mA |
| $P_D$ | Power dissipation | $I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$ | | 255 | 435 | | | 435 | mW |

## AC ELECTRICAL CHARACTERISTICS $V_{CC}+ = +15V$, $V_{CC}- = -15V$, unless otherwise specified.

| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = 55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{SLH}$ | Setting time[4] | $\pm 1/2$ LSB | Input | All bits low-to-high[3] | | 1.8 | | | | | μs |
| $t_{SHL}$ | Setting time[5] | $\pm 1/2$ LSB | Input | All bits high-to-low[4] | | 2.3 | | | | | μs |
| $t_{PLH}$ | Propagation delay[4] | Output | Input | All bits switched low-to-high | | 300 | | | | | ns |
| $t_{PHL}$ | Propagation delay[5] | Output | Input | All bits switched high-to-low | | 150 | | | | | ns |
| $t_{PLSB}$ | Propagation delay[4, 5] | Output | Input | 1 LSB change[3,4] | | 150 | | | | | ns |
| $t_{PLH}$ | Propagation delay[6] | Output | $\overline{CE}$ | low-to-high transition | | 300 | | | | | ns |
| $t_{PHL}$ | Propagation delay[7] | Output | $\overline{CE}$ | high-to-low transition | | 150 | | | | | ns |
| $t_S$ | Setup time[3, 8] | $\overline{CE}$ | Input | | 100 | | | | | | ns |
| $t_H$ | Hold time[3, 8] | Input | $\overline{CE}$ | | 50 | | | | | | ns |
| $t_{PW}$ | Latch enable pulse width[3, 8] | | | | 150 | | | | | | ns |

**NOTES:**
1. Operation beyond limits in the table may impair the useful life of the device.
2. Refer to Figure 2.
3. Refer to Figure 3.
4. See Figure 6.
5. See Figure 7.
6. See Figure 8.
7. See Figure 9.
8. See Figure 10.
9. For reference currents > 3mA, use of an external buffer is required.

## TEST CONFIGURATIONS AND WAVEFORM DEFINITIONS

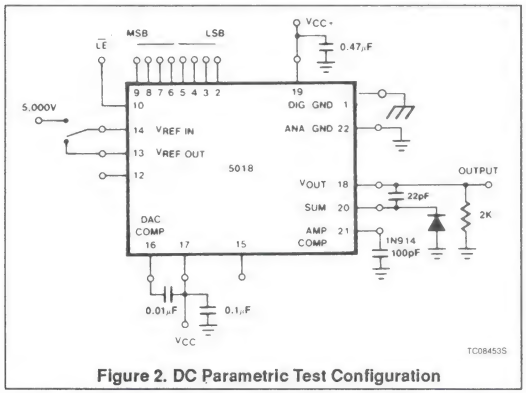



Figure 2. DC Parametric Test Configuration

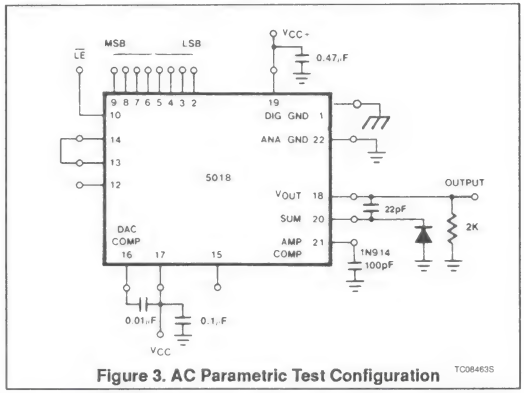



Figure 3. AC Parametric Test Configuration

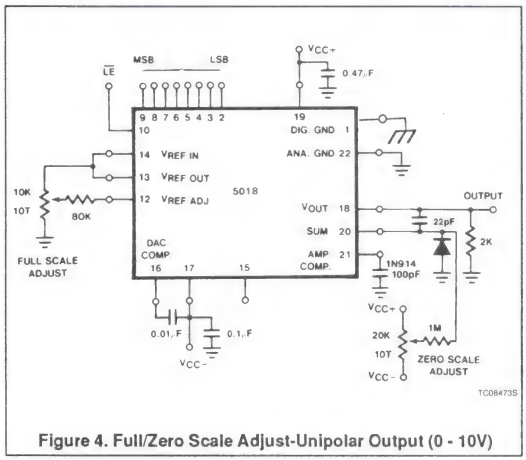



Figure 4. Full/Zero Scale Adjust-Unipolar Output (0 - 10V)

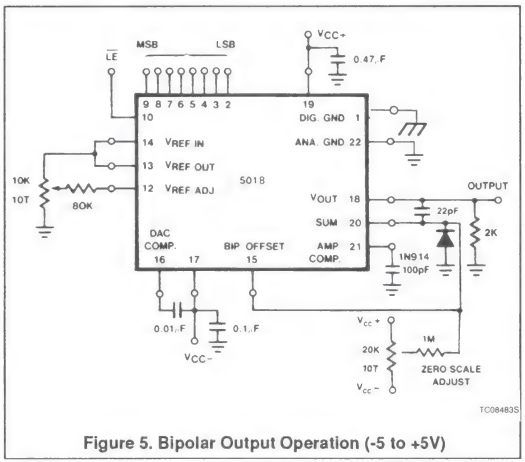



Figure 5. Bipolar Output Operation (-5 to +5V)

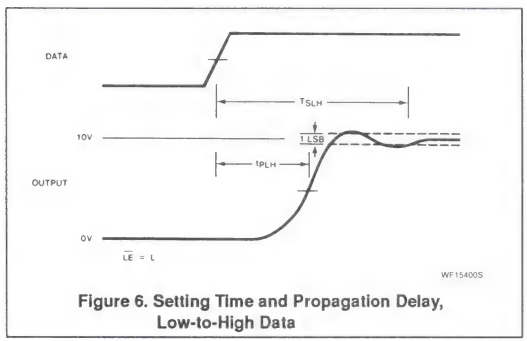



Figure 6. Setting Time and Propagation Delay, Low-to-High Data

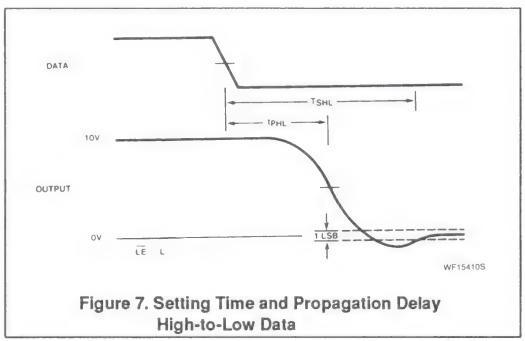



Figure 7. Setting Time and Propagation Delay High-to-Low Data

## TEST WAVEFORM DEFINITIONS

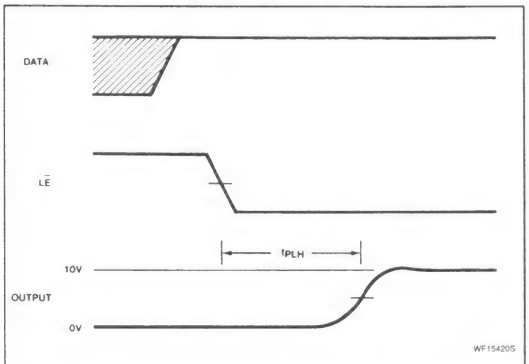



Figure 8. Propagation Delay, Latch Enable to Output

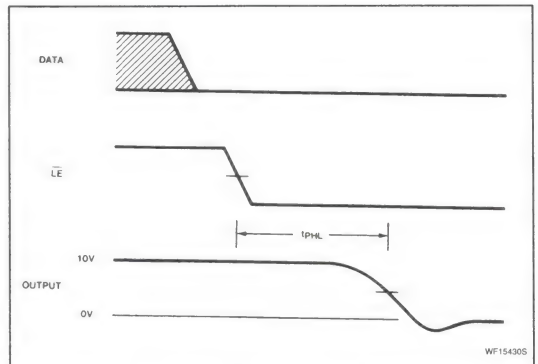



Figure 9. Propagation Delay, Latch Enable to Output

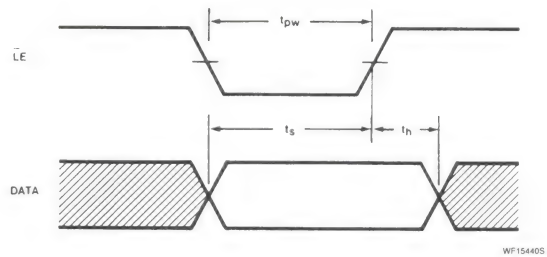



Figure 10. Latch Enable Pulse Width, Setup and Hold Times

# 5205

## Wideband High Frequency Amplifier

*Product Specification*

**Military Linear Products**

### DESCRIPTION

The 5205 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz. The 5205 operates with a single supply of 6V, and only draws 31mA of supply current which is much less than comparable hybrid parts. The noise figure is typically 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to fuse high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The 5205 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50Ω or 75Ω input and output impedances. The Standing Wave Rations in 50Ω and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 400MHz operating range.

No external components are needed other than AC coupling capacitors because the 5205 is internally compensated and matched to 50Ω and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz (typical values).

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional 5205's in series as required, without any degradation in amplifier stability.

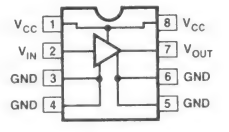
### FEATURES

- **650MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure $Z_O$ = 75Ω ($Z_O$ = 50Ω)**
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**

### APPLICATIONS

- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LANs**
- **Fiber optics**
- **Modems**
- **Mobile radio**
- **Telecommunications**

### PIN CONFIGURATION




TOP VIEW

CD12760S

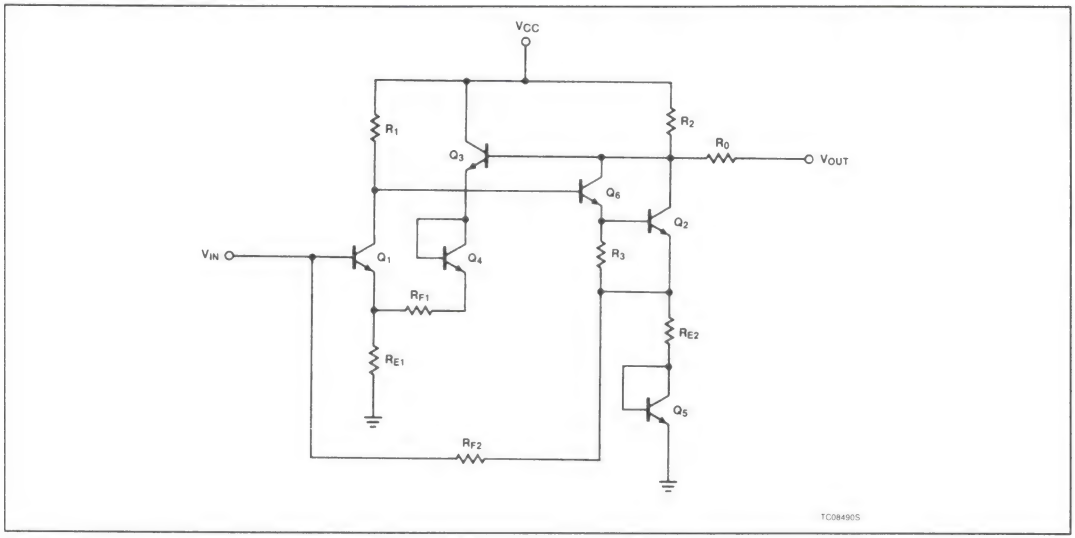
### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 8-Pin Ceramic DIP | 5205/BPA |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 9 | V |
| $V_I$ | AC input voltage | 5 | $V_{PP}$ |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## EQUIVALENT SCHEMATIC



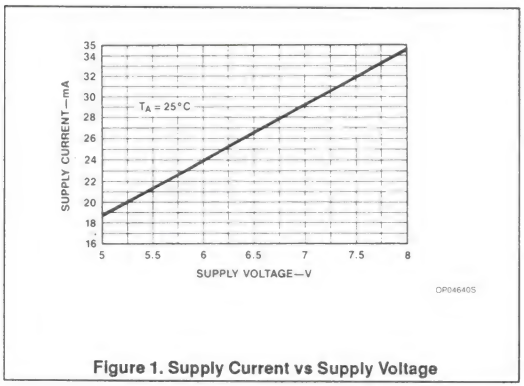




Figure 1. Supply Current vs Supply Voltage

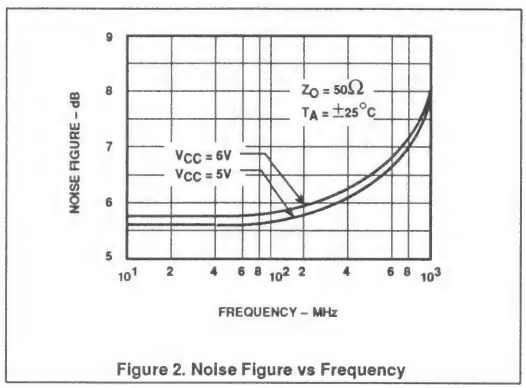



Figure 2. Noise Figure vs Frequency

# Wideband High Frequency Amplifier | 5205

## ELECTRICAL CHARACTERISTICS $V_{CC}$ = 6V, $Z_S = Z_L = Z_O = 50\Omega$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $I_{CC}$ | Supply current | $V_{CC}$ = 6.0V | 20 | 24 | 30 | 19 | | 31 | mA |
| $S_{21}$ | Insertion gain | f = 100MHz | 17 | 19 | 21 | 16.5 | | 21.5 | dB |
| $S_{11}$ | Input return loss[1, 2] | 1 to 400MHz | 12 | 29 | | | | | dB |
| $S_{11}$ | Input return loss[1] | 1 to 300MHz | | | | 9 | | | dB |
| $S_{22}$ | Output return loss[1, 2] | 1 to 400MHz | 12 | 27 | | | | | dB |
| $S_{22}$ | Output return loss[1] | 1 to 300MHz | | | | 9 | | | dB |
| $S_{12}$ | Isolation[1, 2] | 1 to 400MHz | –18 | –25 | | | | | dB |
| $S_{12}$ | Isolation[1] | 1 to 300MHz | | | | –18 | | | dB |
| $B_W$ | Bandwidth | ±0.5dB | | 300 | | | | | MHz |
| $B_W$ | Bandwidth | –3dB | 400 | 550 | | 300 | | | MHz |
| $E_N$ | Noise figure | f = 100MHz | | 4.8 | | | | | dB |
| $E_N$ | Noise figure | f = 100MHz | | 6.0 | | | | | dB |
| $P_{SAT}$ | Saturated output power | f = 100MHz | | +7.0 | | | | | dBm |
| $P_{SAT}$ | 1dB gain compression | f = 100MHz | | +4.0 | | | | | dBm |
| $IM_2$ | Second-order intermodulation intercept (output) | f = 100MHz | | +24 | | | | | dBm |
| $IM_3$ | Third–order intermodulation intercept (output) | f = 100MHz | | +17 | | | | | dBm |

**NOTES:**
1. This parameter/test condition is guaranteed but not tested.
2. Typical value is for 100MHz operation.

## THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wideband gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 3, the gain is set primarily by the equation:

$$\frac{V_O}{V_1} = (R_{F1} + R_{E1})/R_{E1} \quad (1)$$

which is series–shunt feedback. There is also shunt–series feedback due to $R_{F2}$ and $R_{E2}$ which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, $R_{E1}$ and the base resistance of $Q_1$ are kept as low as possible while $R_{F2}$ is maximized.

The noise figure is given by the following equation:

$$NF = 10 \text{ Log } \left\{1 + \frac{\left[r_B + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_0}\right\} 2qI_{C1} \text{ dB} \quad (2)$$

where $1_{C1}$ = 5.5mA, $R_{E1} = 12\Omega$, $r_B = 130\Omega$, KT/q = 26mV at 25°C and $R_O$ = 50 for a $50\Omega$ system and 75 for a $75\Omega$ system.

The DC input voltage level $V_1$ can be determined by the equation:

$$V_1 = V_{BE1} + (I_{C1} + IC3)R_{E1} \quad (3)$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3}$ = 7mA (currents rated at $V_{CC}$ = 6V).

Under the above conditions, $V_1$ is approximately equal to 1V.

Level shifting is achieved by emitter–follower $Q_3$ and diode $Q_4$ which provide shunt feedback to the emitter of $Q_1$ via $R_{F1}$. The use of an emitter–follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. the value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage $V_O$ can be determined by:

$$V_O = V_{CC} - (I_{C2} + I_{C6})\ R_2 \quad (4)$$

where $V_{CC}$ = 6V, $R_2 = 225\Omega$, $I_{C2}$ = 7mA and $I_{C6}$ = 5mA.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode $Q_5$ is included for bias purposes to allow direct coupling of $R_{F2}$ to the base of $Q_1$. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair ($Q_6$ and $Q_2$) which increases the DC bias voltage on the input stage ($Q_1$) to a more desirable value, and also increases the feedback loop gain. Resistor $R_0$ optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors $L_1$ and $L_2$ are bondwire and lead inductances which are roughly 3nH. These improve the high frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

## POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package. With this in mind, the following equation can be used to estimate the die temperature:

$$T_J = T_A + (P_D \times O_{JA})$$

where $T_A$ = Ambient Temperature, $T_J$ = Die Temperature, $P_D$ = Power Dissipation = $I_{CC}$ x $V_{CC}$, $O_{JA}$ = Package Thermal Resistance.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for $I_{CC}$ versus $V_{CC}$ curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air–mount specifications.

# Wideband High Frequency Amplifier 5205

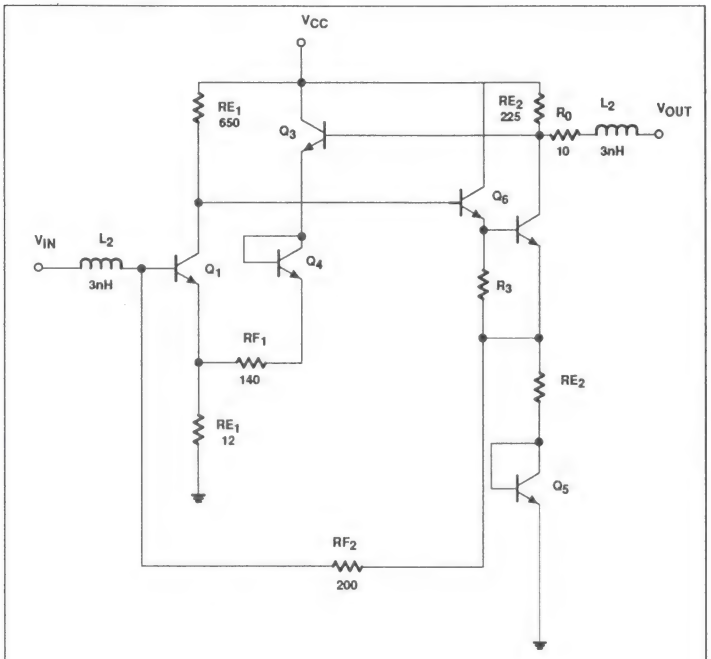



Figure 3. Schematic Diagram

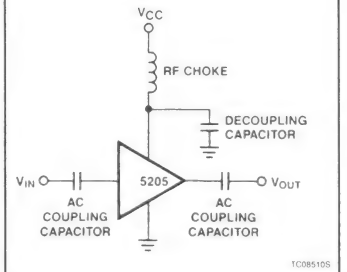



**Figure 4. Circuit Schematic for Coupling and Power Supply Decoupling**

## PC BOARD MOUNTING

In order to realize satisfactory mounting of the 5205 to a PC board, certain techniques need to be utilized. The board must be double–sided with copper and all pins must be soldered to their respective areas (i.e., all GND and $V_{CC}$ pins). The power supply should be decoupled with a capacitor as close to the $V_{CC}$ pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. there should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at $V_{CC}$ = 6V, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC Bias on the output of the amplifier will be loaded down causing loss of output power. This circuit is shown in Figure 4. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

The most important parameter is $S_{21}$. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_I = Z_O$ for the 5205

$$P_I = \frac{V_I^2}{Z_D} \quad \text{5205 } (Z_D) \quad P_O = \frac{V_O^2}{Z_D}$$

$$\frac{P_O}{P_I} = \frac{\frac{V_O^2}{Z_D}}{\frac{V_I^2}{Z_D}} = \frac{V_O^2}{V_I^2} = P_1$$

$P_I = V_I^2$

$P_I$ = Insertion Power Gain
$V_I$ = Insertion Voltage Gain

Measured value for the 5205 = $|S_{21}|^2 = 100$

$$P_I = \frac{P_o}{P_I} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_O}{V_I} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 6. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. these relationships are as follows:

INPUT RETURN LOSS = $S_{11}$ dB

$S_{11}$ dB = 20 Log $|S_{11}|$

OUTPUT RETURN LOSS = $S_{22}$ dB

$S_{22}$ dB = 20 Log $|S_{22}|$

$$\text{INPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leq 1.5$$

$$\text{OUTPUT VSWR} = \frac{|1 + S_{11}|}{|1 - S_{11}|} \leq 1.5$$

## 1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small–signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, and indication of the point of transition between small–signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

## INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. the intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. the relationship ratio is illustrated in Figure 7, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. these are expressed as:

$$IP_2 = P_O + IMR_2$$

$$IP_3 = P_O + IMR_3/2$$

where $P_O$ is the power level in dBm of each of a pair of equal level fundamental output signals, $IP_2$ and $IP_3$ are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operation range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure $IP_2$ and $IP_3$ at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the 5205 we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

## ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S–parameters, please refer to:

- **High–Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & sons, Inc.**
- **S–Parameter Techniques for Faster, More Accurate Network Design, H.P. App Note 95–1, Richard W. Anderson, 1967, HP Journal.**
- **S–Parameter Design, H.P. App Note 154, 1972.**

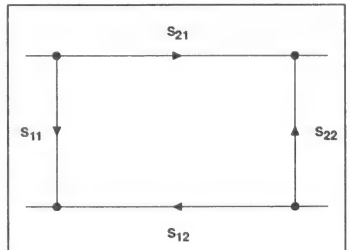
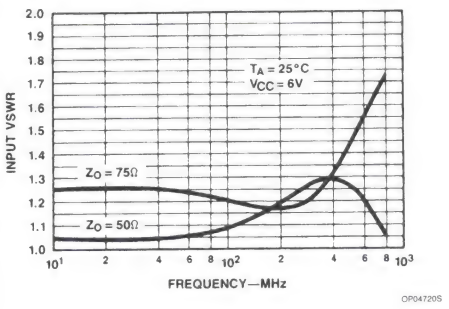
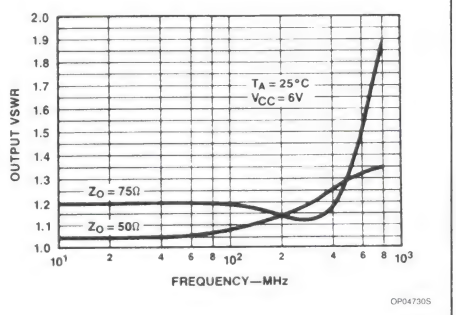



**Figure 5.**
**Two–Port Network Defined**




**a. Input VSWR vs Frequency**




**b. Output VSWR vs Frequency**

**Figure 6.**

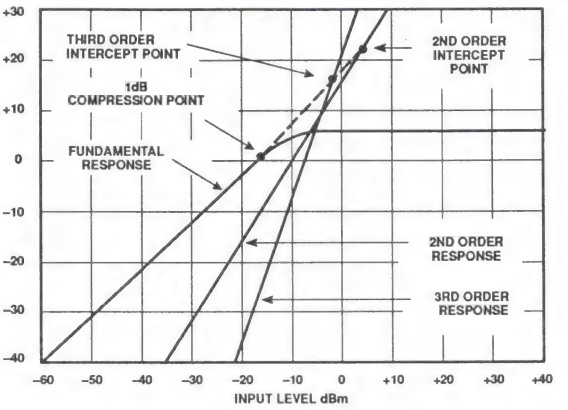



Figure 7. Output dBm vs Input dBm

Signetics

# 5212
## Transimpedance Amplifier

*Product Specification*

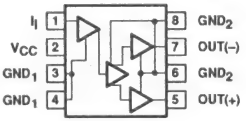
**Military Linear Products**

### DESCRIPTION
The 5212 is a wide band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber–optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block

### FEATURES
- **Extremely Low Noise**
- **Single 5V Supply**
- **Large Bandwidth Differential Outputs**
- **Low Input/Output Impedances**
- **High Power Supply Rejection Ratio**
- **14K OHM Differential Transresistance**

### APPLICATIONS
- **Fiber–Optic Receivers**
- **Wideband Gain Block**
- **General Purpose**
- **Instrumentation**
- **Sensor Preamplifiers**
- **Single–Ended to Differential Conversion**
- **Low Noise RF Amplifiers**

### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 8–Pin Ceramic DIP | 5212/BPA |

### ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Operating Ambient Temperature Range | –55 to + 125 | °C |
| $T_S$ | Operating Junction Temperature Range | –55 to +150 | °C |
| $T_{STG}$ | Storage Temperature Range | –65 to + 150 | °C |
| $V_{CC}$ | Power Supply | 6 | $V_{DC}$ |
| G–G | Ground Differential | None allowed, short 4 ground pins together | |

### RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Ambient Temperature | –55 to + 125 | °C |
| $T_S$ | Junction Temperature | –55 to +150 | °C |
| $V_{CC}$ | Supply Voltage | 4.5 to 5.5 | $V_{DC}$ |

### DC ELECTRICAL CHARACTERISTICS
Min. and Max. limits apply over operating temperature range at $V_{CC}$ =5V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| $V_I$ | Input bias voltage | $I_{IN} = 0$ | 0.55 | 0.8 | 1.05 | V |
| $V_O$ | Output bias voltage | $I_{IN} = I_{OUT} = 0$ | 2.5 | 3.3 | 3.8 | V |
| $V_{OS}$ | Output offset voltages | $I_{IN} = I_{OUT} = 0$ | | 0 | 120 | mA |
| $I_{CC}$ | Supply current | $I_{IN} = I_{OUT} = 0$ | 20 | 26 | 33 | mA |
| $I_{OMAX}$ | Output sink/source current | $\Delta V_{OUT} = \leq 100mV$ | 3 | 4 | | mA |
| $I_B$ | Maximum input current (2% linearity) | $I_O = 0$ | ±40 | ±80 | | µA |
| $I_{MAX}$ | Maximum input current overload threshold | | ±60 | ±120 | | µA |

# Transimpedance Amplifier 5212

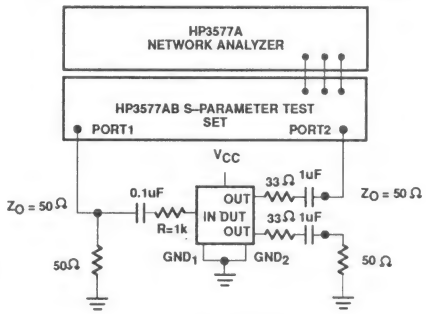
## AC ELECTRICAL CHARACTERISTICS[1] Min. and Max. limits apply over operating temperature range at $V_{CC}$ =5V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | |
| $R_T$ | Transresistance (Differential output) | Test Circuit 1 F = 10MHz, $R_L$=inf. | Note 5 | 9.0 | 14 | 19 | kΩ |
| $R_O$ | Output resistance (Differential output) | Test Circuit 1 F = 10MHz | Note 4 | 14 | 30 | 46 | Ω |
| $R_T$ | Transresistance (Single–ended output) | Test Circuit 1 F = 10MHz, $R_L$=inf. | Note 4 | 4.5 | 7 | 9.5 | kΩ |
| $R_O$ | Output resistance (Single–ended output) | Test circuit 1 F = 10MHz | Note 5 | 7 | 15 | 23 | Ω |
| $f_{3db}$ | Bandwidth (–3dB) | $T_A$=25°C | Note 4 | 100 | 120 | | MHz |
| $R_{IN}$ | Input resistance | | Note 4 | 70 | 110 | 150 | Ω |
| $C_{IN}$ | Input capacitance | | Note 4 | | 10 | 18 | pF |
| ΔR/ΔV | Transresistance power supply sensitivity | $\Delta V_{CC}$ = 5±0.5V | Note 4 | | 9.6 | | |
| ΔR/ΔT | Transresistance ambient temperature sensitivity | | | | 0.05 | | %/°C |
| $I_N$ | Input RMS noise current spectral density | Test Circuit 2 F = 10MHz | | | 2.5 | | pA $\sqrt{Hz}$ |
| $I_T$ | Input RMS noise current | Test Circuit 2 ΔF = 100MHz | | | 30 | | NA |
| PSRR | Power supply rejection ratio | Test Circuit 3 F = 0.1MHz | Note 2,3 | 20 | 33 | | dB |
| PSRR | Power supply rejection ratio (ECL configuration) | Test Circuit 4 F = 0.1MHz | Note 2,3 | | 23 | | dB |
| $V_{OMAX}$ | Max. output voltage swing differential | $R_L$ = ∞ | | 1.7 | 3.2 | | $V_{p-p}$ |
| $I_{PMAX}$ | Pulse distortion overload threshold | | | | ±300 | | μA |

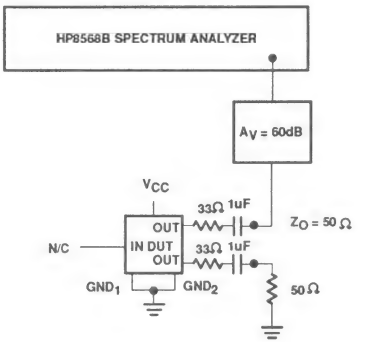
**NOTES:**
1. Typical data applies at $V_{CC}$ = 5V and $T_A$=25°C.
2. Circuit board layout dependent at higher frequencies. For best performance use RF filter in $V_{CC}$ lines.
3. Output referenced.
4. This parameter is guaranteed but not tested.
5. Due to test equipment limitation, actual tested conditions and/or limits may differ from those specified, however the specified test limits and conditions are guaranteed.

# Transimpedance Amplifier 5212

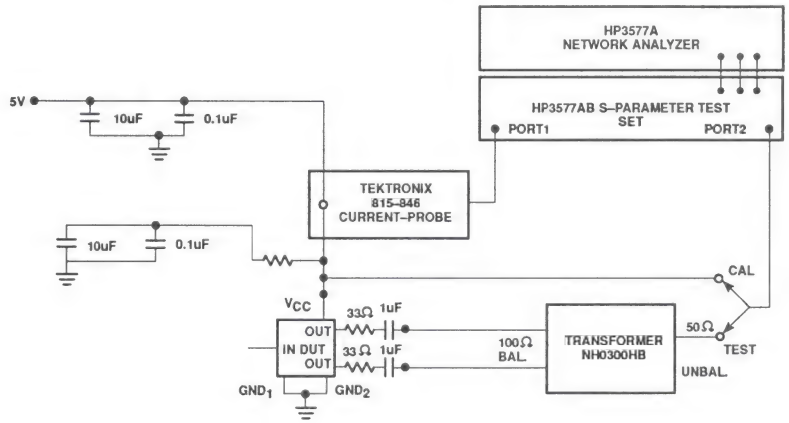
| SINGLE–ENDED | DIFFERENTIAL |
|---|---|
| $R_t = \frac{V_{OUT}}{V_{IN}} R = S21 = R$ | $R_t = \frac{V_{OUT}}{V_{IN}} R = S21 = R$ |
| $R_O = Z_O \left\| \frac{1 + S22}{1 - S22} \right\| -33$ | $R_O = 2Z_O \left\| \frac{1 + S22}{1 - S22} \right\| -33$ |



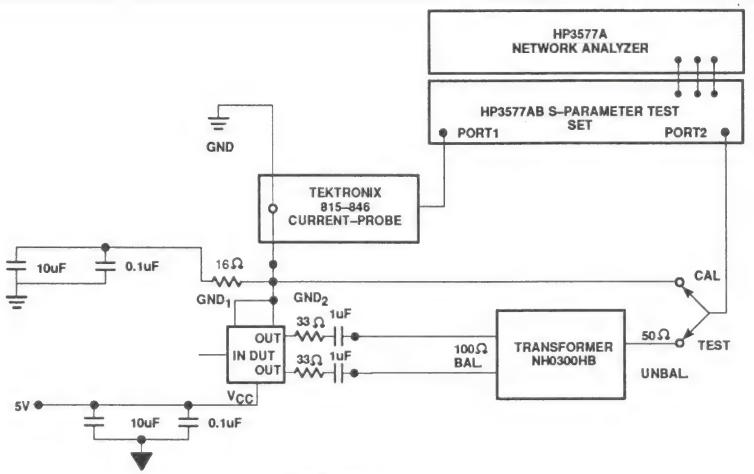

Test Circuit 1




Test Circuit 2




Test Circuit 3




Test Circuit 4

## DEFINITION OF TERMS

| Symbol | Name and Function |
|---|---|
| $V_I$ | **INPUT BIAS VOLTAGE:** The Input Bias Level test measures the quesent voltage on the input pin of the DUT, referenced to ground. |
| $V_O$ | **OUTPUT BIAS VOLTED:** The Output Bias Level tests measure the quesent voltage level of the OUT(–) and OUT(+) pins referenced to ground. |
| $V_{OS}$ | **OUTPUT OFFSET VOLTAGE:** The $V_{OS}$ test measures output offset voltage due to the mismatch of the output bias levels. A high impedance meter is connected across the two output pins and $V_{OS}$ is measured directly. |
| **Output Sink/Source Current** | |
| $I_{O\ MAX}$ | **ISOURCE:** The ISOURCE test measures the DUT's output capability of forcing current to a load. A 3mA load is applied to the DUT. The change in the output bias level, from no load to loaded, is measured. The input has no signal applied during this test. |
| $I_{O\ MAX}$ | **ISINK:** The ISINK test measures the DUT's output capability of sinking current from a load. A 3mA load is applied to the DUT. The change in the output bias level, from no load to loaded, is measured. the input has no signal applied during this test. |
| $I_B$ | **MAXIMUM INPUT CURRENT (2% Linearity):** The LINEARITY test measures the nonlinearity, of the transfer curve, of the DUT. Four points on the transfer curve of the DUT are measured. Specific DC currents forced at the input and the resulting output voltage is measured. The percent of nonlinearity is calculated as follows:<br>+Linearity(%) = {1 – ABS(R/T+)} X 100<br>–Linearity(%) = {1 – ABS(R/T–)} X 100<br>Where<br>R = (V4 – V6) / (I4 – I6)<br>T+ = (V3 – V5) / (I3 – I5)<br>T– = (V5 – V7) / (I5 – I7)<br>The forcing DC currents if $I_S = \pm 40\mu A$:<br>I1 = 130μA I7 = –30μA<br>I2 = 100μA I8 = –40μA<br>I3 = 60μA I9 = –60μA<br>I4 = 40μA I10 = –100μA<br>I5 = 30μA I11 = 130μA<br>I6 = 0μA |

## DEFINITION OF TERMS (Continued)

| | |
|---|---|
| $I_{MAX}$ | **INPUT OVERLOAD CURRENT THRESHOLD:** The input overload tests are used to guarantee that the knees of DUT's transfer curve are within spec. The ATE's meter is connected to the output pin being tested and ground; in the same manner as the OUTPUT BIAS test. The input is forced with a DC current. The output swing is then measured. This is done twice, once with 130μA and then with 80μA. The two readings are stored, and the results are calculated from the following:<br>INPUT OVERLOAD = $V_{OUT}$(120μA) – $V_{OUT}$(50μA)<br>if difference is greater than 50mV, the 50μA test point must be in the linear region. |
| $R_T$ | **TRANSRESISTANCE AT 10MHz:** The Transresistance test measures the single-ended, midband gain of the DUT at 10MHz. The network analyzer is set to measure S21 for the DUT. The actual value displayed is calculated as follows:<br>TRANSRESISTANCE = 2 X S21 X 1KΩ<br>INPUT SERIES RESISTANCE, R = 1KΩ |
| $R_o$ | **DIFFERENTIAL GAIN AT 10MHz (DIFFERENTIAL TRANSRESISTANCE):** This test calculates the total gain of the DUT at 10MHz. The value displayed is the sum of the single–ended tests. |
| $R_O$ | **ROUT:** the DC output resistance (ROUT) is calculated from the measurement in the ISOURCE test. The calculation is as follows:<br>ROUT = 3mA / ISOURCE measurement<br>the AC output resistance as specified is similar to measurement made with a Network Analyzer. |
| $f_{3db}$ | **3dB BANDWIDTH:** This test measures the –3dB bandwidth of the DUT relative to the midband gain. |
| $P_{SRR}$ | **PSRR:** The PSRR test measures the effect that a changing $V_{CC}$ has to $V_{OS}$ test. The $V_{CC}$[7] is changed with a small delta (+/– 0.1 V). The change in $V_{OS}$ is then measured. The two readings are stored and the PSRR results are calculated from the following:<br>PSRR = 20 X ABS(LOG(R))<br>WHERE<br>$R = \frac{V_{OS\ (VCC=5.1V)} - V_{OS(VCC=4.9V)}}{(0.20\ volts)}$ |
| $V_{OUT\ MAX}$ | **VOUT MAX:** The VOUT MAX test measures the DUT's maximum output swing. The ATE's meter is connected across the output of the DUT in the same manner as the $V_{OS}$ test. The input is forced with a DC current. The output swing is then measured. This is done twice, once with +130μA and then with –130μA. The two readings are stored. The VOUT MAX is calculated from the following:<br>$V_{OUT\ MAX} = V_{OUT(+130uA)} - V_{OUT(-130uA)}$ |
| $I_{PMAX}$ | **IPMAX:** An Bipolar Square wave of frequency = 1MHz is applied to the input, via a 1KΩ Resistor. The $I_p$ is the ± current where the output duty cycle deviates by 10% from that of the input duty cycle. |

Signetics

# 5512
## Dual High-Performance Operational Amplifier

*Product Specification*

**Military Communications and Industrial Products**

### DESCRIPTION

The 5512 series of high-performance operational amplifier provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector-to-emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability yet have low supply quiescent current.

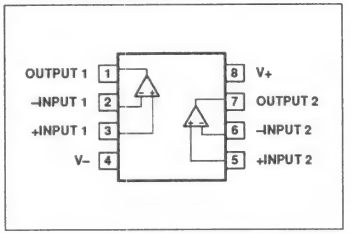
### APPLICATIONS

- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Battery operation
- Instrumentation amplifiers

### FEATURES

- Low input bias < ±20nA
- Low input offset current < ±20nA
- Low input offset voltage < 1mV
- Low $V_{OS}$ temperature drift 5μV/°C
- Low input bias temperature drift 40pA/°C
- Low input voltage noise $30nV/\sqrt{Hz}$
- Low supply current 1.5mA/amp
- High slew rate 1.0V/μs
- High CMRR 100dB
- High input impedance 100MΩ
- High PSRR 110dB
- High differential input voltage limit
- No cross-over distortion
- Indefinite output short-circuit protection
- Internally compensated for unity gain
- 600Ω drive capability

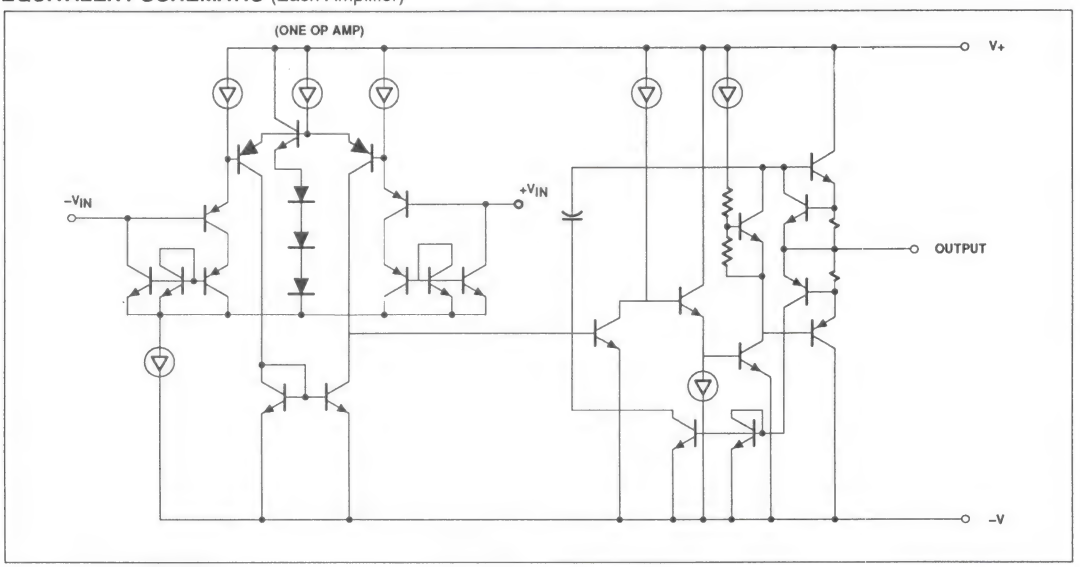
### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 8–Pin Ceramic DIP | 5512/BPA |

### EQUIVALENT SCHEMATIC (Each Amplifier)



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | ±16 | V |
| $P_D$ | Power dissipation | 500 | mW |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL PERFORMANCE CHARACTERISTICS

V+ = +15V, V– = –15V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IO}$ | Input offset voltage | $R_S$ = 50Ω | | 0.7 | 2.0 | | | 3.0 | mV |
| $I_{IO}$ | Input offset current | $R_S$ = 100kΩ | | 3.0 | 10.0 | | | 20.0 | nA |
| $I_{IB}$ | Input bias current | $R_S$ = 100kΩ | | 3.0 | 10.0 | | | 20.0 | nA |
| $R_I$ | Input resistance differential | | | 100.0 | | | | | MΩ |
| $V_{ICR}$ | Common mode voltage range | | ±13.5 | ±13.7 | | ±13.0 | | | V |
| CMRR | Input common–mode rejection ratio | $V_I$ = ±13.5V | 70.0 | 100.0 | | | | | dB |
| | | $V_I$ = ±13.0V | | | | 70.0 | | | dB |
| $A_V$ | Large–signal voltage gain | $R_L$ = 2kΩ, $V_O$ = ±10V | 50.0 | 200.0 | | 25.0 | | | V/mV |
| S.R. | Slew rate[2] | | 0.6 | 1.0 | | | | | V/μS |
| GBW | Small–signal unity gain bandwidth | | | 3.0 | | | | | MHz |
| $\theta_M$ | Phase margin | | | 45.0 | | | | | Degree |
| $V_O$ | Output voltage swing | $R_L$ = 2kΩ | ±13.0 | ±13.5 | | ±12.5 | | | V |
| $V_O$ | Output voltage swing | $R_L$ = 600Ω | ±10.0 | ±11.5 | | ±7.5 | | | V |
| $I_{CC}$ | Power supply current | | | 3.4 | 5.0 | | | 5.5 | mA |
| $P_{SRR}$ | Power supply rejection ratio | | 80.0 | 110.0 | | 80.0 | | | dB |
| CS | Amplifier to amplifier coupling | f = 1kHz to 20kHz | | –120.0 | | | | | dB |
| HD | Total harmonic distortion | f = 10kHz, $V_O$ = 7$V_{RMS}$ | | 0.01 | | | | | % |
| $E_N$ | Input noise voltage | f = 1kHz | | 30.0 | | | | | nV/√Hz |
| $I_N$ | Input noise current | f = 1kHz | | 0.2 | | | | | pA/√Hz |
| $I_{SC}$ | Output short–circuit current | | | 40 | | | | | mA |

**NOTE:**
1. Operation beyond the limit of this table may impair the useful life of this device.
2. This parameter is guaranteed, but not tested.

Signetics

Military Linear Products

# 5521
# LVDT Signal Conditioner

*Product Specification*

## DESCRIPTION

The 5521 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LDVTs) and Rotary Variable Differential Transformers (RVDTs). The chip includes a low distortion, amplitude–stable sine wave oscillator with programmable frequency to drive the primary of the LVDT/RVDT, a synchronous demodulator to convert the LVDT/RVDT output amplitude and phase to position information, and an output amplifier to provide amplification and filtering of the demodulated signal.

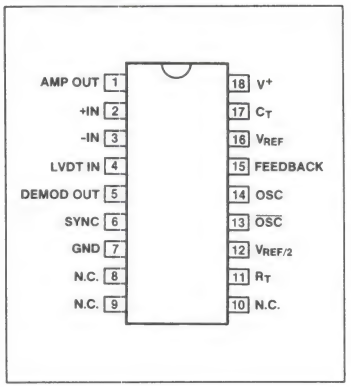
## FEATURES

- **Low distortion**
- **Single supply 5V to 20V, or dual supply ± 2.5V to ± 10V**
- **Oscillator frequency 1kHz to 20kHz**
- **Capable of ratiometric operation**
- **Low power consumption (182mV typ)**

## APPLICATIONS

- **LVDT signal conditioning**
- **RVDT signal conditioning**
- **LPDT signal conditioning**
- **Bridge circuits**

## PIN CONFIGURATION




## ORDERING INFORMATION

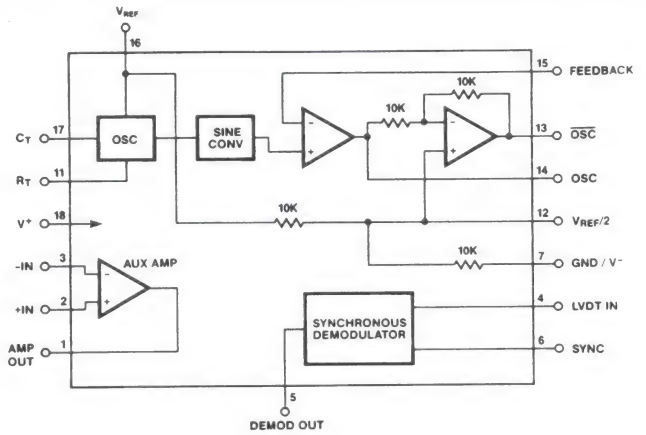
| DESCRIPTION | ORDER CODE |
|---|---|
| 18–Pin Ceramic DIP | 5521/BVA |

## PIN DEFINITIONS

| PIN NO. | SYMBOL | DEFINITION |
|---|---|---|
| 1 | Amp Out | Auxiliary Amplifier Output. |
| 2 | + IN | Auxiliary Amplifier non–inverting input. |
| 3 | – IN | Auxiliary Amplifier inverting input. |
| 4 | LVDT IN | Input to Synchronous Demodulator from the LVDT/RVDT secondary. |
| 5 | DEMOD OUT | Pulsating DC output from the Synchronous Demodulator output. This voltage should be filtered before use. |
| 6 | SYNC | Synchronizing input for the Synchronizing Demodulator. This input should be connected to the OSC or $\overline{OSC}$ output. Sync is referenced to $V_{REF}/2$. |
| 7 | GND | Device return. Should be connected to system ground or to the negative supply. |
| 8 | NC | No internal connection. |
| 9 | NC | No internal connection. |
| 10 | NC | No internal connection. |
| 11 | $R_T$ | Oscillator frequency-determining resistor. A temperature stable 18kΩ resistor should be connected between this pin and pin 7. |
| 12 | $V_{REF}/2$ | A high impedance source of one half the potential applied to $V_{REF}$ (pin 16). The LVDT/RVDT secondary return should be to this point. A bypass capacitor with low impedance at the oscillator frequency should also be connected between this pin and ground. |
| 13 | $\overline{OSC}$ | Oscillator sinewave output that is 180° out of phase with the OSC signal at pin 14. The LVDT/RVDT primary is usually connected between OSC and $\overline{OSC}$ pins. |
| 14 | OSC | Oscillator sinewave output. The LVDT/RVDT primaries are usually connected between OSC and $\overline{OSC}$ pins. |
| 15 | FEEDBACK | Usually connected to the OSC (pin 14) output for unity gain, a resistor between this pin and OSC, and one between this pin and ground can provide for a change in the oscillator output pin amplitudes. |
| 16 | $V_{REF}$ | Reference voltage input for the oscillator and sine converter. This voltage MUST be stable and must not exceed +V supply voltage. |
| 17 | $C_T$ | Oscillator frequency-determining capacitor. The capacitor connected between this pin and ground should be a temperature–stable type. |
| 18 | +V | Positive supply connection. |

# LVDT Signal | 5521

## BLOCK DIAGRAM




NOTE:
Pin numbers are for F, N packages.

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +20 | V |
| V+/V– | Split supply voltage | ±10 | V |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $P_D$ | Power dissipation | 840 | mW |

## DC ELECTRICAL CHARACTERISTICS $V+ = V_{REF} = 10V$, $R_T = 18k\Omega$, $C_T = 0.047\mu F$, Frequency ≈ 1kHz, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $I_T$ | Supply current | | | 12.9 | 18 | | | 18 | mA |
| $I_{REF}$ | Reference current | | | 5.3 | 8 | | | 8 | mA |
| $V_{REF}$ | Reference voltage range | | 5 | | V+ | 5 | | V+ | V |
| $P_D$ | Power dissipation | | | 182 | 260 | | | 260 | mW |
| **Oscillator Section** | | | | | | | | | |
| $V_{OSC}$ | Oscillator output | $R_L$ = 10k | | $\frac{V_{REF}}{8.8}$ | | | | | $V_{RMS}$ |
| $D_{IST}$ | Sineware distortion | No load | | 1.5 | | | | | % |
| $\Delta V_{OSC}$ | Initial amplitude error | | | 0.4 | | | | | % |
| $\Delta V_{OSC}/\Delta T$ | Temperature coeff. of amplitude | | | | | | 0.005 | | %/°C |
| $\Delta f_O$ | Init. accuracy of oscillator freq. | | | 0.9 | 5.0 | | | | % |
| $\Delta f_O/\Delta T$ | Temperature coeff. of frequency[2] | | | | | | 0.05 | | %/°C |
| $\Delta f/\Delta V$ | Voltage coeff. of frequency | | | 3.3 | | | | | %/ $V(V_{REF})$ |
| $R_L$ | Min OSC ($\overline{OSC}$) Load[3] | | 300 | 170 | | 300 | | | Ω |

## DC ELECTRICAL CHARACTERISTICS (Continued)

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **Demodulator Section** | | | | | | | | | |
| $\Delta L$ | Linearity error[4] | $5V_{P-P}$ input | | 0.05 | 0.1 | | | 0.1 | %FS |
| $V_{I\,(MAX)}$ | Maximum demodulator input | | | $\frac{V_{REF}}{2}$ | | | $\frac{V_{REF}}{2}$ | | $V_{P-P}$ |
| $V_{IO}$ | Demodulator offset voltage | | | 1.4 | 5.0 | | | 5.0 | mV |
| $\Delta V_{IO}/\Delta T$ | Demodulator offset voltage drift[4] | | | | | | | 25 | µV/°C |
| $I_{IB}$ | Demodulator input current | | | 234 | 500 | | | 500 | nA |
| $\Delta V_R/2$ | $V_R/2$ accuracy | | | 0.1 | 1.0 | | | 1.0 | % |
| **Auxiliary Output Amplifier** | | | | | | | | | |
| $V_{IO}$ | Input offset voltage | | | 0.5 | 5.0 | | | 5.0 | mV |
| $\Delta V_{IO}/\Delta T$ | Input offset voltage drift[4] | | | | | | | 25 | µV/°C |
| $I_{IB}$ | Input bias current | | | 210 | 500 | | | 500 | nA |
| $I_{IO}$ | Input offset current | | | 9 | 50 | | | 50 | nA |
| $A_V$ | Gain | | 100 | 385 | | 100 | | | V/mV |
| SR | Slew rate | | | 1.3 | | | | | V/µs |
| GBW | Unity gain bandwidth product | $A_V$ = 1 | | 1.6 | | | | | MHz |
| $V_O$ | Output voltage swing | $R_L$ = 10k | 7 | 8.2 | | 7 | | | V |
| $I_{SC}$ | Output short circuit current to ground or to $V_{CC}$ | | | 42 | 100 | | | | mA |

**NOTES:**
1. Operation beyond the limit of this table may impair the useful life of the device.
2. This is temperature coefficient of frequency for the device only. It is assumed that $C_T$ and $R_T$ are fixed in value and $C_T$ leakage is fixed over the operating temperature range.
3. Minimum lead impedence for which distortion is guaranteed to be less than 5%.
4. This parameter is guaranteed, but not tested.

# LVDT Signal 5521

## DEFINITION OF TERMS

| | |
|---|---|
| Oscillator Output | RMS value of the AC voltage available at the oscillator output pin. This output is referenced to $V_{REF}/2$ and is a function of $V_{REF}$. |
| Sine Wave Distortion | The Total Harmonic Distortion (THD) of the oscillator output with no load. This is not a critical specification in LVDT/RVDT systems. This figure could be 15% or more without affecting system performance. |
| Temperature Coefficient of Oscillator Amplitude | A measure of how the oscillator amplitude varies with ambient temperature as that temperature deviates from a 25°C ambient. |
| Temperature Coefficient of Oscillator Frequency | A measure of how the oscillator frequency varies with ambient temperature as that temperature deviates from a 25°C ambient. |
| Voltage Coefficient of Oscillator Frequency | The degree to which the oscillator frequency will vary as the reference voltage ($V_{REF}$) deviates from +10V. |
| Linearity Error | The degree to which the DC output of the demodulator/amplifier combination matches a change in the AC signal at the demodulator input. It is measured as the worst case nonlinearity from a straight line drawn between positive and negative full scale end points. |
| Maximum Demodulator Input | The maximum signal that can be applied to the demodulator input without exceeding the specified linearity error. |

## APPLICATION INFORMATION

$$\text{OSC frequency} = \frac{V_{REF}-1.3V}{V_{REF}(R_T + 1.5k)C_T}$$

Signetics

# 5532/5532A

## Internally Compensated Dual Low Noise Op Amp

*Product Specification*

**Military Linear Products**

### DESCRIPTION

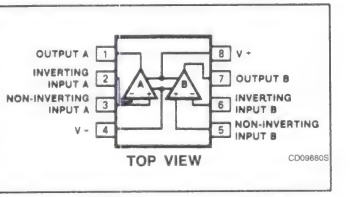
The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high-quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version, which has guaranteed noise voltage specifications, be used.

### FEATURES

- **Small–signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms)**
- **Input noise voltage: 5nV/√Hz (typical)**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew-rate: 9V/μs**
- **Large supply voltage range: ±3 to ± 20V**
- **Compensated for unity gain**

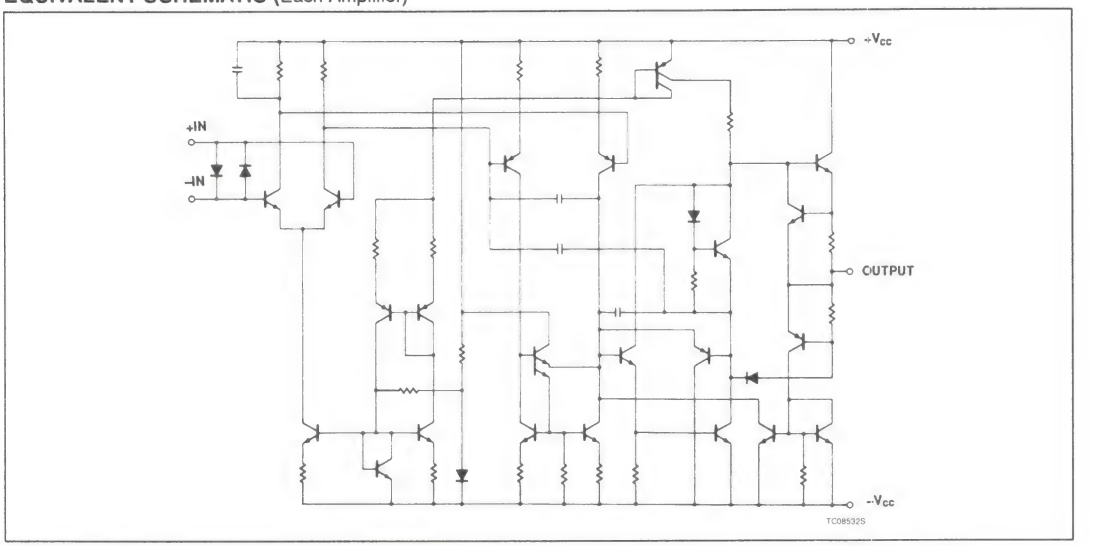
### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 8–Pin Ceramic DIP | 5532/BPA |
| 8–Pin Ceramic DIP | 5532A/BPA |

### EQUIVALENT SCHEMATIC (Each Amplifier)



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[2] | UNIT |
|---|---|---|---|
| $V_S$ | Supply voltage | ±22 | V |
| $V_I$ | Input voltage | ±V supply | V |
| $V_{DIFF}$ | Differential input voltage[1] | ±0.5 | V |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Junction temperature | 150 | °C |
| $P_D$ | Power dissipation | 1000 | mW |

## DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IO}$ | Input offset voltage | | | 0.5 | 2.0 | | | 3 | mV |
| $I_{IO}$ | Input offset current | | | | 100 | | | 200 | nA |
| $I_{IB}$ | Input bias current | | | 200 | 400 | | | 700 | nA |
| $V_{ICR}$ | Common mode voltage range | | ±12 | ±13 | | ±12 | | | V |
| CMRR | Common mode rejection ratio | | 80 | 100 | | 70 | | | dB |
| PSRR | Power supply rejection ratio | | | 10 | 50 | | | 100 | µV/V |
| $A_V$ | Large signal voltage gain | $R_L \geq 2k\Omega$, $V_O = \pm 10V$ | 50 | | | 25 | | | V/mV |
| | | $R_L \geq 600\Omega$, $V_O = \pm 10V$ | 40 | | | 20 | | | V/mV |
| $V_O$ | Output voltage swing | $R_L \geq 600\Omega$, $V_S = \pm 18V$ | ±15 | ±16 | | | | | V |
| | | $R_L \geq 2k\Omega$, $V_S = \pm 15V$ | ±12 | ±13 | | ±12 | | | V |
| $R_I$ | Input resistance | | 30 | 300 | | | | | kΩ |
| $I_{SC}$ | Output short–circuit current | | 10 | 38 | 60 | 5 | | 80 | mA |
| $I_{CC}$ | Supply current | | | | 13 | | | 13 | mA |

## AC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $R_{OUT}$ | Output resistance | $A_V$ = 30dB Closed loop<br>f = 10kHz, $R_L = 600\Omega$ | | 0.3 | | | | | Ω |
| OS | Overshoot | Voltage follower<br>$V_I = 100mV_{P-P}$<br>$C_L$ = 100pF, $R_L = 600\Omega$ | | 10 | | | | | % |
| $A_V$ | Gain | f = 10kHz | | 2.2 | | | | | V/mV |
| GBW | Gain bandwidth product | $C_L$ = 100pF, $R_L = 600\Omega$ | | 10 | | | | | MHz |
| SR | Slew rate | | | 9 | | | | | V/μs |
| PBW | Power bandwidth | $V_O = \pm 10V$<br>$V_O = \pm 14V$, $R_L = 600\Omega$<br>$V_{CC} = \pm 18V$ | | 140<br>100 | | | | | kHz<br>kHz |

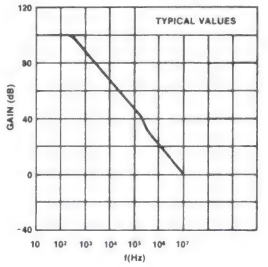
## ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $E_N$ | Input noise voltage[3] | $f_O$ = 30Hz<br>$f_O$ = 1kHz | | 8<br>5 | 12<br>6 | | | | $nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$ |
| $I_N$ | Input noise current | $f_O$ = 30Hz<br>$f_O$ = 1kHz | | 2.7<br>0.7 | | | | | $pA/\sqrt{Hz}$<br>$pA/\sqrt{Hz}$ |
| CS | Channel separation | f = 1kHz, RS = 5kΩ | | 110 | | | | | dB |

**NOTES:**
1. Diodes protect the inputs against over–voltage. Therefore, unless current–limiting resistors are used, large currents will flow if the different input voltage exceeds 0.6V. Maximum current should be limited to ± 10mA.
2. Operations beyond the limits of this table may impair the useful life of the device.
3. Input noise voltage is guaranteed for the 5532A only.

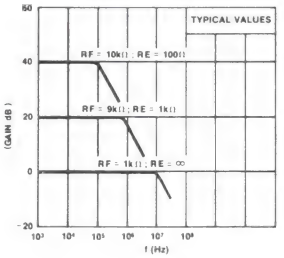
## TYPICAL PERFORMANCE CHARACTERISTICS

### Open-Loop Frequency Response



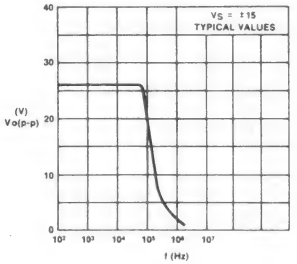

OP04870S

### Closed-Loop Frequency Response



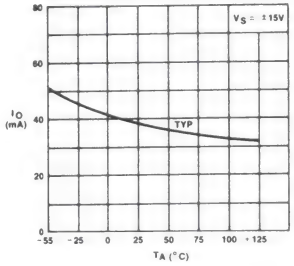

OPT4880S

### Large-Signal Frequency Response



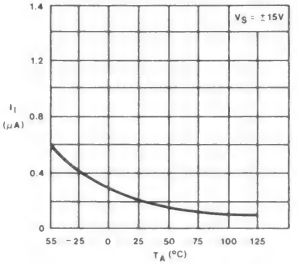

OPT4890S

### Output Short-Circuit Current



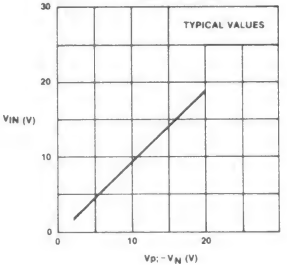

OP04900S

### Input Bias Current



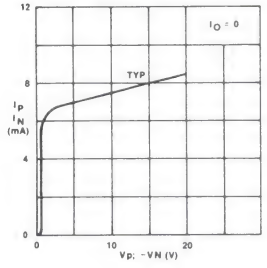

OP04910S

### Input Common-Mode Voltage Range



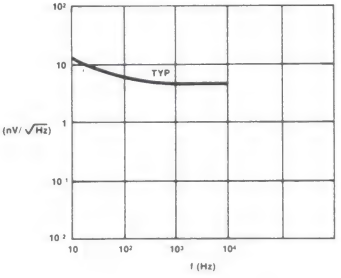

OP04920S

### Supply Current



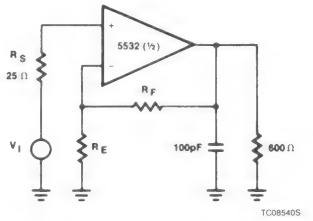

OP04930S

### Input Noise Voltage Density

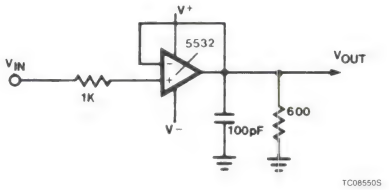



OP04940S

## TYPICAL TEST CIRCUITS




Closed-Loop Frequency Response




Voltage-Follower

Signetics

# 5534/5534A
## Low-Noise Op Amps

*Product Specification*

**Military Linear Products**

### DESCRIPTION

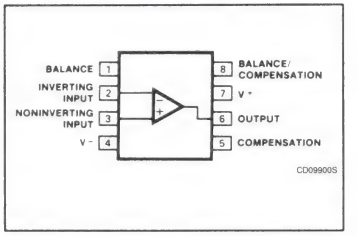
The 5534 is a high-performance low-noise operational amplifier. Compared to other operational amplifiers, such as TL083, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

The op amps are internally compensated for again equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.). If very low noise is of prime importance, it is recommended that the 5534A version be used which has guaranteed noise specifications.

### FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, $10V_{RMS}$ at $V_S = \pm 18V$**
- **Input noise voltage: $4nV/\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew rate: 13V/μs**
- **Large supply voltage range: ±3 to ±20V**

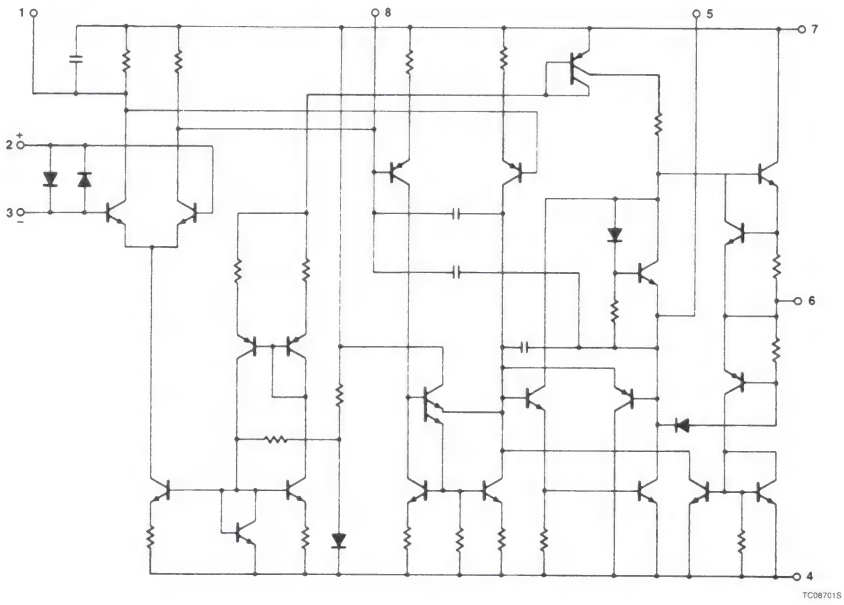
### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 8–Pin Ceramic DIP | 5534/BCA |
| 8–Pin Ceramic DIP | 5534A/BCA |

### EQUIVALENT SCHEMATIC



## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[2] | UNIT |
|---|---|---|---|
| $V_S$ | Supply voltage | ±22 | V |
| $V_{IN}$ | Input voltage | ± V supply | V |
| $V_{DIFF}$ | Differential input voltage[1] | ±0.5 | V |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Junction temperature | 150 | °C |
| $P_D$ | Power dissipation at 25 °C | 800 | mW |

## DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IO}$ | Input offset voltage | | | 0.5 | 2.0 | | | 3 | mV |
| $I_{IO}$ | Input offset current | | | 10 | 200 | | | 500 | nA |
| $I_{IB}$ | Input bias current | | | 400 | 800 | | | 1500 | nA |
| $V_{ICR}$<br>CMRR<br>PSRR | Common mode voltage range<br>Input mode rejection ratio<br>Power supply rejection ratio | $R_S = 10k\Omega$ | <br>±12<br>80 | ±13<br>100<br>10 | <br><br>50 | <br>±12<br>70 | | <br><br>100 | V<br>dB<br>µV/V |
| $A_V$ | Large signal voltage gain | $R_L \geq 600\Omega$, $V_O = \pm 10V$ | 50 | 100 | | 25 | | | V/mV |
| $V_O$ | Output voltage swing | $R_L \geq 600\Omega$,<br>$R_L \geq 600\Omega$, $V_S = \pm 18V$<br>$R_L \geq 2k\Omega$, $V_S = \pm 15V$ | ±12<br>±15<br>±13 | ±13<br>±16<br>±13.5 | | ±10<br><br>±12 | | | V<br>V<br>V |
| $R_I$ | Input resistance[3] | | 50 | 100 | | | | | kΩ |
| $I_{SC}$ | Output short–circuit current | | | 38 | | | | | mA |
| $I_{CC}$ | Supply current | | | 4 | 6.5 | | | 9 | mA |

## AC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $R_{OUT}$ | Output resistance | $A_V$ = 30dB closed loop<br>f = 10kHz, $R_L = 600\Omega$<br>$C_C$ = 22pF | | 0.3 | | | | | Ω |
| $t_r$<br>OS | Transient response<br>Rise time<br>Overshoot | Voltage follower,<br>$R_L = 600\Omega$, $C_C$ = 22pF,<br>$C_L$ = 100pF, $V_I$ = 50mV | | <br>20<br>20 | | | | | <br>ns<br>% |
| $t_r$<br>OS | Transient response<br>Rise time<br>Overshoot | <br>$V_{IN}$ = 50mv, $R_L = 600\Omega$<br>$C_C$ = 47pF, $C_L$ = 500pF | | <br>50<br>35 | | | | | <br>ns<br>% |
| AC | Gain | f = 10kHz, $C_C$ = 0<br>f = 10kHz, $C_C$ = 22pF | | 6<br>2.2 | | | | | V/mV<br>V/mV |
| GBW | Gain bandwidth product | $C_C$ = 22pF, $C_L$ – 100pF | | 10 | | | | | mHz |
| SR | Slew rate[3] | $C_C$ = 0<br>$C_C$ = 22pF | <br>4 | 13<br>6 | | | | | VμS<br>V/mus |
| PBW | Power bandwidth | $V_{OUT} = \pm 10V$, $C_C$ = 0<br>$V_{OUT} = \pm 10V$, $C_C$ = 22pF<br>$V_{OUT} = \pm 14V$, $R_L = 600\Omega$<br>$C_C$ = 22pF, $V_{CC} = \pm 18V$ | | 200<br>95<br>70 | | | | | kHz<br>kHz<br>kHz |

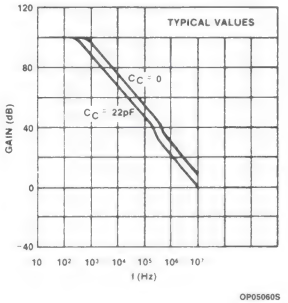
## ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S \pm 15V$, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | 5533/5534 | | | 5533A/5534A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $E_N$ | Input noise voltage | $f_O$ = 30Hz<br>$f_O$ = 1kHz | | 7<br>4 | | | 5.5<br>3.5 | 7<br>4.5 | $nV/\sqrt{Hz}$<br>$nV/\sqrt{Hz}$ |
| $I_N$ | Input noise current | $f_O$ = 30Hz<br>$f_O$ = 1kHz | | 2.5<br>0.6 | | | 1.5<br>0.4 | | $pA/\sqrt{Hz}$<br>$pA/\sqrt{Hz}$ |
| $BB_N$ | Broadband noise figure | f = 10Hz – 20kHz,<br>$R_S = 5k\Omega$ | | | | | 0.9 | | dB |
| CS | Channel separation | f = 1kHz, $R_S = 5k\Omega$ | | 110 | | | 110 | | dB |

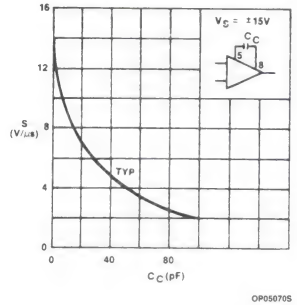
**NOTES:**
1. Diodes protect the inputs against over–voltage. Therefore, unless current–limiting resistors are used, large currents will flow if the different input voltage exceeds 0.6V. Maximum current should be limited to ± 10mA.
2. Operations beyond the limits of this table may impair the useful life of the device.
3. This parameter is guaranteed but not tested.

## TYPICAL PERFORMANCE CHARACTERISTICS

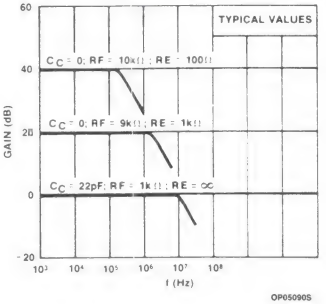
### Open-Loop Frequency Response



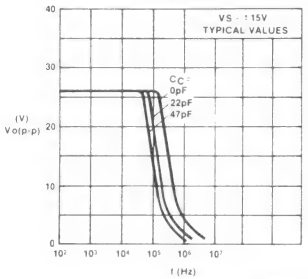

### Slew Rate as a Function of Compensation Capacitance



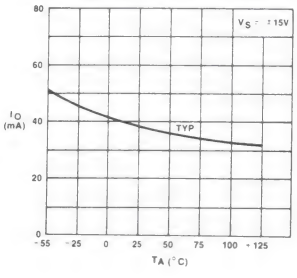

### Closed-Loop Frequency Response



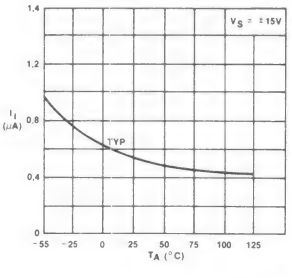

### Large-Signal Frequency Response



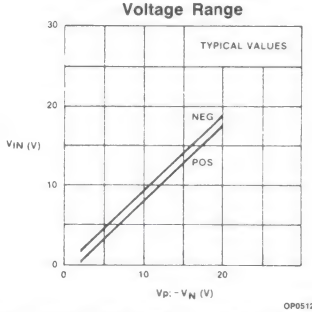

### Output Short-Circuit Current



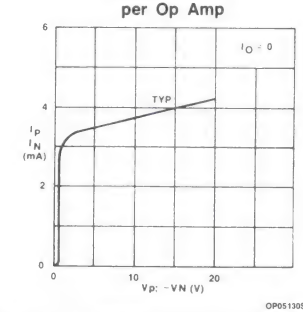

### Input Bias Current



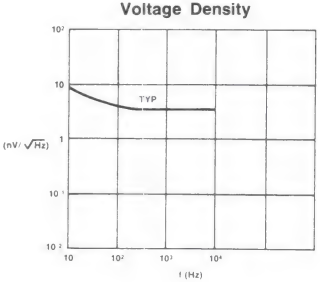

### Input Common-Mode Voltage Range



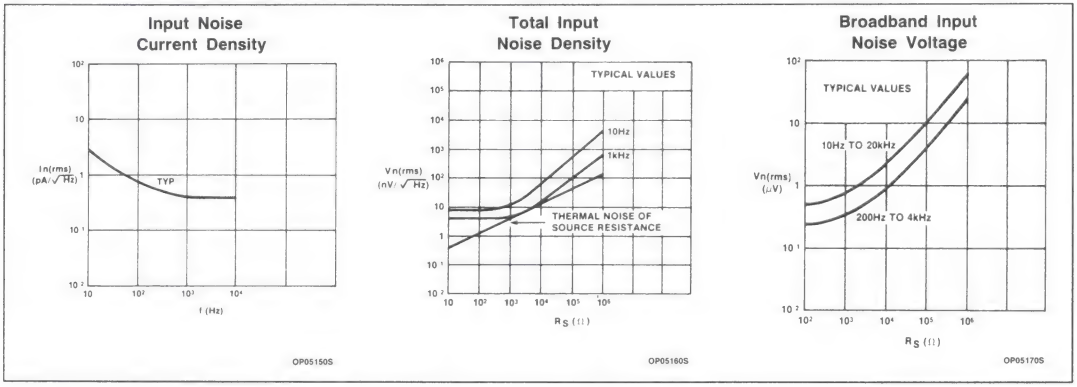

### Supply Current per Op Amp



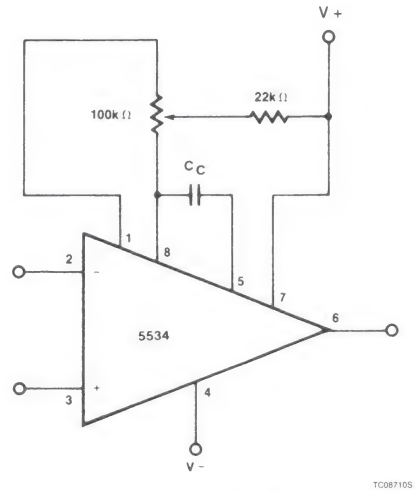

### Input Noise Voltage Density



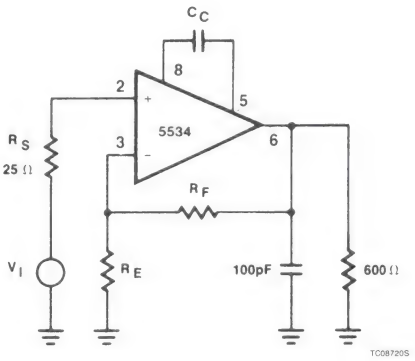
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)




## TEST LOAD CIRCUITS

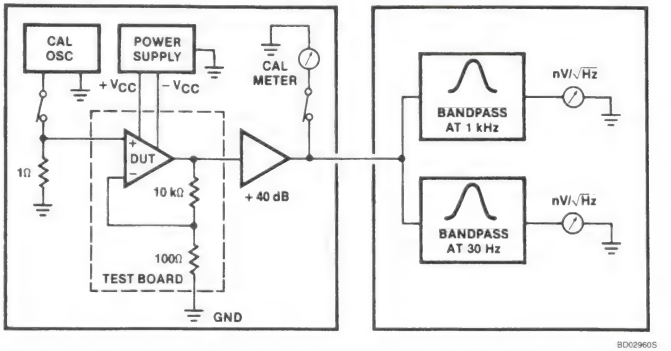



Frequency Compensation and Offset Voltage Adjustment Circuit




Closed-Loop Frequency Response

## NOISE TEST BLOCK DIAGRAM



Signetics

# 5537
## Sample-and-Hold Amplifier

*Product Specification*

**Military Linear Products**

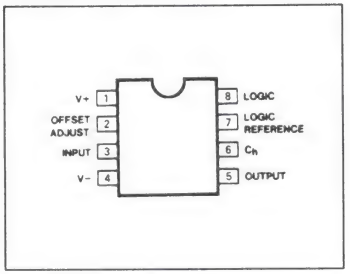
### DESCRIPTION

The 5537 monolithic sample-and-hold amplifier combines the best features of ion-implanted JFET's with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the sample mode. The first amplifier has bipolar input transistors which give the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the 5537 a low droop rate at higher temperature. the output stage has the capability to drive a 2kΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the sample mode occurring when the logic input is high.

### FEATURES

- **Operates from ±5V to ±18V supplies**
- **Hold leakage current 6pA @ $T_J$ = 25°C**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at $C_H$ = 0.01μF**
- **Low input offset: 1MV (typical)**
- **0.002% gain accuracy with $R_L$ = 2kΩ**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in samples or hold**
- **Wide bandwidth**

### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 8-Pin Ceramic DIP | 5537/BPA |

### BLOCK DIAGRAM

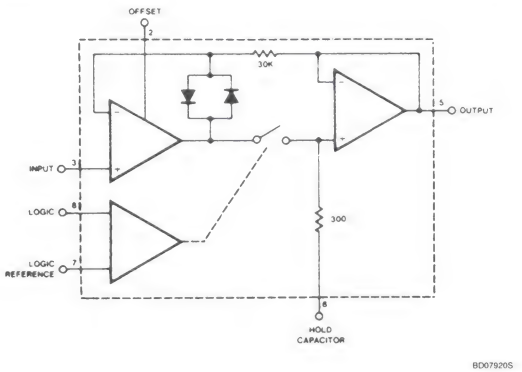



Figure 1

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_S$ | Voltage Supply | ±18 | V |
| $P_D$ | Power dissipation (package limitation)[1] | 500 | mW |
| $T_A$ | Operating ambient temperature range | –55 to +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_{IN}$ | Input voltage | Equal to supply voltage | |
| | Logic to logic reference differential voltage[2] | +7, –30 | V |
| | Output short circuit duration | Indefinite | |
| | Hold capacitor short circuit duration | 10 | s |
| $T_{SOLD}$ | Lead soldering temperature (10sec max) | 300 | °C |

## DC ELECTRICAL CHARACTERISTICS[3]

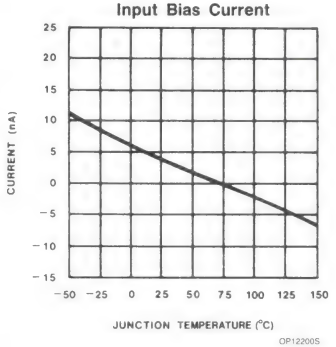
| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IO}$ | Input offset voltage[5] | | | 1 | 3 | | | 5 | mV |
| $I_{IB}$ | Input bias current[5] | | | 5 | 25 | | | 75 | nA |
| $R_{IN}$ | Input impedance | | | $10^{10}$ | | | | | Ω |
| | Gain error | $-10V \leq V_{IN} \leq 10V$, $R_L = 2k\Omega$ | | 0.002 | 0.007 | | | 0.01 | % |
| | | $-11.5V \leq V_{IN} \leq 11.5V$, $R_L = 10k\Omega$ | | | 0.007 | | | 0.01 | % |
| | Feedthrough attenuation ratio | $C_H = 0.01\mu F$ | 86 | 96 | | | | | dB |
| $R_{OUT}$ | Output impedance | "HOLD mode" | | 0.5 | 2 | | | 4 | Ω |
| | "HOLD" Step[4] | $C_H = 0.01\mu F$<br>$V_{OUT} = 0$ | | 0.5 | 2.0 | | | | mV |
| $I_{CC}$ | Supply current | $V_S = \pm 18V$ | | 4.5 | 6.5 | | | 7.5 | mA |
| $I_{IN}$ | Logic and logic reference Input current | $V_{IN} = 2.4V$<br>$V_{IN} = 0V$ | | | 10<br>–10 | | | 20<br>–20 | µA<br>µA |
| $I_H$ | Leakage current into hold capacitor[5] | HOLD mode | | .006 | .050 | | | 25 | nA |
| | Acquisition time to 0.1% | $V_{OUT} = 10V$<br>$C_H = 1000pF$<br>$C_H = 0.01\mu f$ | | <br>4<br>20 | | | | | <br>µs<br>µs |
| $I_C$ | Hold capacitor charging current | $V_{IN} - V_{OUT} = 2V$ | | 5 | | | | | mA |
| PSRR | Supply voltage rejection ratio | $V_{OUT} = 0$ | 80 | 110 | | 80 | | | dB |
| VTH | Differential logic threshold | | 0.8 | 1.4 | 2.4 | 0.8 | | 2.4 | V |

**NOTES:**

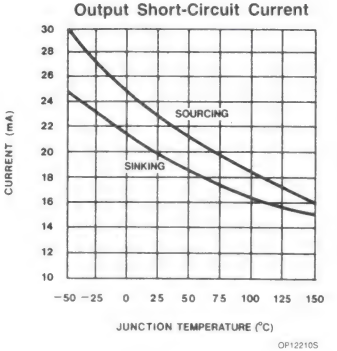
1. The maximum junction temperature of the 5537 is 150°C.
2. Although the differential voltage may not exceed the limits given, the common mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Unless otherwise specified, the following conditions apply: Unit is in "sample" mode, $V_S = \pm 15V$, $T_J = 25°C$, $-11.5V \leq V_{IN} \leq 11.5V$, $C_H = 0.01\mu F$, and $R_L = 2k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5. These parameters guaranteed over a supply voltage range of ±5 to ±18V.

## TYPICAL PERFORMANCE CHARACTERISTICS

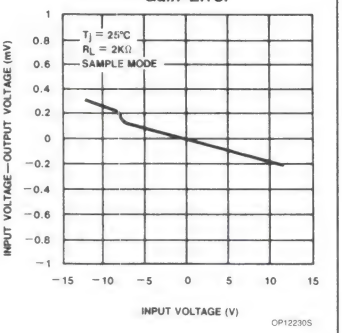
Input Bias Current



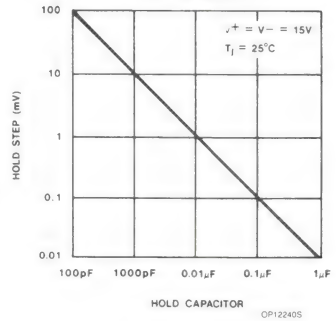

Output Short-Circuit Current



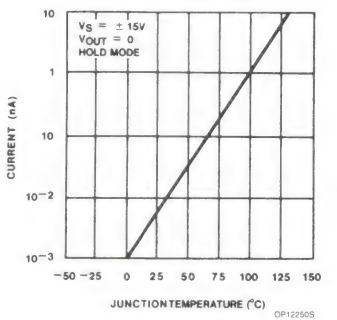

Gain Error



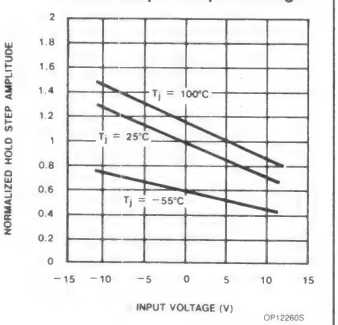

Hold Step



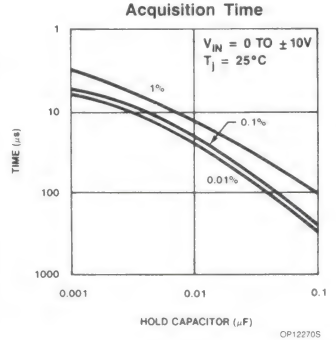

Leakage Current Into Hold Capacitor



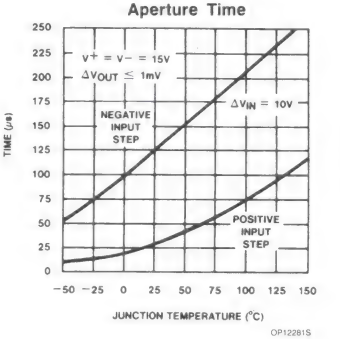

Hold Step vs Input Voltage



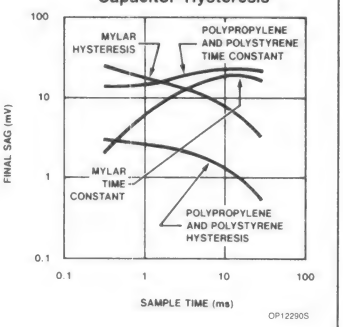

Acquisition Time




Aperture Time

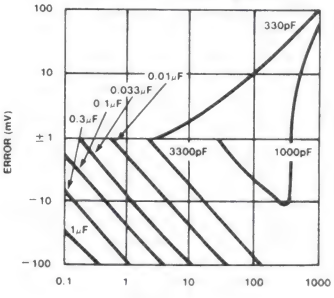



Capacitor Hysteresis



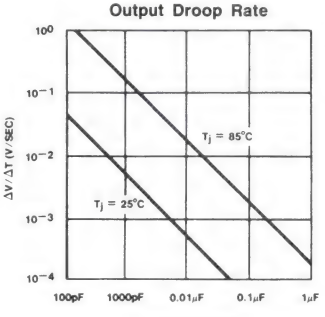
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### Dynamic Sampling Error



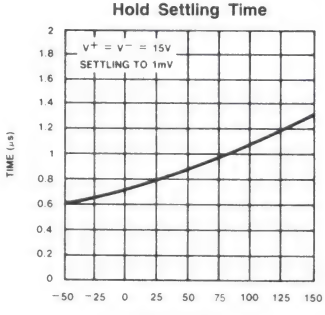

OP12300S

### Output Droop Rate



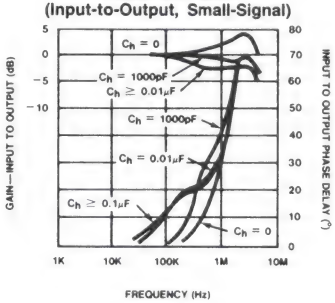

OP12310S

### Hold Settling Time



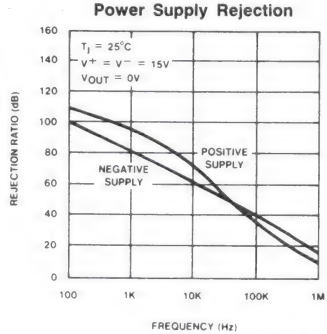

OP12320S

### Phase and Gain (Input-to-Output, Small-Signal)



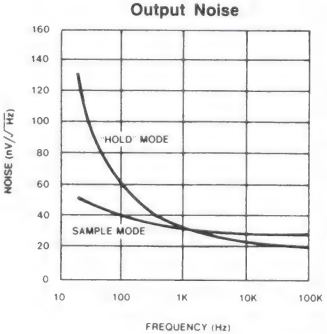

OP12330S

### Power Supply Rejection



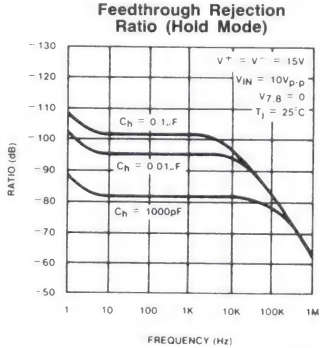

OP12340S

### Output Noise




OP12350S

### Feedthrough Rejection Ratio (Hold Mode)




OP12360S

# Sample-and-Hold Amplifier

5537

## SAMPLE–AND–HOLD

For many years designers have used the sample–and–hold (or track–and–hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout allows the designer certain freedom in performing predetermined manipulative functions. Therefore, the sample–and–hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample–and–hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog–to–digital converter products available today, the "DC memory" of the sample–and–hold can be easily converted to digital format and further incorporated into microprocessor based systems.

Parametric evaluation of the sample–and–hold will be discussed in the following paragraphs.

## DEFINITION OF TERMS

**Acquisition Time** — The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

**Aperture Delay Time** — The time elapsed from the hold command to the opening of the switch.

**Aperture Jitter** — Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

**Aperture Time** — The delay required between "hold" command and an input analog transition, so that the transition does not affect the held output.

**Bandwidth** — The frequency at which the gain is down 3dB from its DC value. It's measured in sample (track) mode with a small–signal sine wave that doesn't exceed the slew rate limit.

**Effective Aperture Delay** — The time difference between the hold command and the time at which the input signal is at the held voltage.

**Figure of Merit** — The ratio of the available charging current during sample mode to the leakage current during hold mode.

**Hold–Mode Droop** — The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

**Hold–Mode Feedthrough** — The percentage of an input sinusoidal signal that is measured at the output of a sample–hold when it's in hold mode.

**Hold Settling Time** — The time required for the output to settle within 1mV of final value after the "hold" logic command.

**Sample–to–Hold Offset Error** — The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

**Slew Rate** — The fastest rate at which the sample–and–hold output can change (specified in V/μs).

**Hold Step** — The voltage step at the output of the sample–and–hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5V.

**Dynamic Sampling Error** — The error introduced into the hold output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

**Gain Error** — The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

**Threshold Level** — will be defined as that level which causes the switch control to change state.

## BASIC BLOCK DIAGRAM

The basic circuit concept of the sample–and–hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions). Reference Figure 1.

The block diagram of the 5537 is a closed loop non–inverting unity gain sample–and–hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop such that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to all sample–and–hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode) the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample–and–hold device (see Figure 2). The switch control has a floating reference (Pin 7), referred to as the logic reference which makes the sample–and–hold device compatible to several types of external logic signals (TTL, PMOS, and CMOS). The switching device operates at a threshold level of 1.4V.

The switch mechanism is on (sampling an information stream) when the logic level is high (Pin 8 is 1.4V higher than Pin 7) and presents a load of 5μA to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (Pin 6) is loaded down by an operational amplifier connected in the unity gain non–inverting configuration. This amplifier, whose input impedance is effectively:

$$R = R_{IN}(A_{OL})/(1 + 1/A)$$

where
- $R$ = Effective input impedance
- $R_{IN}$ = Open loop input impedance
- $A_{OL}$ = Open loop gain
- $A$ = AC loop gain

Therefore, the higher the open loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality, the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation (remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature).

Sampling time for the 5537 is less than 10μsec, (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2kΩ.

## BASIC APPLICATIONS

### Multiplying DAC

As depicted in the block diagram of Figure 3, the sample–and–hold circuit is used to supply a "variable" reference to the digital–to–analog converter. As the input reference varies, the output will change in accordance with Equation 1, shown in Figure 3.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DAC's

used are the Signetics 5008; however, if the rate of change of the reference variation is kept slow enough a microprocessor compatible DAC can be incorporated, such as the 5018 or the 5020.

**Data Acquisition Systems**

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however, he is limited by the fact that only one analog to digital converter channel is available to him. Figure 4 shows the means by which a multiplexing system may be accomplished.

## APPLICATION HINTS

### Hold Capacitor

A significant source of error in an accurate sample–and–hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with > 1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10–50ms. If A–to–D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

### DC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1kΩ potentiometer which has one end tied to V+ and the other end tied through a resistor to ground. The resistor should be selected to give ≃0.6mA through the 1kΩ potentiometer.

### Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample–and–hold circuits. There exist finite phase delays through the sample–and–hold circuit causing an input–output phase differential for moving signals. In addition, the series protection resistor (300Ω to Pin 6 of the 5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 $V_{P-P}$ at 10kHz. Maximum dV/dt is 0.6V/μs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1μs) (0.6V/μs) = 60mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive going input would give a ± 60mv error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs) (0.6V/μs) = –96mV (analog) for a total of –36mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled "Aperture Time" has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "HOLD" command. This curve is based on a 1mV error fed into the output.

A second curve, "Hold Settling Time", indicates the time required for the output to settle to 1mV after the "HOLD" command.

### Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

**Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a PC card trace connected to the sample–and–hold output. This will also minimize board leakage.**

## SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the 5537, but are legitimate terms used in sample–and–hold systems.
2. Reference should be made to *Design Engineering*, Volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc. for a further discussion of sample–and–hold circuits.
3. Reference also made to National Semiconductor's Special Functions Data Book (1976.)

## TYPICAL APPLICATIONS

TYPICAL CONNECTION

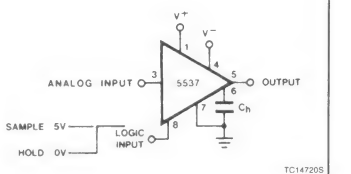
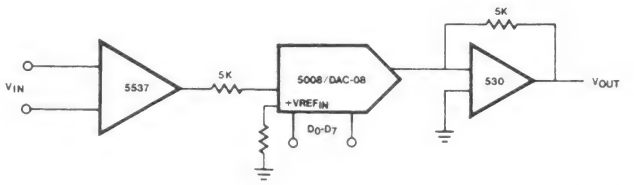



Figure 2

## MULTIPLYING DAC APPLICATION




**NOTE:**

$$V_{OUT} = V_{IN} \times \frac{1}{256} \left\{ 20\ D_0 + 2^1 D_1 + 2^7 D_7 \right\} \quad \text{Equation 1}$$

**Figure 3**

## ANALOG DATA MULTIPLEXING

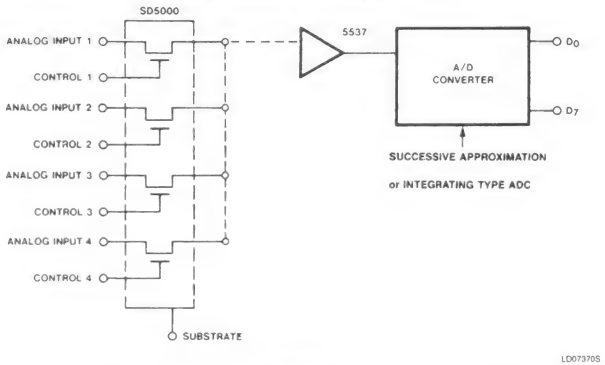



**Figure 4**

Signetics

# 5539

## Ultra High-Frequency Operational Amplifier

*Product Specification*

**Military Linear Products**

### DESCRIPTION

The Signetics 5539 is a very wide band-width, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed loop gains, both inverting and non-inverting, to meet specific design requirements.

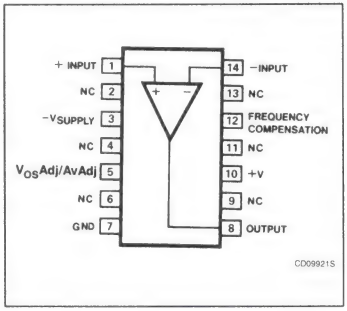
### FEATURES

- **Gain bandwidth product: 1.2GHz at 17dB**
- **Slew rate: 600/V$\mu$s**
- **Full power response: 48MHz**
- **$A_{VOL}$: 52dB typical**
- **350 MHz unity gain**

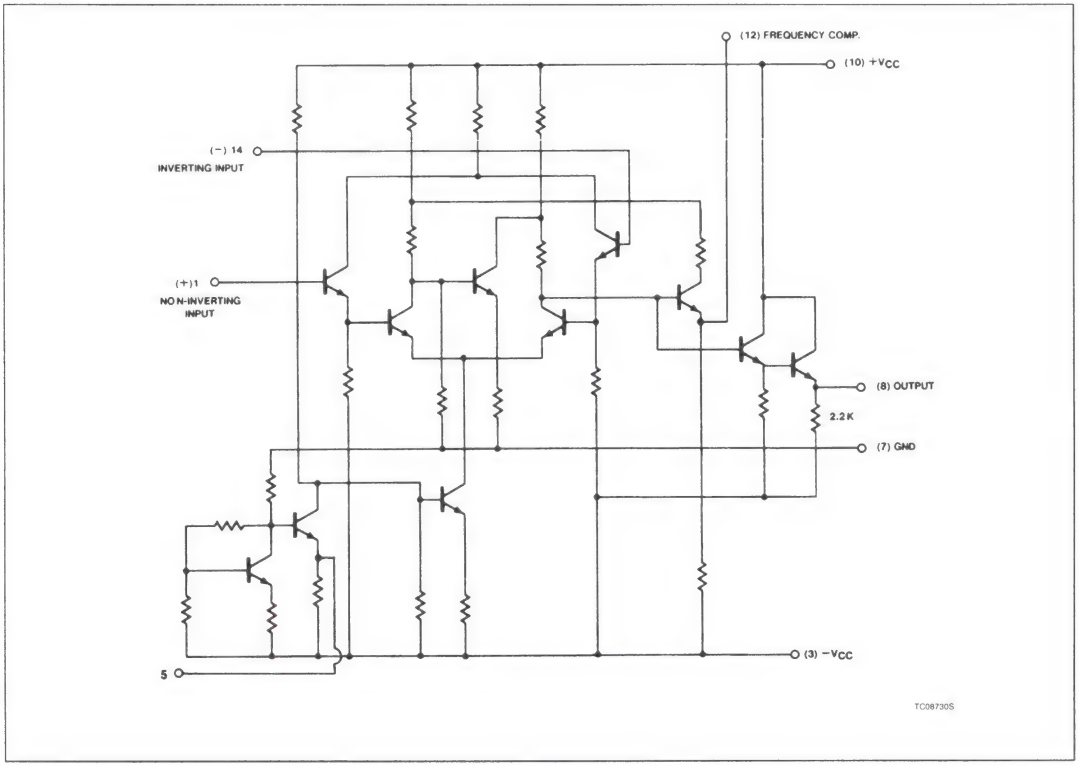
### APPLICATIONS

- **Fast pulse amplifers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

### PIN CONFIGURATION




### EQUIVALENT CIRCUIT



# Ultra High-Frequency Operational Amplifier 5539

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 14–Pin Ceramic DIP | 5539/BCA |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | ±12 | V |
| $P_D$ | Internal power dissipation | 550 | mW |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Max junction temperature | 150 | °C |

## DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = ± 8V, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{IO}$ | Input offset voltage | $V_O$ = 0V, $R_S$ = 100Ω | | | 2 | 3 | | | 5 | mV |
| $I_{IO}$ | Input offset current | | | | 0.1 | 1.0 | | | 3.0 | µA |
| $I_{IB}$ | Input bias current | | | | 5 | 13 | | | 25 | µA |
| CMRR | Input common mode[2] rejection ratio | f = 1kHz, $R_S$ = 100Ω $V_{CM}$ = ±1.7V | | 70 | 80 | | 70 | | | dB |
| $R_{IN}$ | Input impedance | | | | 100 | | | | | kΩ |
| $R_{OUT}$ | Output impedance | | | | 10 | | | | | Ω |
| $V_{OUT}$ | Output voltage swing | $R_L$ = 2kΩ to GND | $V_O$+ | +2.5 | +3.1 | | +2.3 | | | V |
| | | | $V_O$– | –2.0 | –2.7 | | –1.5 | | | V |
| $I_{CC}$+ | Positive supply current | $V_O$ = 0, $R_1$ = ∞ | | | 14 | 17 | | | 18 | mA |
| $I_{CC}$– | Negative supply current | $V_O$ = 0, $R_1$ = ∞ | | | 11 | 14 | | | 15 | mA |
| PSRR | Power supply rejection ratio | $\Delta V_{CC}$ = ±1V | | | 200 | 1000 | | | 1000 | µV/V |
| $A_V$ | Large signal voltage gain | $V_O$ = $V_O$+min, $V_O$–min $R_L$ = 2kΩ to GND | | 48 | 53 | 58 | 46 | | 60 | dB |

# Ultra High-Frequency Operational Amplifier | 5539

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND and $470\Omega$ to $-V_{CC}$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| GBW | Gain bandwidth product[3] | $A_{CL} = 7$ $V_O = 0.1V_{P-P}$ | | 1200 | | | | | MHz |
| GBW | Small signal bandwidth[3] | $A_{CL} = 2$ $R_L = 150\Omega$ | | 110 | | | | | MHz |
| $t_S$ | Settling time[3] | $A_{CL} = 2$ $R_L = 150\Omega$ | | 15 | | | | | ns |
| SR | Slew rate[3] | $A_{CL} = 2$ $R_L = 150\Omega$ | | 600 | | | | | V/µs |
| $t_P$ | Propagation delay[3] | $A_{CL} = 2$ $R_L = 150\Omega$ | | 7 | | | | | ns |
| $f_{FP}$ | Full power response[3] | $A_{CL} = 2$ $R_L = 150\Omega$ | | 48 | | | | | MHz |
| $f_{FP}$ | Full power response | $A_V = 7$, $R_L = 150\Omega$ | | 20 | | | | | MHz |
| En | Input noise voltage | $R_S = 50\Omega$ | | 4 | | | | | $^{NV}/\sqrt{Hz}$ |

## DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OS}$ | Input offset voltage | | | | 2 | 3 | | | 5 | mV |
| $I_{OS}$ | Input offset current | | | | 0.1 | 1 | | | 3 | µA |
| $I_B$ | Input bias current | | | | 4 | 10 | | | 20 | µ |
| CMRR | Input common mode rejection ratio | $V_{CM} = \pm 1.3V$ $R_S = 100\Omega$ | | 70 | 80 | | | | | dB |
| $I_{CC+}$ | Positive supply current | | | | 11 | 13 | | | 14 | mA |
| $I_{CC-}$ | Negative supply current | | | | 8 | 10 | | | 11 | mA |
| PSRR | Power supply rejection ratio | $\Delta V_{CC} = \pm 1V$ | | | 300 | 1000 | | | 1000 | µV/V |
| $V_{OUT}$ | Output voltage swing | $R_L = 150\Omega$ to GND | $V_{O+}$ | +1.5 | +2.0 | | +1.4 | | | V |
| | | and $389\Omega$ to $-V_{CC}$ | $V_{O-}$ | −1.4 | −1.8 | | −1.1 | | | V |

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and $390\Omega$ to $-V_{CC}$, unless otherwise specified.

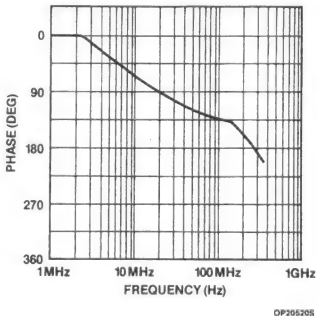
| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A = +25°C$ | | | $T_A = -55°C, +125°C$ | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| GBW | Gain bandwidth product | $A_{CL} = 7$ | | 700 | | | | | MHz |
| GBW | Small signal bandwidth | $A_{CL} = 2^3$ | | 120 | | | | | MHz |
| $t_S$ | Settling time | $A_{CL} = 2^3$ | | 23 | | | | | ns |
| SR | Slew rate | $A_{CL} = 2^3$ | | 330 | | | | | V/µs |
| $t_P$ | Propagation delay | $A_{CL} = 2^3$ | | 4.5 | | | | | ns |
| $f_{FP}$ | Full power response[3] | $A_{CL} = 2^3$ | | 20 | | | | | MHz |

**NOTE:**
1. Operation beyond limits in this table may impair the useful life of the device.
2. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common mode voltage 2.5V. These voltage limits may be exceeded if current limit is 10mA.
3. External compensation.
4. External compensation.

# Ultra High-Frequency Operational Amplifier | 5539

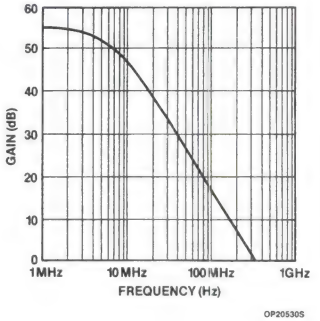
## TYPICAL PERFORMANCE CHARACTERISTICS

5539 Open-Loop Phase



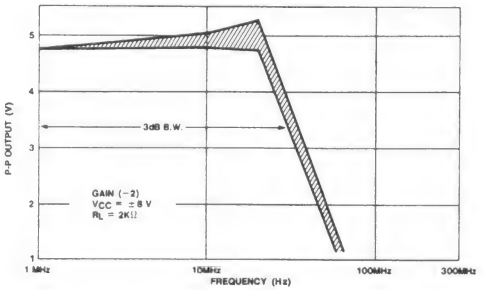

OP20520S

5539 Open-Loop Gain



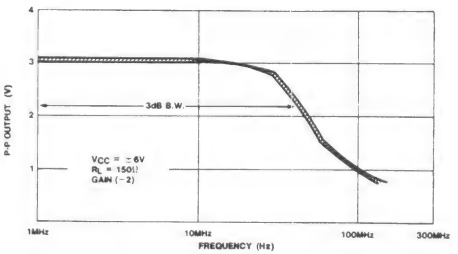

OP20530S

Power Bandwidth



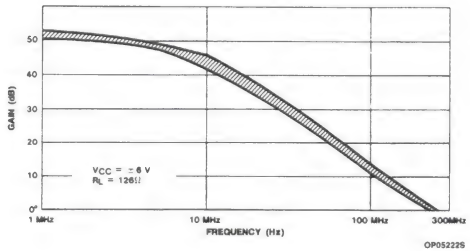

OP05202S

Power Bandwidth



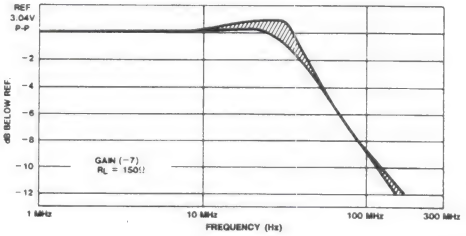

OP05212S

5539 Open-Loop Gain vs Frequency




OP05222S

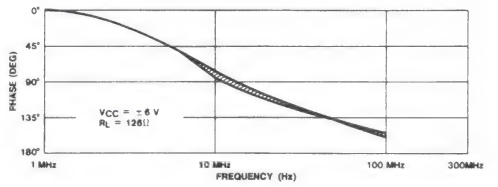
Power Bandwidth




OP05231S

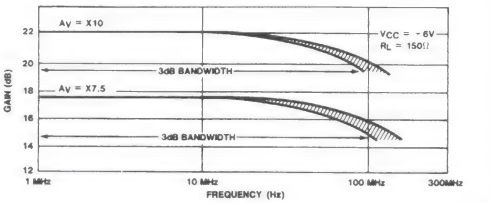
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

**5539 Open-Loop Phase vs Frequency**




OP05241S

**Gain Bandwidth Product vs Frequency**




OP05251S

NOTE

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

Signetics

# 5560

## Switched-Mode Power Supply Control Circuit

*Product Specification*

**Military Linear Products**

### DESCRIPTION

The 5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener references, sawtooth generator, pulse width modulator, output stage and various protection circuits.

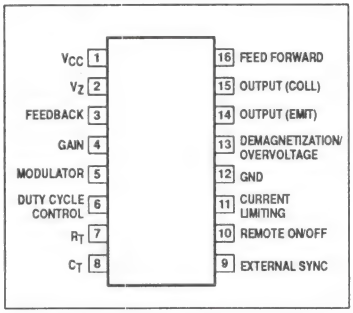
### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 16-Pin Ceramic DIP | 5560/BEA |

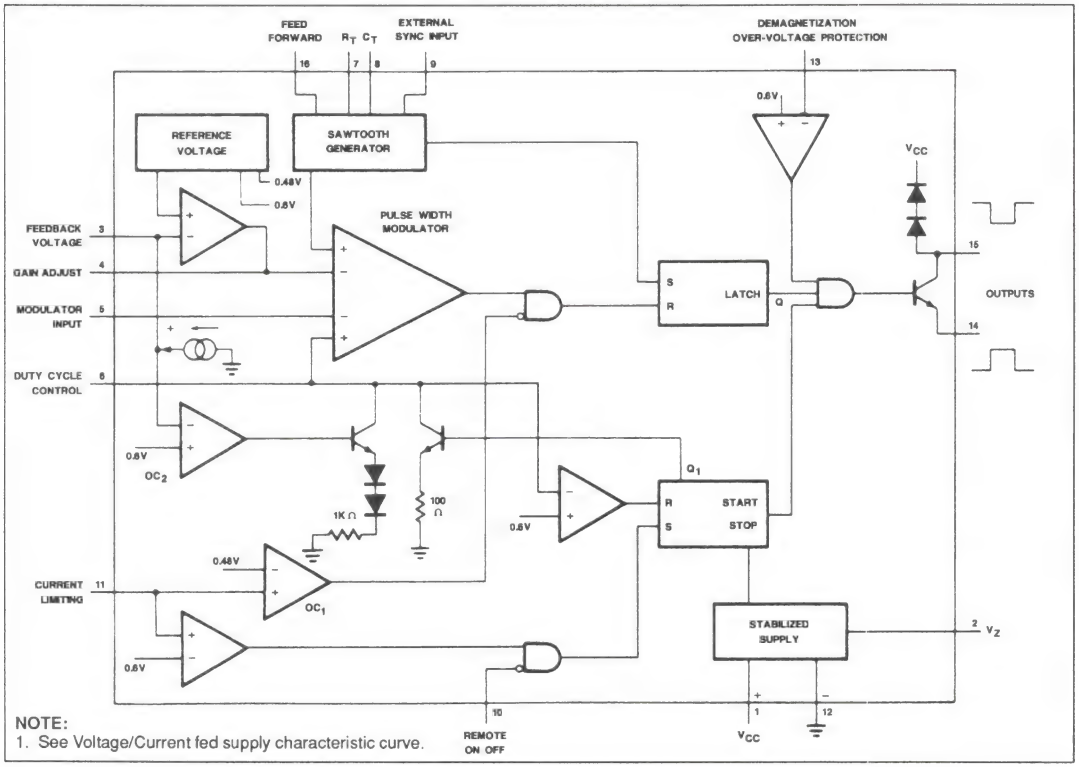
### FEATURES

- Stabilized power supply
- Temperature compensated reference source
- Sawtooth generator
- Pulse width modulator
- Remote on/off switching
- Current limiting
- Low supply voltage protection
- Loop fault protection
- Demagnetization/overvoltage protection
- Maximum duty cycle clamp
- Feed forward control
- External synchronization

### PIN CONFIGURATION




### BLOCK DIAGRAM




NOTE:
1. See Voltage/Current fed supply characteristic curve.

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING[2] | UNIT |
|---|---|---|---|
| | Supply[1] | | |
| $V_S$ | Voltage forced mode | +18 | V |
| $I_S$ | Current fed mode | 30 | mA |
| | Output transistor (at 20 – 30V max) | | |
| $I_C$ | Output current | 40 | mA |
| $V_C$ | Collector voltage (Pin 15) | $V_{CC}$ + 1.4V | V |
| $V_E$ | Max. emitter voltage (Pin 14) | +5 | V |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = 12V, unless otherwise specified.

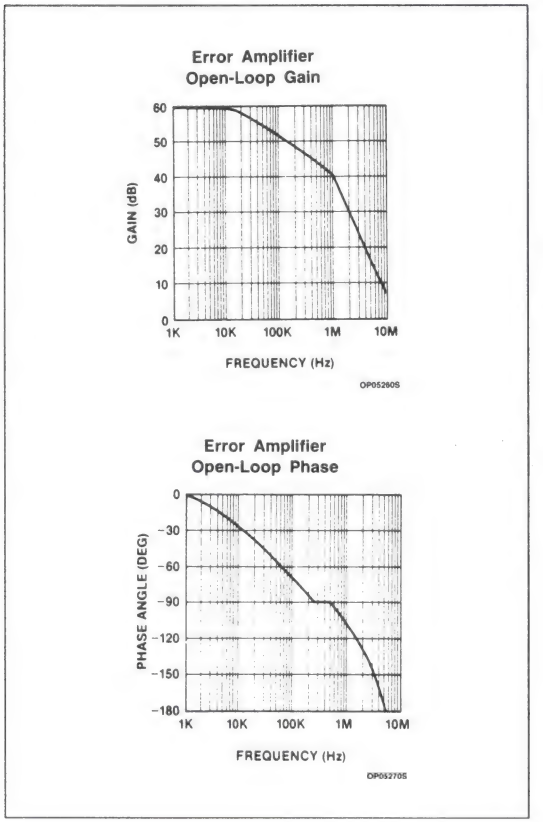
| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **Reference Section** | | | | | | | | | |
| $V_{REF}$ | Internal reference voltage | | 3.69 | 3.72 | 3.81 | 3.65 | | 3.85 | V |
| $\Delta V_{REF}/\Delta T$ | Temperature coefficient | | | | | | –100 | | ppm/°C |
| $V_Z$ | Internal Zener reference | $I_L$ = –7mA | 7.8 | 8.4 | 8.8 | | | | V |
| $\Delta V_Z/\Delta T$ | Temperature coefficient | | | | | | 200 | | ppm/°C |
| **Oscillator Section** | | | | | | | | | |
| $f_R$ | Frequency range | | 50 | | 100k | 50 | | 100k | Hz |
| $\Delta f_R$ | Initial accuracy oscillator | R = 5kΩ | | 5 | | | | | % |
| D.C. | Duty cycle range[4] | $f_o$ = 20kHz | 0 | | 98 | | | | % |
| **Modulator, Pin 5** | | | | | | | | | |
| $I_I$ | Modulation input current | Voltage at Pin 5 = 2V | | | 20 | | | 20 | µA |
| **Housekeeping Function** | | | | | | | | | |
| $I_I$ | Pin 6, input current | Pin 6 = 2V | | | 20 | | | 20 | µA |
| D.C. (6) | Pin 6, duty cycle limit control | (for 50% max duty cycle) 15kHz to 50kHz/41% of $V_Z$ | 40 | 50 | 60 | | | | % of duty cycle |
| $V_{CC(TH)}$ | Pin 1, low supply voltage protection thresholds | | 8 | 9.0 | 10.5 | | | | V |
| $V_{TH(3)}$ | Pin 3, feedback loop protection trip threshold | | 400 | 600 | 720 | | | | mV |
| $I_{fo}$ | Pin 3, pull up current | Pin 3 = 2V | –7 | –15 | –35 | –7 | | –35 | µA |
| $V_{TH(13)}$ | Pin 13, demagnetization/over voltage protection trip on threshold | | 470 | 600 | 720 | | | | mV |
| $I_{I(13)}$ | Pin 13, input current | Pin 13 = 0.25V | | –0.6 | –10 | | | –20 | µA |
| D.C.$_{ff}$ | Pin 16, feed forward duty cycle control | Pin 16 = 2$V_Z$ | 30 | 40 | 50 | | | | % original duty cycle |
| $I_{I(16)}$ | *Pin 16, feed forward input[3] | Pin 16 = 16V, $V_{CC}$ = 18V | | 0.2 | 5 | | | 10 | µA |

## DC ELECTRICAL CHARACTERISTICS (Continued)

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = –55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| **External Synchronization** | | | | | | | | | |
| $V_{OFF(9)}$ | Pin 9 off | | 0 | | 0.8 | | | | V |
| $V_{ON(9)}$ | Pin 9 on | | 2 | | $V_Z$ | | | | V |
| $I_{I(9)}$ | Pin 9 sink current | Pin 9 = 0V | | –65 | –100 | | | –125 | µA |
| **Remote** | | | | | | | | | |
| $V_{OFF(10)}$ | Pin 10 off | | 0 | | 0.8 | | | | V |
| $V_{ON(10)}$ | Pin 10 on | | 2 | | $V_Z$ | | | | V |
| $I_{I(10)}$ | Pin 10 sink current | Pin 10 = 0V | | –85 | –100 | | | –125 | µA |
| **Current Limiting** | | | | | | | | | |
| $I_{I(11)}$ | Pin 11 | Pin 11 = 250mV | | –2 | –20 | | | –40 | µA |
| $T_{D(11)}$ | Single pulse inhibit delay[4] (Pin 11) | Inhibit delay time for 20% overdrive at 40mA $I_{OUT}$ | | 0.7 | 0.8 | | | | µs |
| $V_{TH(SD)}$ | Trip Levels: Shut down, Slow start | | 0.560 | 0.600 | 0.700 | | | | V |
| $V_{TH(CL)}$ | Trip Level: Current limit | | 0.400 | 0.480 | 0.500 | | | | V |
| **Error Amplifier** | | | | | | | | | |
| $V_{OH}$ | Output voltage swing | | 6.2 | | 9.5 | | | | V |
| $V_{OL}$ | Output voltage swing | | | | 0.7 | | | | V |
| $A_O$ | Open–loop gain | | 54 | 60 | | | | | dB |
| $R_f$ | Feedback resistor | | 10k | | | | | | Ω |
| BW | Small signal bandwidth | | | 3 | | | | | MHz |
| **Output Stage** | | | | | | | | | |
| $V_{CE(SAT)}$ | Output collector (Pin 15) | $V_{CE(SAT)}$ $I_C$ = 40mA | | | 0.5 | | | | V |
| $V_{E(MAX)}$ | Max emitter voltage (Pin 14)[4] | $V_C$ = 12V, $I_E$ = –200mA | 5 | 6 | | | | | V |
| **Supply Voltage/Current** | | | | | | | | | |
| $I_{CC}$ | Pin 1 | $I_Z$ = 00, voltage forced | | | 10 | | | 15 | mA |
| $V_{CC}$ | Pin 1 | $I_{CC}$ = 10mA current fed | 20 | | 23 | | | | V |
| $V_{CC}$ | Pin 1 | $1_{CC}$ = 30mA current fed | 20 | | 30 | | | | V |

**NOTE:**
1. See voltage/current fed supply characteristics curve.
2. Operation beyond limits in the table may impair the useful life of the device.
3. Does not include current for timing resistors or capacitors.
4. This parameter is guaranteed but not tested.

## TYPICAL PERFORMANCE CHARACTERISTICS




## MAXIMUM PIN VOLTAGES

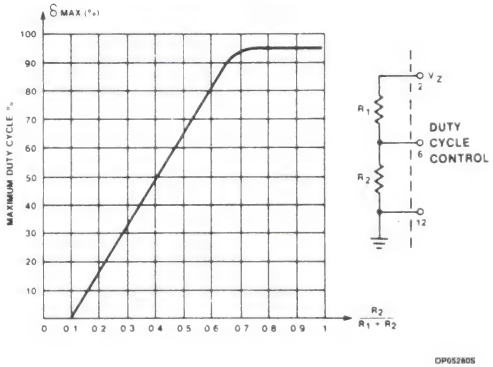
| Function | Maximum Voltage |
|---|---|
| 1. $V_{CC}$ | See Note 1 |
| 2. $V_Z$ | Do not force (8.4V) |
| 3. Feedback | $V_Z$ |
| 4. Gain | |
| 5. Modulator | $V_Z$ |
| 6. Duty Cycle Control | $V_Z$ |
| 7. $R_T$ | Current force mode |
| 8. $C_T$ | |
| 9. External Synch | $V_Z$ |
| 10. Remote On/Off | $V_Z$ |
| 11. Current Limiting | $V_{CC}$ |
| 12. GND | GND |
| 13. Demagnetization/Overvoltage | $V_{CC}$ |
| 14. Output (Emit) | $V_Z$ |
| 15. Output (Collector) | $V_{CC}$ + 2Vbe |
| 16. Feed forward | $V_{CC}$ |

**NOTE:**

1. When voltage forced, max. is 18V; when current fed. max is 30mA. See voltage/current fed supply characteristic curve.

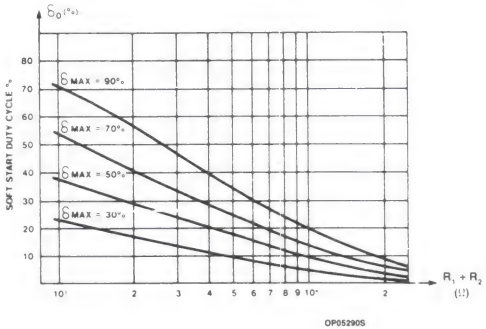
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### Graph for Determining $\delta_{MAX}$



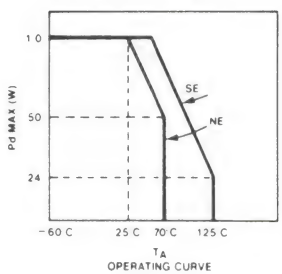

OP05280S

### Soft-Start Min. Duty Cycle vs $R_1 + R_2$



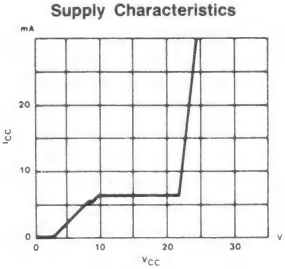

OP05290S

### Power Derating Curve



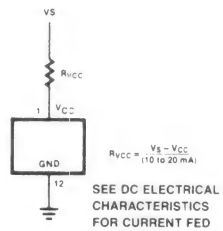

OP05300S

### 5560 Voltage-/Current-Fed Supply Characteristics



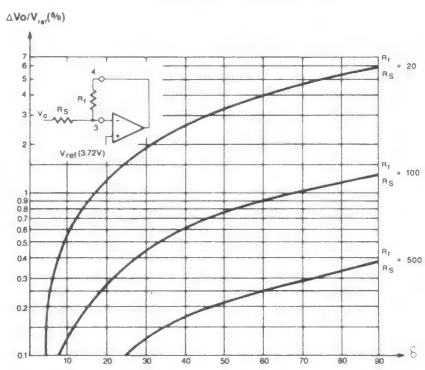

OP05310S

### Current-Fed Dropping Resistor



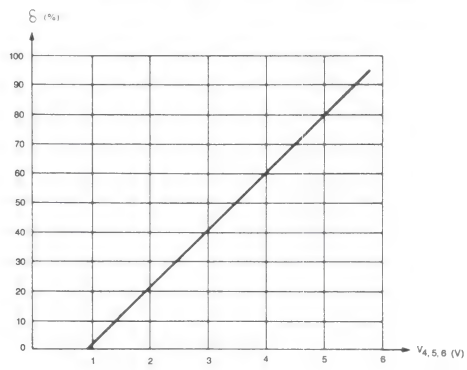

TC08780S

### Regulation vs Error Amp Closed-Loop Gain




OP05320S

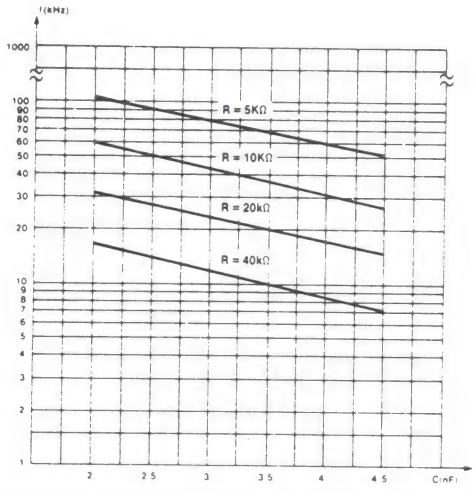
### Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage



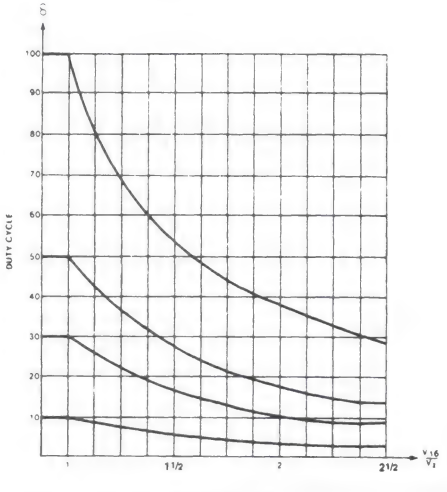

OP05330S

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Typical Frequency Plot vs $R_T$ and $C_T$




Duty Cycle Sensitivity to Feed-Forward Voltage (Pin 16)




## THEORY OF OPERATION

The following functions are incorporated:

- A temperature compensated reference source.
- An error amplifier with Pin 3 as input. The output is connected to Pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (Pins 7,8,9).
- A pulse-width modulator with a duty-cycle range from 0 to 95%.

(The PWM has two additional inputs:

Pin 6 can be used for a precise setting of $\delta$ max.

Pin 5 gives a direct access to the modulator, allowing for real constant current operation:)

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above-mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore Pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at Pin 10, also operating via the start-stop circuit.
- An inhibit input at Pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (Pin 15) and the emitter (Pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage or current driven (Pins 1 and 12). The internally generated stabilized output voltage $V_Z$ is connected to Pin 2.
- A special function is the so-called feed-forward at Pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim 1/V16$
- Loop fault protection circuits assure that the duty-cycle is reduced to zero or a low value for open or short-circuited feedback loops.

### Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the 5560 is of the well known series regulation type and provides a stabilized output voltage of typically 8.5V.

This voltage $V_Z$ is also present at Pin 2 and can be used for precise setting of $\delta$ max. and to supply external circuitry. Its max. current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage: typical 23V for 10mA and max. 30V for 30mA.

The low supply voltage protection is active when V(1 – 12) is below 10.5V and inhibits the output pulse (no hysteresis).

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from $V_Z$ and R(7 – 12) > 20kΩ.

### The Sawtooth Generator

Figure 2 shows the principal circuitry of the oscillator. A resistor between Pin 7 and Pin 12 (GND) determines the constant current that charges the timing capacitor C(8 – 12).

This causes a linear increasing voltage on Pin 8 until the upper level of 5.6V is reached. Comparator H sets the RS flip-flop and $Q_1$ discharges C(8 – 12) down to 1.1V, where comparator L resets the flip-flop. During this flyback time, $Q_2$ inhibits the output.

Synchronization at a frequency lower than the free-running frequency is accomplished via the TTL gate on Pin 9. By activating this gate

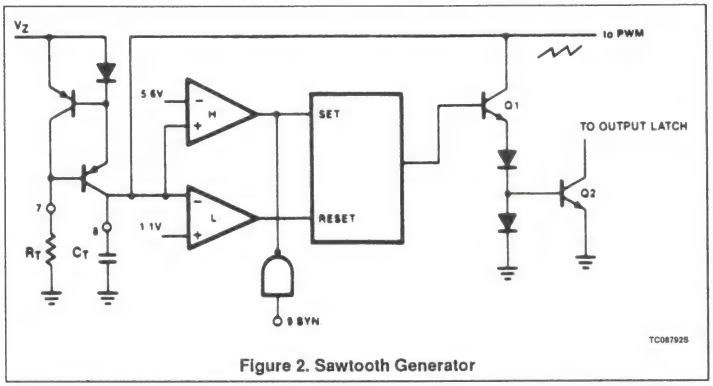



Figure 2. Sawtooth Generator

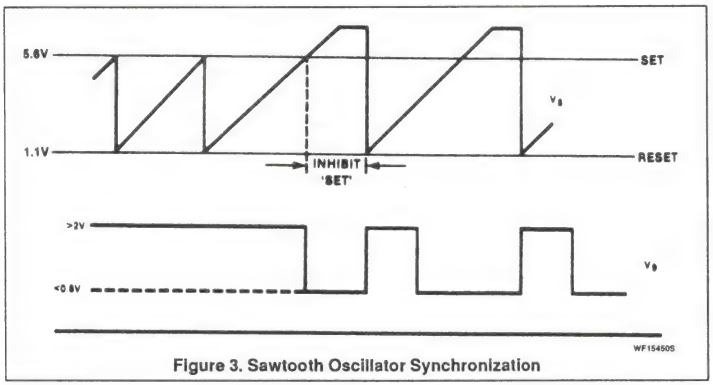



Figure 3. Sawtooth Oscillator Synchronization

($V^9$ < 2V), the setting of the sawtooth is prevented. This is indicated in Figure 3.

Figure 4 shows a typical plot of the oscillator frequency against the timing capacitor. The frequency range of the 5560 goes from < 50Hz up to > –100kHz.

## Reference Voltage Source

The internal reference voltage source is based on the bandgap voltage of silicon. Good design practice assures a temperature dependency typically ± 100ppm/°C. The reference voltage is connected to the positive input of the error amplifier and has a typical value of 3.72V.

## Error Amp Compensation

For closed-loop gains less than 40dB, it is necessary to add a simple compensation capacitor as shown in Figures 4, 5.

## Error Amplifier with Loop-Fault Protection Circuits

This operational amplifier is of a generally used concept and has an open-loop gain of typically 60dB. As can be seen in Figure 5, the inverting input is connected to Pin 3 for a feedback information proportional to $V_O$.

The output goes to the PWM circuit, but is also connected to Pin 4, so that the required gain can be set with $R_S$ and R(3 - 4). This is indicated in Figure 5, showing the relative change of the feedback voltage as a function of the duty cycle. Additionally, Pin 4 can be used for phase shift networks that improve the loop stability.

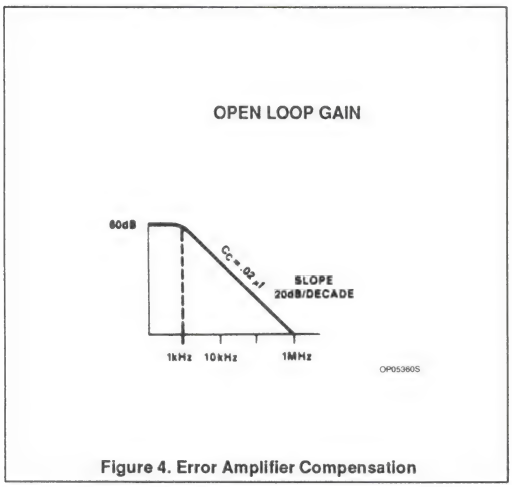



Figure 4. Error Amplifier Compensation

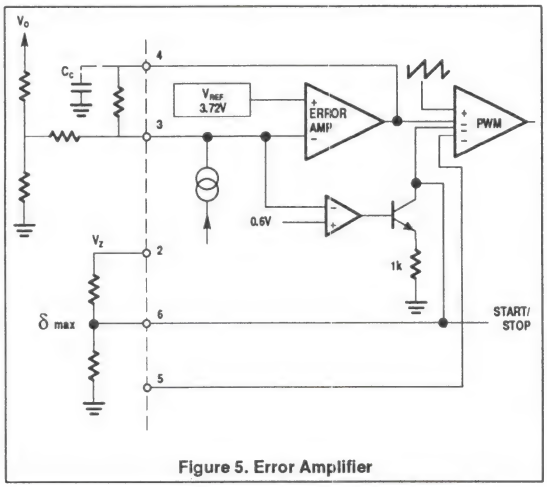
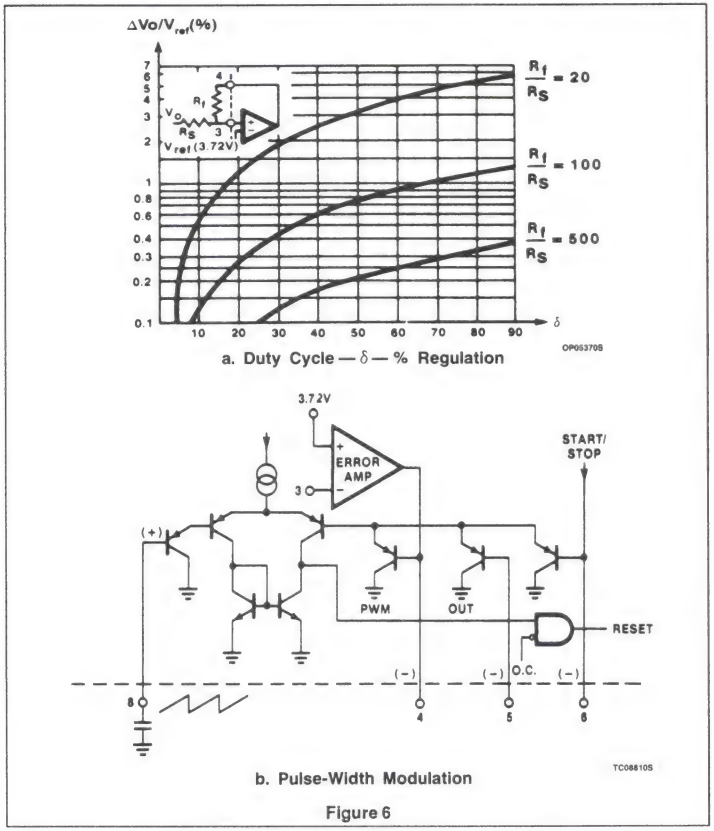



Figure 5. Error Amplifier




a. Duty Cycle — δ — % Regulation

b. Pulse-Width Modulation

Figure 6

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via R(3 – 4). This would result in a large duty cycle. A current source on Pin 3 prevents this by pushing the input voltage high via the voltage drop over R(3 – 4). As a result, the duty cycle will become zero, provided that R(3 – 4) > 100k. When the feedback loop is short-circuited, the duty cycle would jump to the adjusted max. duty cycle. Therefore, an additional comparator is active for feedback voltages at Pin 3 below 0.6V. Now an internal resistor of typically 1k is shunted to the impedance on the $\delta_{MAX}$ setting Pin 6. Depending on this impedance, $\delta$ will be reduced to a value $\delta_o$. This will be discussed further.

## The Pulse-Width Modulator

The function of the PWM circuit is to translate a feedback voltage into a periodical pulse of which the duty cycle depends on that feedback voltage. As can be seen in Figure 6, the PWM circuit in the 5560 is a long-tailed pair in which the sawtooth on Pin 8 is compared with the LOWEST voltage on either Pin 4 (error amplifier), Pin 5, or Pin 6 $\delta_{MAX}$ and slow-start). The transfer graph is given in Figure 7. The output of the PWM causes the resetting of the output bistable.

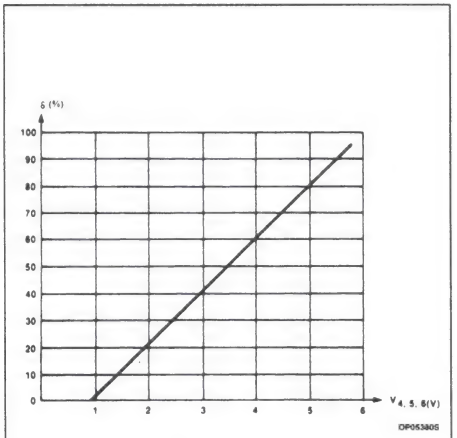



Figure 7. Transfer Curve of Pulse Width Modulator Duty Cycle vs Input Voltage

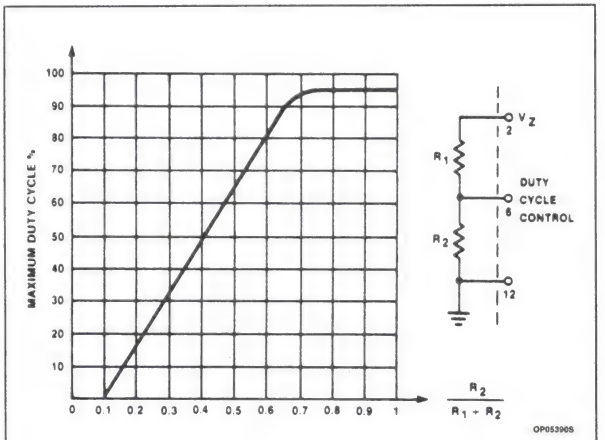



Figure 8. Graph for Determining δ

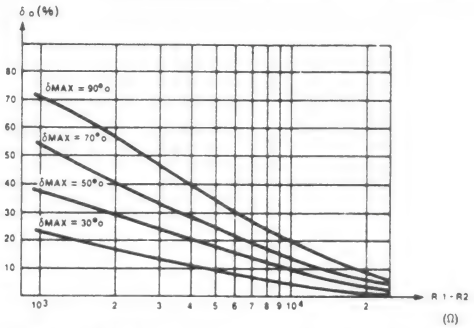



Figure 9. Soft-Start Min Duty Cycle vs $R_1 + R_2$

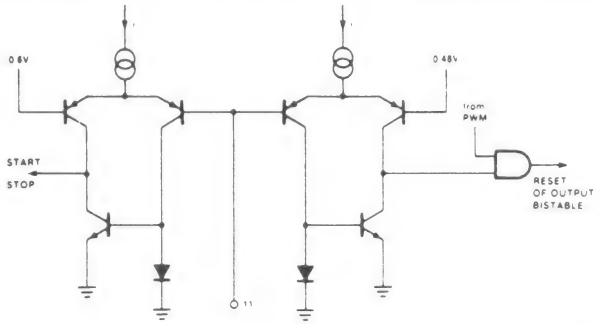



Figure 10. Current Protection Input

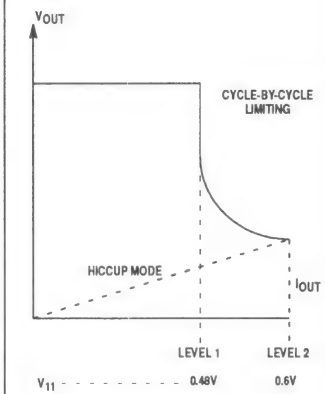



Figure 11. Output Characteristic

## Limitation of the Maximum Duty Cycle

With Pins 5 and 6 not connected and with a rather low feedback voltage on Pin 3, the 5560 will deliver output pulses with a duty cycle of ≈95%. In many SMPS applications, however, this high $\delta$ will cause problems. Especially in forward converters, where the transformer will saturate when $\delta$ exceeds 50%, a limitation of the max. duty-cycle is a must.

A DC voltage applied to Pin 6 (PWM input) will set $\delta_{MAX}$, at a value in accordance with Figure 7. For low tolerances of $\delta_{MAX}$, this voltage on Pin 6 should be set with a resistor divider from $V_Z$ (Pin 2). The upper and lower sawtooth levels are also set by means of an internal resistor divider form $V_Z$, so forming a bridge configuration with the $\delta_{MAX}$ setting is low because tolerances in $V_Z$ are compensated and the sawtooth levels are determined by internal resistor matching rather than by absolute resistor tolerance. Figure 8 can be used for determining the tap on the bleeder for a certain $\delta_{MAX}$ setting.

As already mentioned, Figure 9 gives a graphical representation of this. The value $\delta_O$ is limited to the lower and the higher side;

- It must be large enough to ensure that at max. load and min. input voltage the resulting feedback voltage on Pin 3 exceeds 0.6V.
- It must be small enough to limit the amount of energy in the SMPS when a loop-fault occurs. In practice a value of 10 – 15% will be a good compromise.

## Extra PWM Input (Pin 5)

The PWM has an additional inverting input: Pin 5. It allows for attacking the duty cycle via the PWM circuit, independently from the feedback and the $\delta_{MAX}$ information. This is necessary when the SMPS must have a real constant current behavior, possibly with a fold-back characteristic. However, the realization of this feature must be done with additional external components. When not used, Pin 5 should be tied to Pin 6.

## Dynamic Current Limit and Current Protection (Pin 11)

In many applications, it is not necessary to have a real constant current output of the SMPS.

Protection of the power transistor will be the prime goal. This can be realized with the 5560 in an economical way. A resistor (or a current transformer) in the emitter of the power transistor gives a replica of the collector current. This signal must be connected to Pin 11. As can be seen in Figure 10, this input has two comparators with different reference levels. The output of the comparator with the lower 0.48V reference is connected to the same gate as the output of the PWM.

When activated, it will immediately reset the output flip-flop, so reducing the duty cycle. The effectiveness of this cycle-by-cycle current limit diminishes at low duty cycle values. When $\delta$ becomes very small, the storage time of the power transistor becomes dominant. The current will now increase again, until it surpasses

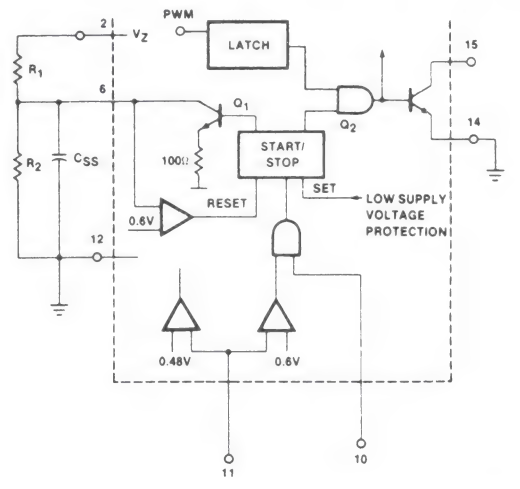



Figure 12. Start/Stop Circuit

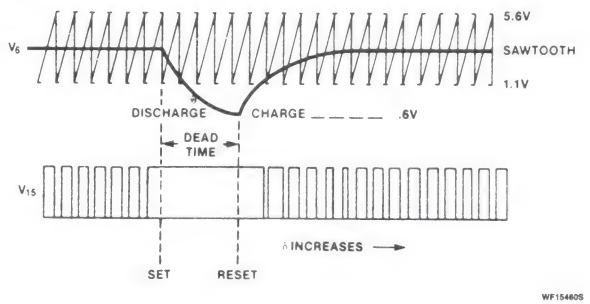



Figure 13. Start/Stop Circuit

the reference of the second comparator. The output of this comparator activates the start/stop circuit and causes an immediate inhibit of the output pulses. After a certain dead-time, the circuit starts again with very narrow output pulses. The effect of this two-level current protection circuit is visualized in Figure 11.

## The Start/Stop Circuit

The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods.

After this dead-time, the output starts with a very small, gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This "hiccup" mode limits effectively the energy during fault conditions. The realization and the working of the circuit is indicated in the Figures 12 and 13. The dead-time and the soft-start are determined by an external capacitor that is connected to Pin 6 ($\delta_{MAX}$ setting).

A RS flip-flop can be set by three different functions:

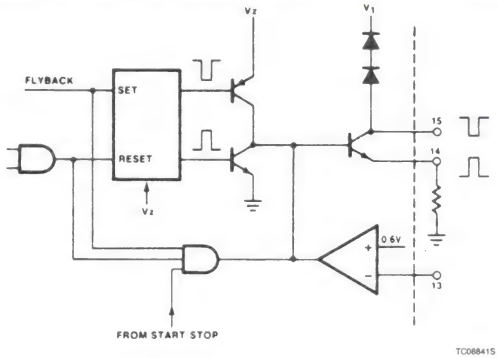
1. Remote on/off on Pin 10.
2. Overcurrent protection on Pin 11.
3. Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the flip-flop, the output pulses are blocked via the output gate. In the same time transistor $Q_1$ is forward-biased, resulting in a discharge of the capacitor on Pin 6.

The discharging current is limited by an internal 150Ω resistor in the emitter of $Q_1$. the voltage at Pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the flip-flop is reset. The output stage is no longer blocked and $Q_1$ is cut-off. Now $V_Z$ will charge the capacitor via $R_1$ to the normal $\delta_{MAX}$ voltage. The output starts delivering very narrow pulses as soon as $V_6$ exceeds the lower sawtooth level. The duty-cycle of the output pulse now gradually increases to a value determined by the feedback on Pin 3, or by the static $\delta_{MAX}$ setting on Pin 6.

## Remote On/Off Circuit (Pin 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applications in which a supply must be switched by a logical signal. This can be done via the TTL-compatible remote on/off input on Pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage > 2V is applied. Start-up occurs via the slow-start circuit.




**NOTE:**
The signal $V_{13}$ can be derived from the demagnetizing winding in a forward converter as shown below.

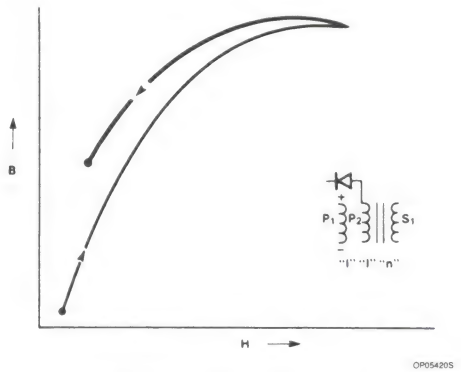



**Figure 14. Output Stage**

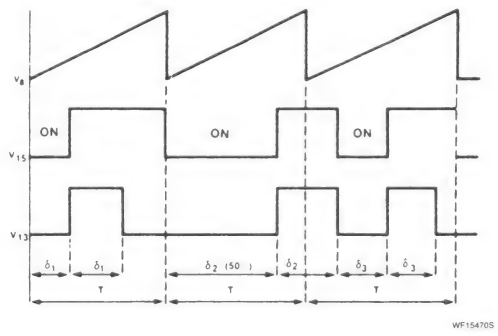



**Figure 15. Output Stage Inhibit**

## The Output Stage

The output stage of the 5560 contains a flip-flop, a push-pull driven output transistor, and a gate, as indicated in Figure 14. The flip-flop is set by the flyback of the sawtooth. Resetting occurs by a signal either from the PWM or the current limit circuit. With this configuration, it is assured that the output is switched only once per period, thus prohibiting double pulsing. The collector and emitter of the output transistor are connected respectively to Pin 15 and Pin 14, allowing for normal or inverted output pulses. An internally grounded emitter would cause untolerable voltage spikes over the bonding wire, especially at high output currents.

This current capability of the output transistor is 40mA peak for $V_{CE} \cong 0.4V$. An internal clamping diode to the supply voltage protects the collector against overvoltages. The max. voltage at the emitter (Pin 14) must not exceed +5V. A gate, activated by one of the set or reset pulses, or by a command from the start-stop circuit will immediately switch-off the output transistor by short-circuiting its base. The external inhibitor (Pin 13) operates also via this base.

### Demagnetization Sense

As indicated in Figure 14, the output of this NPN comparator will block the output pulse, when a voltage above 0.6V is applied to Pin 13. A specific application for this function is to prevent saturation of forward converter transformers. This is indicated in Figure 15.

## Feed-Forward (Pin 16)

The basic formula for a forward converter is

$$V_{OUT} = \frac{\delta V_{IN}}{n} \quad (n=\text{transformer ratio})$$

This means that in order to keep $V_{OUT}$ at a constant value, the duty cycle $\delta$ must be made inversely proportional to the input voltage. A preregulation (feed-forward) with the function $\delta \sim 1/V_{IN}$ can ease the feedback-loop design.

This loop now only has to regulate for load variations, which require only a low feedback gain in the normal operation area. The transformer of a forward converter must be designed in such a way that it does not saturate, even under transient conditions, where the max. inductance is determined by $\delta_{MAX} \times V_{IN}$ max. A regulation of $\delta_{MAX} \sim 1/V_{IN}$ will allow for a considerable reduction or simplification of the transformer. The function of $\delta \sim 1/V_{IN}$ can be realized by using Pin 16 of the 5560.

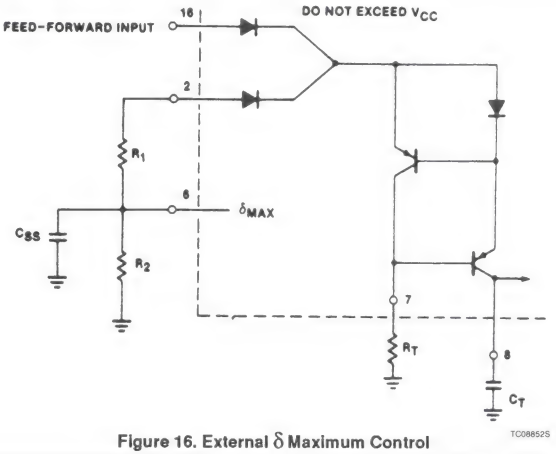



Figure 16. External δ Maximum Control

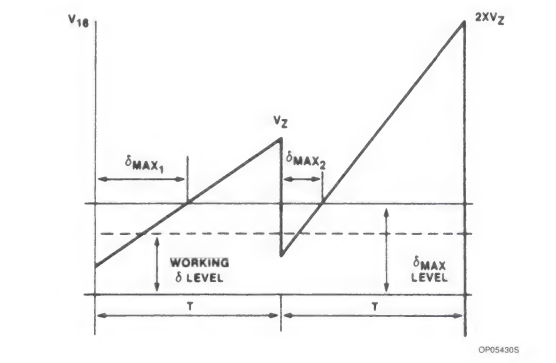



Figure 17. Feed-Forward Circuitry

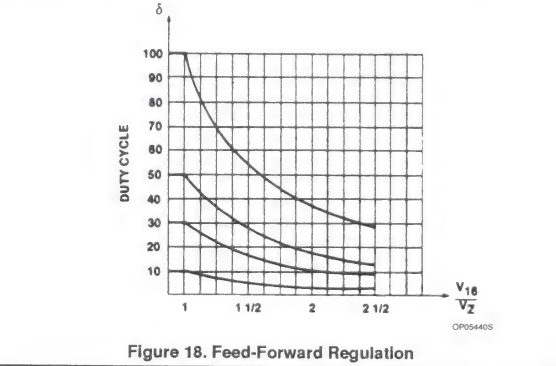



Figure 18. Feed-Forward Regulation

Figure 16 shows the electrical realization. When the voltage at Pin 16 exceeds the stabilized voltage $V_Z$ (Pin 2), it will increase the charging current for the timing capacitor on Pin 8.

The operating frequency is not affected, because the upper trip level for sawtooth increases also. Note that the $\delta_{MAX}$ voltage on Pin 6 remains constant because it is set via $V_Z$. Figure 17 visualizes the effect on $\delta_{MAX}$ and the normal operating duty cycle $\delta$. For $V_{16} = 2 \times V_Z$ these duty cycles have halved. The graph for $\delta = f(V_{16})$ is given in Figure 18. (Note: $V_{16}$ must be less than Pin 1 voltage.)

## APPLICATIONS

### 5560 Push-Pull Regulator

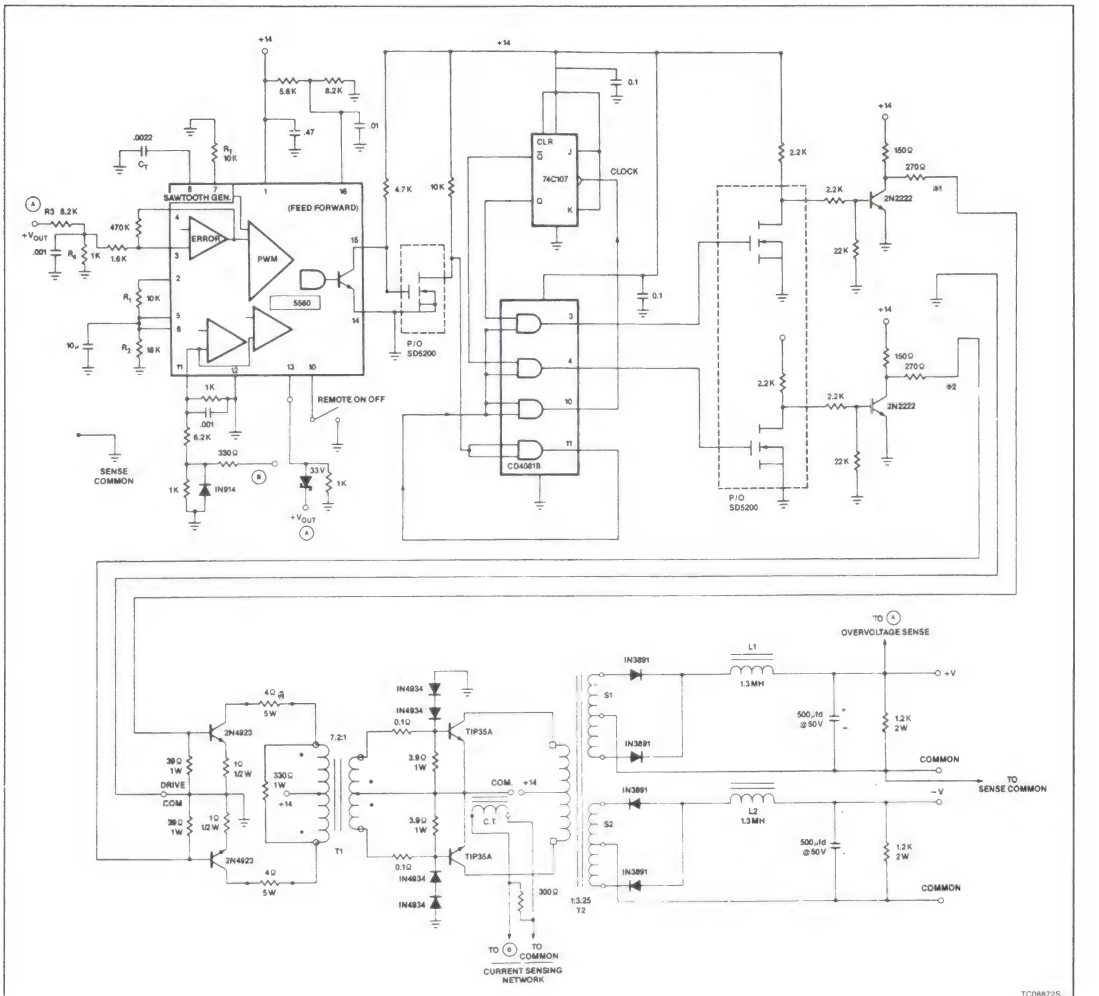
This application describes the use of the Signetics 5560 adapted to function as a push-pull switched mode regulator, as shown in Figures 19 and 20.

Input voltage range is +12 to +18V for a nominal output of +30 and –30V at a max. load current of 1A with an average efficiency of 81%.

Features include feed-forward input compensation, cycle-to-cycle drive current protection and other voltage sensing, line (to positive output) regulation < 1% for an input range of +13 to +18V and load regulation to positive output of < 3% for $\Delta I_L(+)$ of 0.1 to 1A.

The main pulse width modulator operates to 48kHz with power switching at 24kHz.

## TYPICAL APPLICATION

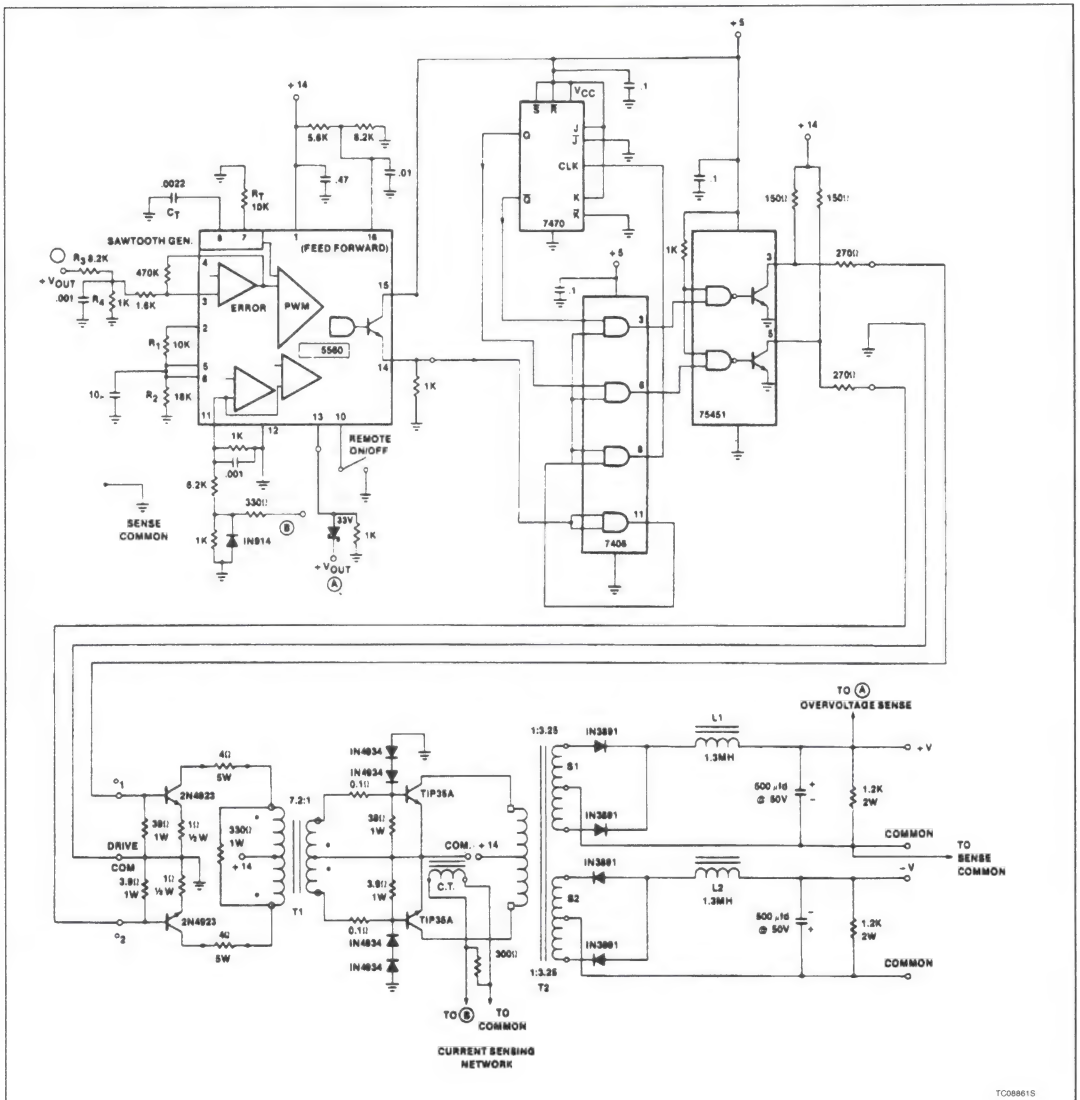



**NOTES:**
Power ground and signal ground must be kept separated
$T_1$, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622 3C8 material
C.T. = 50T #26 on Ferroxcube 2616 core (3C8) F2D bobbin
T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22,
Core = Ferroxcube 4229 3C8 material
$L_1$, $L_2$ = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

**Figure 19. 5560 Push-Pull Switch Mode Regulated Supply with CMOS Drive Conversion Logic**

# Switched–Mode Power Supply Control Circuit

# 5560




TC08861S

**NOTES:**
Power ground and signal ground must be kept separated
$T_1$, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622 3C8 material
C.T. = 50T #26 on Ferroxcube 2616 core (3C8) F2D bobbin
T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22,
Core = Ferroxcube 4229 3C8 material
$L_1$, $L_2$ = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

**Figure 20. 5560 Push-Pull Switch Mode Regulated Supply with TTL Drive Conversion Logic**

Signetics

# µA733
## Differential Video Amplifier

*Product Specification*

**Military Communications and Industrial Products**

### DESCRIPTION

The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

### FEATURES

- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10,100 and 400**
- **No frequency compensation required**

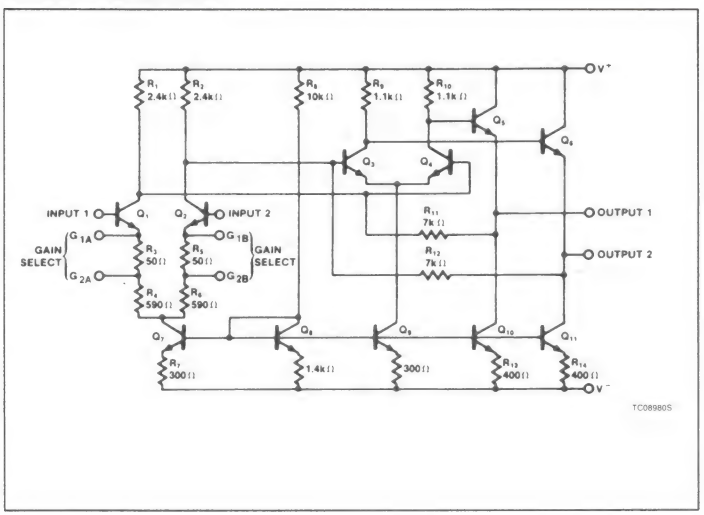
### APPLICATIONS

- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memories**
- **Video recorder systems**

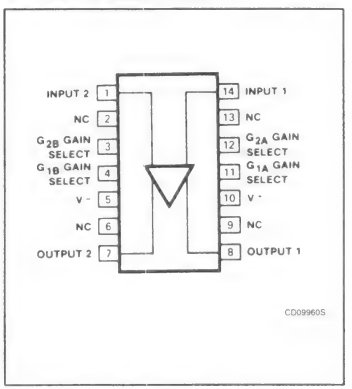
### ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING[1] | UNIT |
|---|---|---|---|
| $V_{IDR}$ | Differential input voltage | ±5 | V |
| $V_{ICR}$ | Common mode input voltage range | ±6 | V |
| $V_{CC}$ | Supply voltage | ±8 | V |
| $I_O$ | Output current | 10 | mA |
| $T_J$ | Junction temperature | +150 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $P_D$ | Power dissipation | 670 | mW |

### CIRCUIT SCHEMATIC




### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 14-Pin Ceramic DIP | µA733/BCA |

# Differential Video Amplifier — μA 733

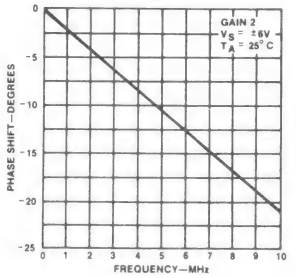
## ELECTRICAL CHARACTERISTICS $T_A$ = +25°C, $V_S$ = ±6V, VCM = 0, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = -55°C, +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | Differential voltage gain, | | | | | | | | |
| $A_{DIF1}$ | Gain 1[2] | | 300 | 400 | 500 | 200 | | 600 | V/V |
| $A_{DIF2}$ | Gain 2[3] | $R_L$ = 2kΩ, $V_O$ = $3V_{p-p}$ | 90 | 100 | 110 | 80 | | 120 | V/V |
| $A_{DIF3}$ | Gain 3[4] | | 9 | 10 | 11 | 8 | | 12 | V/V |
| | Bandwidth | | | | | | | | |
| BW1 | Gain 1[2] | | | 40 | | | | | MHz |
| BW2 | Gain 2[3] | $V_O$ = $1V_{p-p}$ | | 90 | | | | | MHz |
| BW3 | Gain 3[4] | | | 120 | | | | | MHz |
| | Rise time | | | | | | | | |
| $t_{R1}$ | Gain 1[2] | | | 10.5 | | | | | ns |
| $t_{R2}$ | Gain 2[3] | $V_O$ = $1V_{p-p}$ | | 4.5 | | | | | ns |
| $t_{R3}$ | Gain 3[4] | | | 2.5 | | | | | ns |
| | Propagation delay | | | | | | | | |
| $t_{PD1}$ | Gain 1[2] | | | 7.5 | | | | | ns |
| $t_{PD2}$ | Gain 2[3] | $V_O$ = $1V_{p-p}$ | | 6.0 | | | | | ns |
| $t_{PD3}$ | Gain 3[4] | | | 3.6 | | | | | ns |
| | Input resistance | | | | | | | | |
| $R_{IN1}$ | Gain 1[3] | | | 4.0 | | | | | kΩ |
| $R_{IN2}$ | Gain 2[3] | | 20 | 30 | | 8 | | | kΩ |
| $R_{IN3}$ | Gain 3[4] | | | 250 | | | | | kΩ |
| $C_{IN}$ | Input capacitance[3] | Gain 2 | | 2.0 | | | | | pF |
| $I_{IO}$ | Input offset current | | | 0.4 | 3.0 | | | 5.0 | μA |
| $I_{IB}$ | Input bias current | | | 9.0 | 20 | | | 40 | μA |
| $E_N$ | Input noise voltage | BW = 1kHz to 10MHz | | 12 | | | | | μVrms |
| $V_{ICR}$ | Input voltage range | | -1.0 | | +1.0 | -1.0 | | +1.0 | V |
| | Common mode rejection ratio | | | | | | | | |
| $CMRR_2$ | Gain 2 | $V_{CM}$ = ±1V | 60 | 86 | | 50 | | | dB |
| $CMRR_2$ | Gain 2 | $V_{CM}$ = ±1V, f = 5MHz | | 60 | | | | | dB |
| | Supply voltage rejection ratio | | | | | | | | |
| PSRR | Gain 2 | $\Delta V_S$ = ±0.5V | 50 | 70 | | 50 | | | dB |
| | Output offset voltage | | | | | | | | |
| $V_{IO1}$ | Gain 1 | $R_S$ = 50Ω, $R_L$ = ∞ | | 0.6 | 1.5 | | | 1.5 | V |
| $V_{IO2,3}$ | Gain 2 and 3[3, 4] | | | 0.35 | 1.0 | | | 1.2 | V |
| $V_{OCM}$ | Output common mode voltage | $R_S$ = 50Ω, $R_L$ = ∞ | 2.4 | 2.9 | 3.4 | | | | V |
| $V_{ODIF}$ | Output voltage swing differential | $R_L$ = 2kΩ | 3.0 | 4.0 | | 2.5 | | | $V_{p-p}$ |
| $I_O$ | Output sink current | $R_L$ = 1kΩ | 2.5 | 3.6 | | 2.2 | | | mA |
| $R_O$ | Output resistance | | | 20 | | | | | Ω |
| $I_S$ | Power supply current | $R_L$ = ∞ | | 18 | 24 | | | 27 | mA |

**NOTES:**
1. Operation beyond the limits of this table may impair the useful life of the device.
2. Gain select Pins $G_{1A}$ and $G_{1B}$ connected together.
3. Gain select Pins $G_{2A}$ and $G_{2B}$ connected together.
4. All gain pins open.

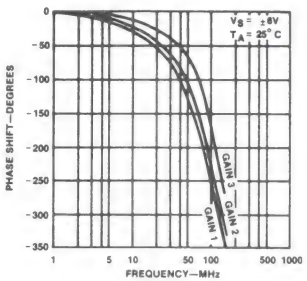
## TYPICAL PERFORMANCE CHARACTERISTICS

Phase Shift as a Function of Frequency



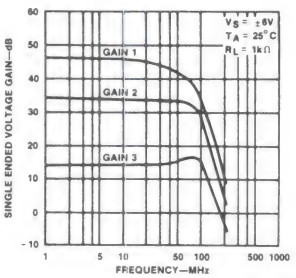

OP05620S

Phase Shift as a Function of Frequency



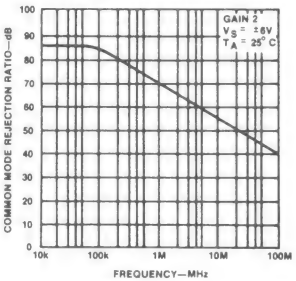

OP05630S

Voltage Gain as a Function of Frequency



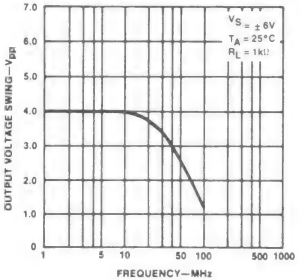

OP05640S

Common Mode Rejection Ratio as a Function of Frequency



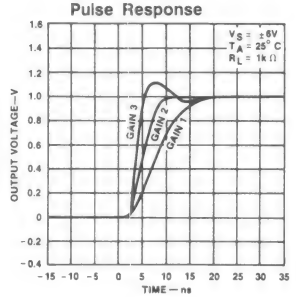

OP05650S

Output Voltage Swing as a Function of Frequency



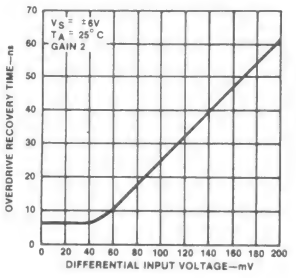

OP05660S

Pulse Response



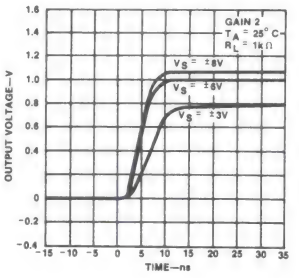

OP05670S

Differential Overdrive Recovery Time



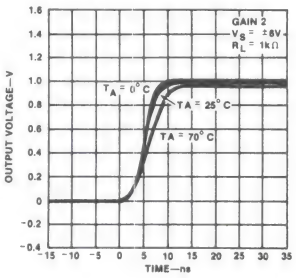

OP05680S

Pulse Response as a Function of Supply Voltage




OP05690S

Pulse Response as a Function of Temperature

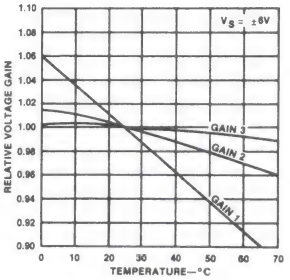



OP05700S

# Differential Video Amplifier — μA 733

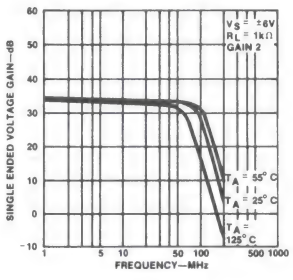
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

**Voltage Gain as a Function of Temperature**



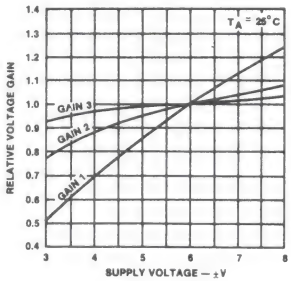

OP05710S

**Gain vs Frequency as a Function of Temperature**



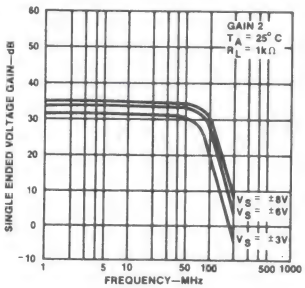

OP05720S

**Voltage Gain as a Function of Supply Voltage**



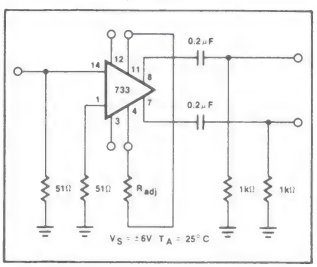

OP05730S

**Gain vs Frequency as a Function of Supply Voltage**




OP05740S

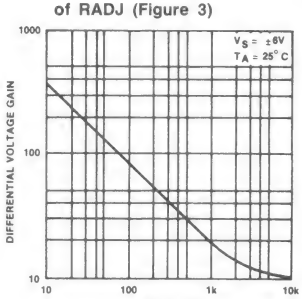
**Voltage Gain Adjust Circuit**




(Pin numbers apply to K Package)

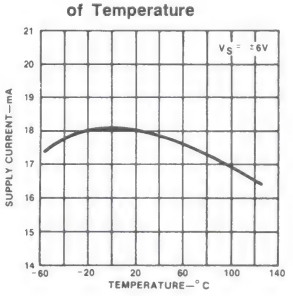
OP05750S

**Voltage Gain as a Function of RADJ (Figure 3)**



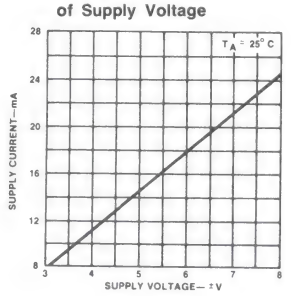

OP05760S

**Supply Current as a Function of Temperature**



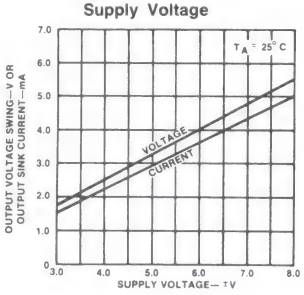

OP05770S

**Supply Current as a Function of Supply Voltage**




OP05780S

**Output Voltage and Current Swing as a Function of Supply Voltage**

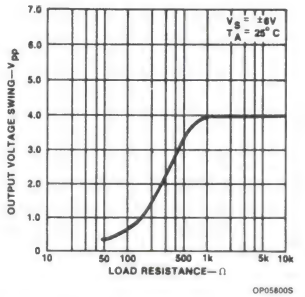



OP05790S

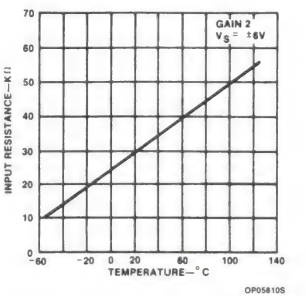
# Differential Video Amplifier — μA 733

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

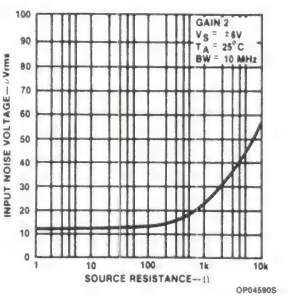
Output Voltage Swing as a Function of Load Resistance



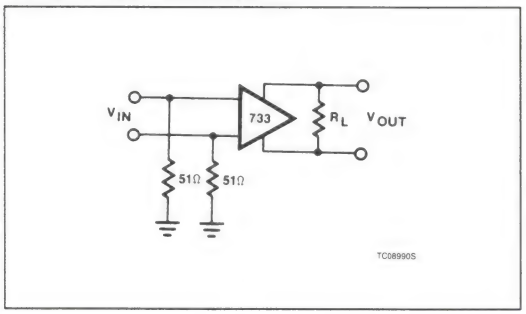

Input Resistance as a Function of Temperature

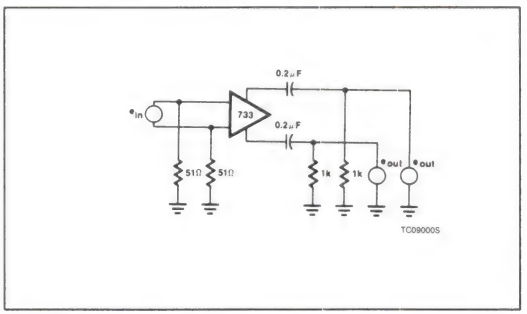



Input Noise Voltage as a Function of Source Resistance




## TYPICAL TEST CIRCUITS



Signetics

# Section 3
# Data Communications

Military Products

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Signetics

Military Microprocessor Products

# 2681
# Dual Asynchronous Receiver/Transmitter (DUART)

*Product Specification*

## DESCRIPTION

The Signetics 2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

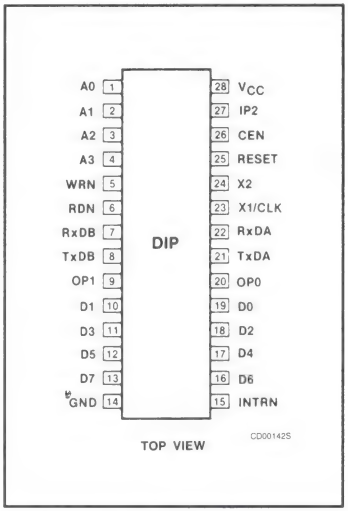
The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

## FEATURES

- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable timer/counter
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multifunction programmable 16-bit counter/timer
- Multifunction 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multifunction 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals

## 28-PIN CONFIGURATION



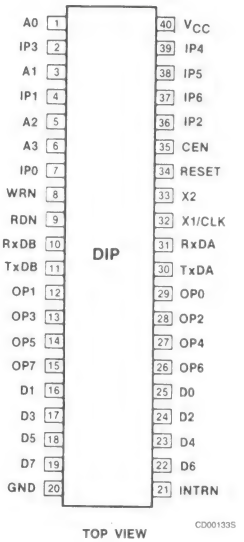

- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply

# Dual Asynchronous Receiver/Transmitter (DUART) 2681

## ORDERING INFORMATION

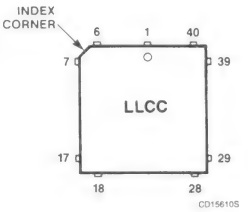
| PACKAGE | ORDER CODE |
|---|---|
| 28-Pin Cerdip | 2681/BXA |
| 40-Pin Ceramic Dip | 2681/BQA |
| 44-Pin LLCC | 2681/BUA |
| 52-Pin Flat Pack | 2681/BYA |

## 40-PIN CONFIGURATION



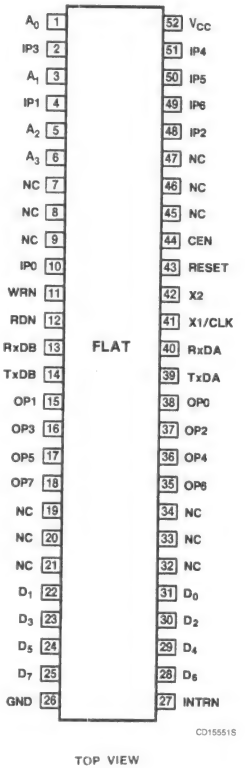

TOP VIEW

## 44-PIN CONFIGURATION




| PIN/FUNCTION | | PIN/FUNCTION | |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | AD | 24 | INTRN |
| 3 | IP3 | 25 | D6 |
| 4 | A1 | 26 | D4 |
| 5 | IP1 | 27 | D2 |
| 6 | A2 | 28 | D0 |
| 7 | A3 | 29 | OP6 |
| 8 | IP0 | 30 | OP4 |
| 9 | WRN | 31 | OP2 |
| 10 | RDN | 32 | OP0 |
| 11 | RxDB | 33 | TxDA |
| 12 | NC | 34 | NC |
| 13 | TxDB | 35 | RxDA |
| 14 | OP1 | 36 | X1/CLK |
| 15 | OP3 | 37 | X2 |
| 16 | OP5 | 38 | RESET |
| 17 | OP7 | 39 | CEN |
| 18 | D1 | 40 | IP2 |
| 19 | D3 | 41 | IP6 |
| 20 | D5 | 42 | IP5 |
| 21 | D7 | 43 | IP4 |
| 22 | GND | 44 | VCC |

## 52-PIN CONFIGURATION




TOP VIEW

# Dual Asynchronous Receiver/Transmitter (DUART) 2681

## PIN DESCRIPTION

| SYMBOL | APPLICABLE | | | | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|---|---|
| | 52 | 44 | 40 | 28 | | |
| D0–D7 | X | X | X | X | I/O | **Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit. |
| CEN | X | X | X | X | I | **Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition. |
| WRN | X | X | X | X | I | **Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal. |
| RDN | X | X | X | X | I | **Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN. |
| A0–A3 | X | X | X | X | I | **Address Inputs:** Select the DUART internal registers and ports for read/write operations. |
| RESET | X | X | X | X | I | **Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. |
| INTRN | X | X | X | X | O | **Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true. |
| X1/CLK | X | X | X | X | I | **Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). |
| X2 | X | X | X | X | I | **Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). |
| RxDA | X | X | X | X | I | **Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low. |
| RxDB | X | X | X | X | I | **Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low. |
| TxDA | X | X | X | X | O | **Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low. |
| TxDB | X | X | X | X | O | **Channel B Transmitter Serial Data Output:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit. |
| OP0 | X | X | X | X | O | **Output 0:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit. |
| OP1 | X | X | X | X | O | **Output 1:** General purpose output or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output. |
| OP2 | X | X | X | | O | **Output 2:** General purpose output or open-drain, active-Low counter/timer output, or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output. |
| OP3 | X | X | X | | O | **Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output. |
| OP4 | X | X | X | | O | **Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output. |
| OP5 | X | X | X | | O | **Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output. |
| OP6 | X | X | X | | O | **Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output. |

## PIN DESCRIPTION (Continued)

| SYMBOL | APPLICABLE 52 | 44 | 40 | 28 | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|---|---|
| OP7 | X | X | X | | O | **Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYB output. |
| IP0 | X | X | X | | I | **Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN). |
| IP1 | X | X | X | | I | **Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN). |
| IP2 | X | X | X | X | I | **Input 2:** General purpose input or counter/timer external clock input. |
| IP3 | X | X | X | | I | **Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. |
| IP4 | X | X | X | | I | **Input 4:** General purpose input or Channel B receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. |
| IP5 | X | X | X | | I | **Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. |
| IP6 | X | X | X | | I | **Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. |
| $V_{CC}$ | X | X | X | X | I | **Power Supply:** +5V supply input. |
| GND | X | X | X | X | I | **Ground:** |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature | -65 to +150 | °C |
| $V_{MAX}$ | All voltages with respect to ground[3] | -0.5 to +6.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High level input voltage (except X1/CLK) | 2.0 | | | V |
| $V_{IH}$ | High level input voltage (X1/CLK) | 4.0V | | | V |
| $V_{IL}$ | Low level input voltage | | | 0.8 | V |
| $I_{OL}$ | Low level output current | | | 2.4 | mA |
| $I_{OH}$ | High level output current | | | -400 | µA |
| $T_A$ | Operating free air temperature range[2] | -55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS $T_A$ = -55°C to +125°C,[2] $V_{CC}$ = +5.0V ± 10%[4,5,6]

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OL}$<br>$V_{OH}$ | Output Low voltage<br>Output High voltage (except o.c. outputs) | $I_{OL}$ = 2.4mA<br>$I_{OH}$ = -400µA | 2.4 | | 0.4 | V<br>V |
| $I_{IL}$ | Input leakage current | $V_I$ = 0 to $V_{CC}$ | -10 | | 10 | µA |
| $I_{OZH}$<br>$I_{OZL}$ | Data bus 3-State leakage current | $V_O$ = 0.4 to $V_{CC}$ | -10 | | 10 | µA |
| $I_{IL}$(X1) | X1/CLK Low input current | $V_I$ = 0, X2 grounded<br>$V_I$ = 0, X2 floated | -4.0<br>-3.0 | -2.0<br>-1.5 | 0.0<br>0.0 | mA<br>mA |
| $I_{IH}$(X1) | X1/CLK High input current | $V_I$ = $V_{CC}$, X2 grounded<br>$V_I$ = $V_{CC}$, X2 floated | -1.0<br>0.0 | 0.2<br>3.5 | 1.0<br>10.0 | mA<br>mA |
| $I_{IL}$(X2)<br>$I_{IH}$(X2) | X2 Low input current<br>X2 High input current | $V_I$ = 0, X1/CLK floated<br>$V_I$ = $V_{CC}$, X1/CLK floated | -100<br>0.0 | -30<br>+30 | 0.0<br>100 | µA<br>µA |
| $I_{OH}$ | Open-drain output leakage current | $V_O$ = 0.4 to $V_{CC}$ | -10 | | 10 | µA |
| $I_{CC}$ | Power supply current | $V_{CC}$ = 5.5V, $T_A$ = 25 to 125°C<br>$V_{CC}$ = 5.5V, $T_A$ = -55°C | | | 150<br>175 | mA<br>mA |
| $C_{IN}$[11] | Input | | | | 20 | pF |
| $C_{OUT}$[11] | Output | | | | 20 | pF |

## AC CHARACTERISTICS $T_A$ = -55°C to +125°C[2], $V_{CC}$ = +5.0V ± 10%[4,5,6,7]

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **Reset Timing (Figure 1)** | | | | | |
| $t_{RES}$ | RESET pulse width | 1.0 | | | µs |
| **Bus Timing (Figure 2)[8]** | | | | | |
| $t_{AS}$ | A0-A3 setup time to RDN, WRN Low | 10 | | | ns |
| $t_{AH}$ | A0-A3 hold time from RDN, WRN High | 0 | | | ns |
| $t_{CS}$ | CEN setup time to RDN, WRN Low | 0 | | | ns |
| $t_{CH}$ | CEN hold time from RDN, WRN High | 0 | | | ns |
| $t_{RW}$ | WRN, RDN pulse width | 225 | | | ns |
| $t_{DD}$ | Data valid after RDN Low | | | 175 | ns |
| $t_{DF}$ | Data bus floating after RDN High | | | 100 | ns |
| $t_{DS}$ | Data setup time before WRN High | 100 | | | ns |
| $t_{DH}$ | Data hold time after WRN High | 20 | | | ns |
| $t_{RWD}$ | High time between READs and/or WRITE[9,10] | 200 | | | ns |
| **Port Timing (Figure 3)[8]** | | | | | |
| $t_{PS}$ | Port input setup time before RDN Low | 0 | | | ns |
| $t_{PH}$ | Port input hold time after RDN High | 0 | | | ns |
| $t_{PD}$ | Port output valid after WRN High | | | 400 | ns |
| **Interrupt Timing (Figure 4)** | | | | | |
| $t_{IR}$ | INTRN (or OP3-OP7 when used as interrupts) negated from: | | | | |
| | Read RHR (RxRDY/FFULL interrupt) | | | 300 | ns |
| | Write THR (TxRDY interrupt) | | | 300 | ns |
| | Reset command (delta break interrupt) | | | 300 | ns |
| | Stop C/T command (counter interrupt) | | | 300 | ns |
| | Read IPCR (input port change interrupt) | | | 300 | ns |
| | Write IMR (clear of interrupt mask bit) | | | 300 | ns |

## AC CHARACTERISTICS (Continued) $T_A = -55°C$ to $+125°C$[2], $V_{CC} = +5.0V \pm 10\%$[4,5,6,7]

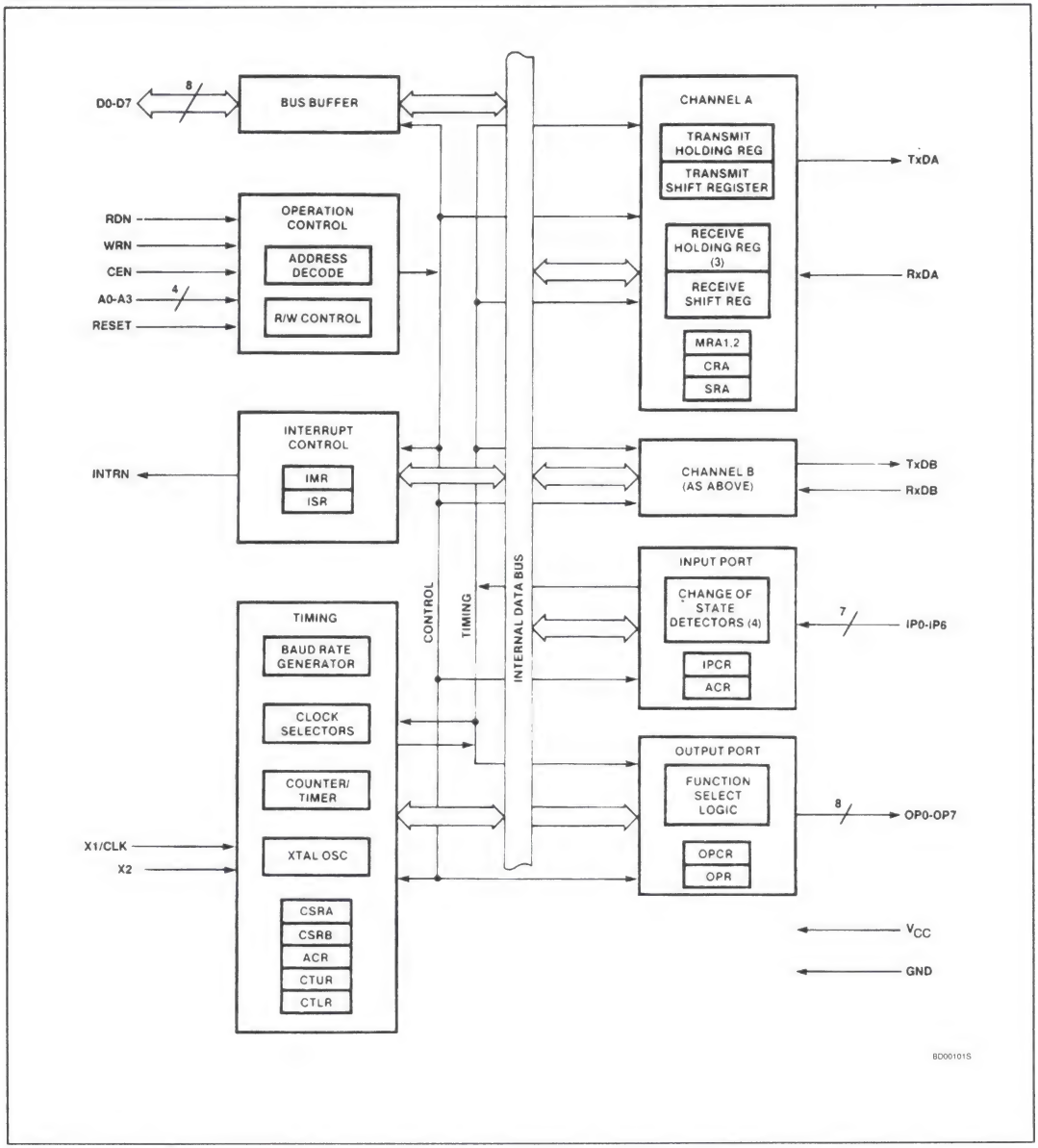
| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **Clock Timing (Figure 5)** | | | | | |
| $t_{CLK}$ | X1/CLK High or Low time | 100 | | | ns |
| $f_{CLK}$ | X1/CLK frequency | 2.0 | 3.6864 | 4.0 | MHz |
| $t_{CTC}$ | CTCLK (IP2) High or Low time | 100 | | | ns |
| $f_{CTC}$ | CTCLK (IP2) frequency | 0 | | 4.0 | MHz |
| $t_{RX}$[12] | RxC High or Low time | 220 | | | ns |
| $f_{RX}$[12] | RxC frequency (16X) | 0 | | 2.0 | MHz |
| | (1X) | 0 | | 1.0 | MHz |
| $t_{TX}$[12] | TxC High or Low time | 220 | | | ns |
| $f_{TX}$[12] | TxC frequency (16X) | 0 | | 2.0 | MHz |
| | (1X) | 0 | | 1.0 | MHz |
| **Transmitter Timing (Figure 6)** | | | | | |
| $t_{TXD}$[12] | TxD output delay from TxC Low | | | 350 | ns |
| $t_{TCS}$[12] | Output delay from TxC Low to TxD data output | 0 | | 150 | ns |
| **Receiver Timing (Figure 7)** | | | | | |
| $t_{RXS}$[12] | RxD data setup time to RxC High | 240 | | | ns |
| $t_{RXH}$[12] | RxD data hold time from RxC High | 200 | | | ns |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of $\leq$ 20ns. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. Test condition for outputs: $C_L = 150pF$, except interrupt outputs. Test condition for interrupt outputs: $C_L = 50pF$, $R_L = 21.7k\Omega$ to $V_{CC}$.
8. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
9. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for $t_{RWD}$ to guarantee that any status register changes are valid.
10. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
11. This parameter is guaranteed, but not tested.
12. This parameter is not applicable to the 28-Pin device.

# Dual Asynchronous Receiver/Transmitter (DUART) 2681

## BLOCK DIAGRAM



# Dual Asynchronous Receiver/Transmitter (DUART) 2681

## BLOCK DIAGRAM

The 2681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the block diagram.

### Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

### Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

### Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

### Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, both X1 and X2 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4k baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

### Communications Channels A and B

Each communications channel of the 2681 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

### Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address D16. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

### Output Port

The 8-bit multipurpose port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address E16 with the accompanying data specifying the bits to be set (1 = set, 0 = no change).

Likewise, a bit is reset by a write at address F16 with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

## OPERATION

### Transmitter

The 2681 is conditioned to transmit data when the transmitter is enabled through the command register. The 2681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR.

If the transmitter is disabled, it continues operating until the character currently being trans-

mitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

## Receiver

The 2681 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7 1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, overrun error and received break state (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

**Table 1. 2681 Register Addressing**

| A3 | A2 | A1 | A0 | READ (RDN = 0) | WRITE (WRN = 0) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Mode Register A (MR1A, MR2A) | Mode Register A (MR1A, MR2A) |
| 0 | 0 | 0 | 1 | Status Register A (SRA) | Clock Select Register A (CSRA) |
| 0 | 0 | 1 | 0 | *Reserved* | Command Register A (CRA) |
| 0 | 0 | 1 | 1 | Rx Holding Register A (RHRA) | Tx Holding Register A (THRA) |
| 0 | 1 | 0 | 0 | Input Port Change Register (IPCR) | Aux. Control Register (ACR) |
| 0 | 1 | 0 | 1 | Interrupt Status Register (ISR) | Interrupt Mask Register (IMR) |
| 0 | 1 | 1 | 0 | Counter/Timer Upper (CTU) | C/T Upper Register (CRUR) |
| 0 | 1 | 1 | 1 | Counter/Timer Lower (CTL) | C/T Lower Register (CTLR) |
| 1 | 0 | 0 | 0 | Mode Register B (MR1B, MR2B) | Mode Register B (MR1B, MR2B) |
| 1 | 0 | 0 | 1 | Status Register B (SRB) | Clock Select Register B (CSRB) |
| 1 | 0 | 1 | 0 | *Reserved* | Command Register B (CRB) |
| 1 | 0 | 1 | 1 | Rx Holding Register B (RHRB) | Tx Holding Register B (THRB) |
| 1 | 1 | 0 | 0 | *Reserved* | *Reserved* |
| 1 | 1 | 0 | 1 | Input Port | Output Port Conf. Register (OPCR) |
| 1 | 1 | 1 | 0 | Start Counter Command | Set Output Port Bits Command |
| 1 | 1 | 1 | 1 | Stop Counter Command | Reset Output Port Bits Command |

## Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

## PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

## MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

**MR1A[7] – Channel A Receiver Request-to-Send Control**

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

**MR1A[6] – Channel A Receiver Interrupt Select**

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

**MR1A[5] – Channel A Error Mode Select**

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

**MR1A[4:3] – Channel A Parity Mode Select**

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] + 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

**MR1A[2] – Channel A Parity Type Select**

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

**MR1A[1:0] – Channel A Bits Per Character Select**

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

## Table 2. Register Bit Formats

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 BIT 3 | BIT 2 | BIT 1 BIT 0 |
|---|---|---|---|---|---|---|
| | RxRTS CONTROL | RxINT SELECT | ERROR MODE | PARITY MODE | PARITY TYPE | BITS PER CHARACTER |
| MR1A MR1B | 0 = No<br>1 = Yes | 0 = RxRDY<br>1 = FFULL | 0 = Char<br>1 = Block | 00 = With Parity<br>01 = Force Parity<br>10 = No Parity<br>11 = Multidrop Mode | 0 = Even<br>1 = Odd | 00 = 5<br>01 = 6<br>10 = 7<br>11 = 8 |

| | BIT 7 BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| | CHANNEL MODE | TxRTS CONTROL | CTS ENABLE Tx | STOP BIT LENGTH* | | | |
| MR2A MR2B | 00 = Normal<br>01 = Auto-Echo<br>10 = Local loop<br>11 = Remote loop | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = 0.563<br>1 = 0.625<br>2 = 0.688<br>3 = 0.750 | 4 = 0.813<br>5 = 0.875<br>6 = 0.938<br>7 = 1.000 | 8 = 1.563<br>9 = 1.625<br>A = 1.688<br>B = 1.750 | C = 1.813<br>D = 1.875<br>E = 1.938<br>F = 2.000 |

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

| | BIT 7 BIT 6 BIT 5 BIT 4 | BIT 3 BIT 2 BIT 1 BIT 0 |
|---|---|---|
| | RECEIVER CLOCK SELECT | TRANSMITTER CLOCK SELECT |
| CSRA CSRB | See Text | See Text |

| | BIT 7 | BIT 6 BIT 5 BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|
| | | MISCELLANEOUS COMMANDS | DISABLE Tx | ENABLE Tx | DISABLE Rx | ENABLE Rx |
| CRA CRB | Not used – must be 0 | See Text | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | RECEIVED BREAK* | FRAMING ERROR* | PARITY ERROR* | OVERRUN ERROR | TxEMT | TxRDY | FFULL | RxRDY |
| SRA SRB | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 BIT 2 | BIT 1 BIT 0 |
|---|---|---|---|---|---|---|
| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 |
| OPCR | 0 = OPR[7]<br>1 = TxRDYB | 0 = OPR[6]<br>1 = TxRDYA | 0 = OPR[5]<br>1 = RxRDY/ FFULLB | 0 = OPR[4]<br>1 = RxRDY/ FFULLA | 00 = OPR[3]<br>01 = C/T OUTPUT<br>10 = TxCB(1x)<br>11 = RxCB(1x) | 11 = OPR[2]<br>01 = TxCA(16x)<br>10 = TxCA(1x)<br>11 = RxCA(1x) |

| | BIT 7 | BIT 6 BIT 5 BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|
| | BRG SET SELECT | COUNTER/TIMER MODE AND SOURCE | DELTA IP 3 INT | DELTA IP 2 INT | DELTA IP 1 INT | DELTA IP 0 INT |
| ACR | 0 = set 1<br>1 = set 2 | See Table 4 | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On |

**Table 2. Register Bit Formats** (Continued)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | DELTA IP 3 | DELTA IP 2 | DELTA IP 1 | DELTA IP 0 | IP 3 | IP 2 | IP 1 | IP 0 |
| IPCR | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | INPUT PORT CHANGE | DELTA BREAK B | RxRDY/ FFULLB | TxRDYB | COUNTER READY | DELTA BREAK A | RxRDY/ FFULLA | TxRDYA |
| ISR | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | IN. PORT CHANGE INT | DELTA BREAK B INT | RxRDY/ FFULLB INT | TxRDYB INT | COUNTER READY INT | DELTA BREAK A INT | RxRDY/ FFULLA INT | TxRDYA INT |
| IMR | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | C/T[15] | C/T[14] | C/T[13] | C/T[12] | C/T[11] | C/T[10] | C/T[9] | C/T[8] |
| CTUR | | | | | | | | |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | C/T[7] | C/T[6] | C/T[5] | C/T[4] | C/T[3] | C/T[2] | C/T[1] | C/T[0] |
| CTLR | | | | | | | | |

## MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

**MR2A[7:6] – Channel A Mode Select**

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

**MR2A[5] – Channel A Transmitter Request-to-Send Control**
This bit controls the deactivation of the RTSAN output (OPO) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Verify the message is sent by waiting until the transmit ready status (TxRDY) is asserted. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

**MR2A[4] – Channel A Clear-to-Send Control**
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes Low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

**MR2A[3:0] – Channel A Stop Bit Length Select**
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of .563 TO 1 AND .563 to 2 bits. In increments of 0.625 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1.0625 to 2 stop bits can be programmed in increments of .0625 bit.

The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled) in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

## MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

## MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode registers 1 and 2 are identical to the bit definitions for MRA and MR2A except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## CSRA – Channel A Clock Select Register

**CSRA[7:4] – Channel A Receiver Clock Select**
This field selects the baud rate clock for the Channel A receiver as follows:

| CSRA[7:4] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 0000 | 50 | 75 |
| 0001 | 110 | 110 |
| 0010 | 134.5 | 134.5 |
| 0011 | 200 | 150 |
| 0100 | 300 | 300 |
| 0101 | 600 | 600 |
| 0110 | 1,200 | 1,200 |
| 0111 | 1,050 | 2,000 |
| 1000 | 2,400 | 2,400 |
| 1001 | 4,800 | 4,800 |
| 1010 | 7,200 | 1,800 |
| 1011 | 9,600 | 9,600 |
| 1100 | 38.4k | 19.2k |
| 1101 | Timer | Timer |
| 1110 | IP4–16X | IP4–16X |
| 1111 | IP4–1X | IP4–1X |

The receiver clock is always a 16X clock except for CSRA[7] = 1111.

**CSRA[3:0] – Channel A Transmitter Clock Select**
This field selects the baud rate clock for the Channel A transmitter. The field definition is as per CSR[7:4] except as follows:

| CSRA[3:0] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 1110 | IP3–16X | IP3–16X |
| 0111 | IP3–1X | IP3–1X |

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

## CSRB – Channel B Clock Select Register

**CSRB[7:4] – Channel B Receiver Clock Select**
This field selects the baud rate clock for the Channel B transmitter. The field definition is as per CSRA[7:4] except as follows:

| CSRB[7:4] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 1110 | IP6–16X | IP6–16X |
| 0111 | IP6–1X | IP6–1X |

The transmitter clock is always a 16X clock except for CSRB[7:4] = 1111.

**CSRB[3:0] – Channel B Transmitter Clock Select**
This field selects the baud rate clock for the Channel B transmitter. The field definition is as per CSRA[7:4] except as follows:

| CSRB[3:4] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 1110 | IP5–16X | IP5–16X |
| 0111 | IP5–1X | IP5–1X |

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

## CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

**CRA[6:4] – Channel A Miscellaneous Command**
The encoded value of this field may be used to specify a single command as follows:

| CRA[6:4] | COMMAND |
|---|---|
| 000 | No command. |
| 001 | Reset MR pointer. Causes the Channel A MR pointer to point to MR1. |

010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.

100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

**CRA[3] – Disable Channel A Transmitter**
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

**CRA[2] – Enable Channel A Transmitter**
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

**CRA[1] – Disable Channel A Receiver**
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

**CRA[0] – Enable Channel A Receiver**
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

## CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## SRA – Channel A Status Register

**SRA[7] – Channel A Received Break**
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

**SRA[6] – Channel A Framing Error**
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first bit position.

**SRA[5] – Channel A Parity Error**
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

**SRA[4] – Channel A Overrun Error**
This bit, when set indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

**SRA[3] – Channel A Transmitter Empty (TxEMTA)**
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

**SRA[2] – Channel A Transmitter Ready (TxRDYA)**
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

**SRA[1] – Channel A FIFO Full (FFULLA)**
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

**SRA[0] – Channel A Receiver Ready (RxRDYA)**
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

## SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## OPCR – Output Port Configuration Register

**OPCR[7] – OP7 Output Select**
This bit programs the OP7 output to provide one of the following:

– The complement of OPR[7].
– The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

**OPCR[6] – OP6 Output Select**
This bit programs the OP6 output to provide one of the following:
– The complement of OPR[6].
– The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

**OPCR[5] – OP5 Output Select**
This bit programs the OP5 output to provide one of the following:
– The complement of OPR[5].
– The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

**OPCR[4] – OP4 Output Select**
This field programs the OP4 output to provide one of the following:
– The complement of OPR[4].
– The Channel B transmitter interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

**OPCR[3:2] – OP3 Output Select**
This bit programs the OP3 output to provide one of the following:
– The complement of OPR[3].
– The counter/timer output, in which case OP3 acts as an Open-Collector output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
– The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
– The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

**OPCR[1:0] – OP2 Output Select**
This field programs the OP2 output to provide one of the following:
– The complement of OPR[2].
– The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
– The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
– The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

## ACR – Auxiliary Control Register

**ACR[7] – Baud Rate Generator Set Select**
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 3.

**ACR[6:4] – Counter/Timer Mode And Clock Source Select**
this field selects the operating mode of the counter/timer and its clock source as shown in Table 4.

**ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable**
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

## IPCR – Input Port Change Register

**IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State**
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

**IPCR[3:0] – IP3, IP2, IP1, IP0 Current State**
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

## ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to $00_{16}$ when the DUART is reset.

**ISR[7] – Input Port Change Status**
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

**ISR[6] – Channel B Change In Break**
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

**ISR[5] – Channel B Receiver Ready or FIFO Full**
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

**ISR[4] – Channel B Transmitter Ready**
This bit is a duplicate of TxRDYB (SRB[2]).

**ISR[3] – Counter Ready.**
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

**ISR[2] – Channel A Change in Break**
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

**ISR[1] – Channel A Receiver Ready Or FIFO Full**
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. IF after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

**ISR[0] – Channel A Transmitter Ready**
This bit is a duplicate of TxRDYA (SRA[2]).

## IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

## CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is $0002_{16}$. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the CT generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR.

If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = 1111). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

On power up and after reset, the timer/counter runs in timer mode and can only be restarted. Because it cannot be shut off or stopped, and runs continuously in timer mode, it is recommended that at initialization, the output port (OP3) should be masked off through the OPCR[3:2] = 00 until the T/C is programmed to the desired operational state.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a counter command. Upon reaching terminal count ($0000_{16}$), the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU.

It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

**Table 3. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz**

| NORMAL RATE (BAUD) | ACTUAL 16x CLOCK (kHz) | ERROR (%) |
|---|---|---|
| 50 | 0.8 | 0 |
| 75 | 1.2 | 0 |
| 110 | 1.759 | -0.069 |
| 134.5 | 2.153 | 0.059 |
| 150 | 2.4 | 0 |
| 200 | 3.2 | 0 |
| 300 | 4.8 | 0 |
| 600 | 9.6 | 0 |
| 1050 | 16.756 | -0.260 |
| 1200 | 19.2 | 0 |
| 1800 | 28.8 | 0 |
| 2000 | 32.056 | 0.175 |
| 2400 | 38.4 | 0 |
| 4800 | 76.8 | 0 |
| 7200 | 115.2 | 0 |
| 9600 | 153.6 | 0 |
| 19.2k | 307.2 | 0 |
| 38.4k | 614.4 | 0 |

**NOTE:** Duty cycle of 16x clock is 50% ± 1%.

**Table 4. ACR 6:4 Field Definition**

| ACR 6:4 | MODE | CLOCK SOURCE |
|---|---|---|
| 000 | Counter | External (IP2) |
| 001 | Counter | TxCA – 1x clock of Channel A transmitter |
| 010 | Counter | TxCB – 1x clock of Channel B transmitter |
| 011 | Counter | Crystal or external clock (x1/CLK) divided by 16 |
| 100 | Timer | External (IP2) |
| 101 | Timer | External (IP2) divided by 16 |
| 110 | Timer | Crystal or external clock (x1/CLK) |
| 111 | Timer | Crystal or external clock (x1/CLK) divided by 16 |

## TIMING DIAGRAMS

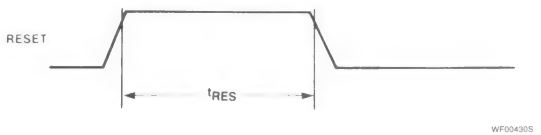



Figure 1. Reset Timing

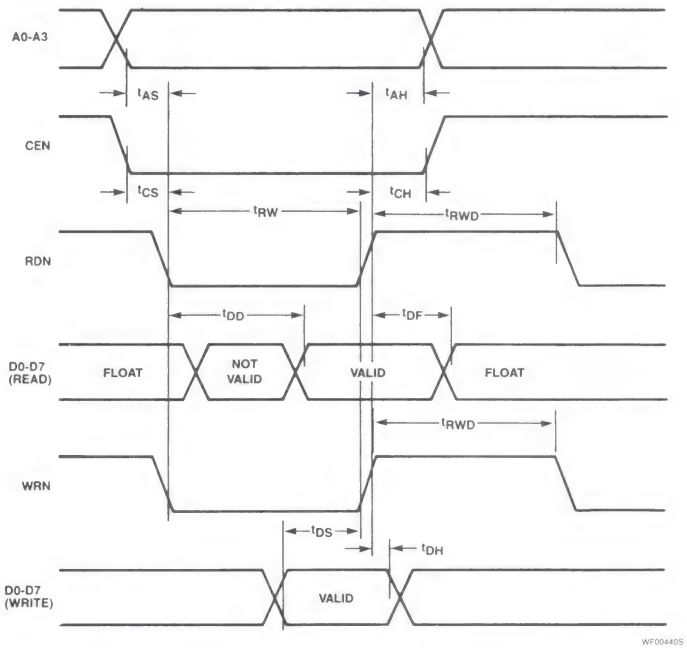



Figure 2. Bus Timing

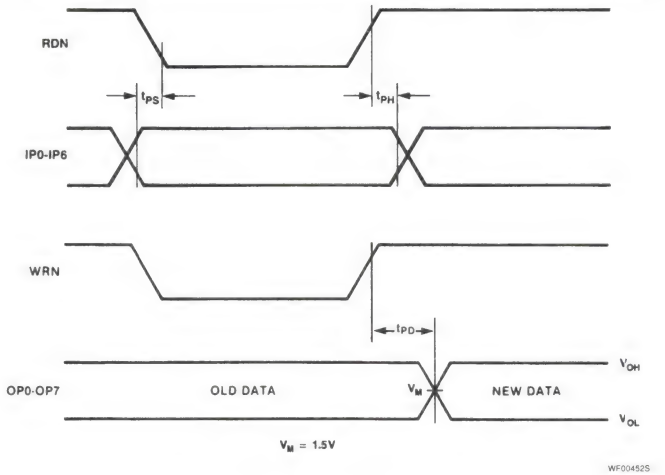
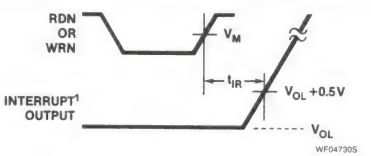



Figure 3. Port Timing




NOTES:
1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, $V_M$, to a point 0.5V above $V_{OL}$. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing

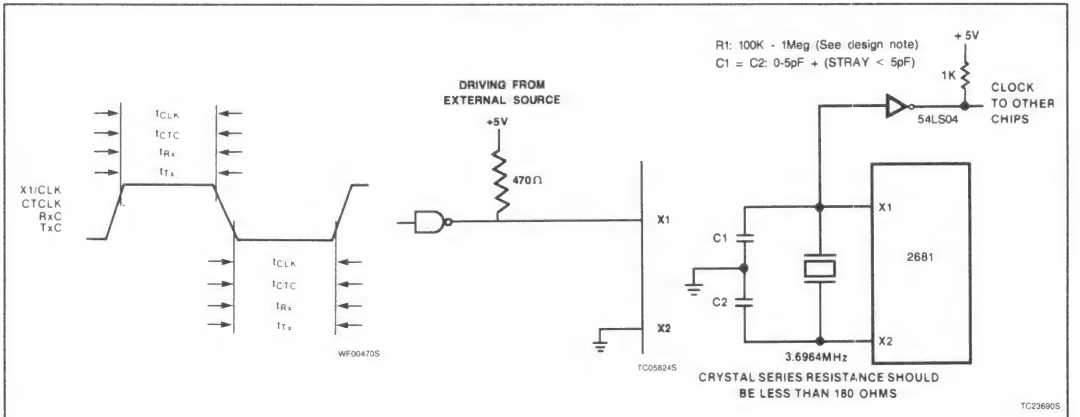



Figure 5. Clock Timing

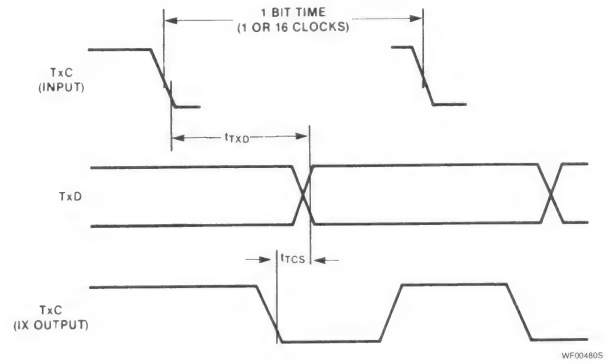



Figure 6. Transmit

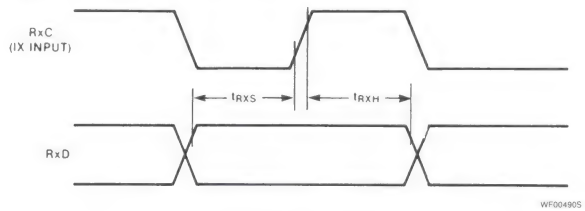
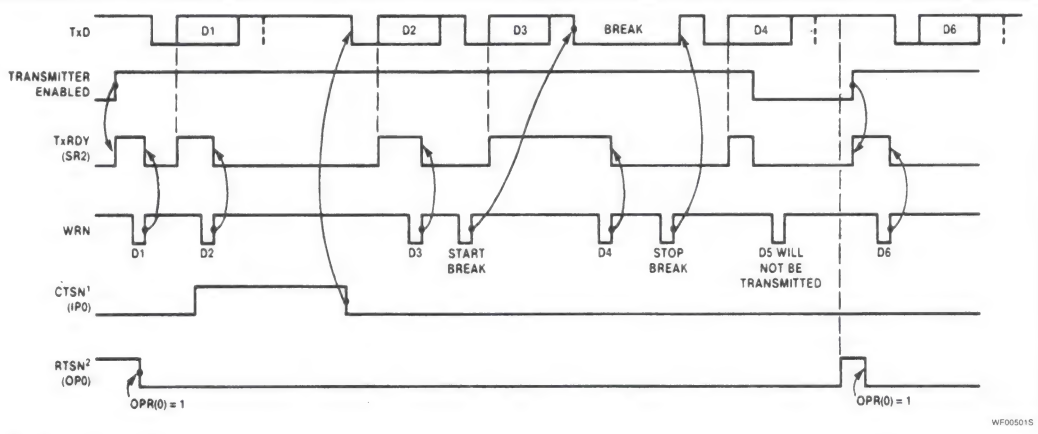
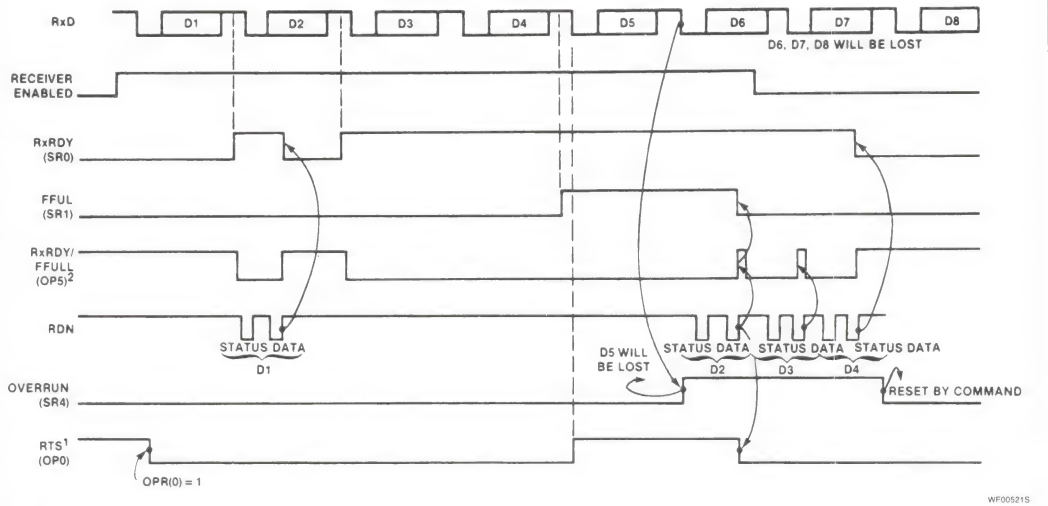



Figure 7. Receive




**NOTES:**
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing




**NOTES:**
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

**Figure 9. Receiver Timing**

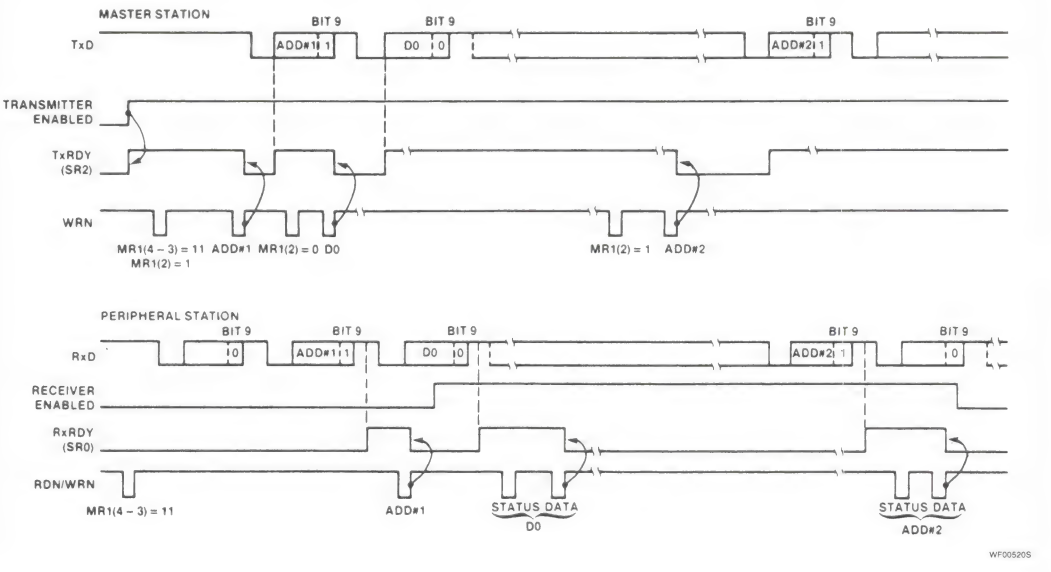



**Figure 10. Wake-Up Mode**

Signetics

# 2691
## Universal Asynchronous Receiver/Transmitter (UART)

*Objective Specification*

**Military Communications and Industrial Products**

### DESCRIPTION

The Signetics 2691 Universal Asynchronous Receiver/Transmitter (UART) is a single-chip CMOS-LSI communications device that provides a full-duplex asynchronous receiver/transmitter in a single 24-pin Skinny DIP. It is fabricated with Signetics CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of the receiver and transmitter can be selected independently as one of 18 fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes.

The UART is fully TTL compatible and operates from a single +5V power supply.

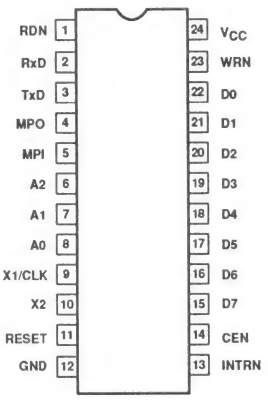
### ORDERING INFORMATION

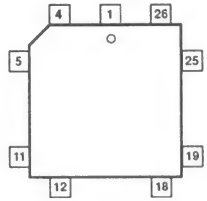
| DESCRIPTION | ORDER CODE |
|---|---|
| 24–Pin Ceramic DIP | 2691/BLA |
| 28–Pin LLCC | 2691/B3A |

### FEATURES

- Full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud
  - One user-defined rate derived from programmable timer/counter
  - External 1X or 16X clock
- Parity, framing, and overrun detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote Loopback
- Multi-function programmable 16-bit counter/timer
- Single interrupt output with seven maskable interrupting conditions
- On-chip crystal oscillator
- Low power mode
- TTL compatible
- Single +5V power supply

### PIN CONFIGURATIONS

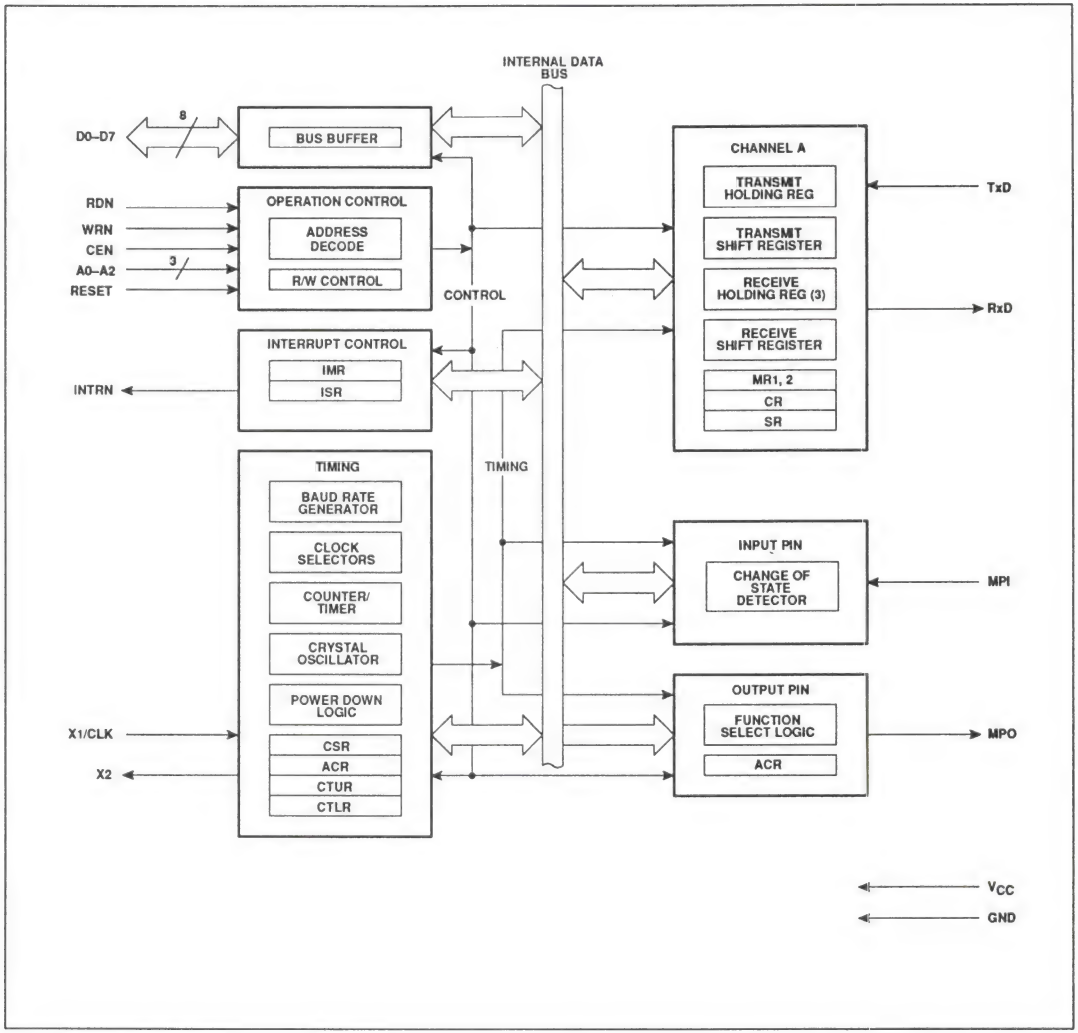



| Pin | Symbol | Pin | Symbol |
|---|---|---|---|
| 1 | $V_{CC}$ | 15 | GND |
| 2 | RDN | 16 | INTRN |
| 3 | RxD | 17 | CEN |
| 4 | TxD | 18 | D7 |
| 5 | MPO | 19 | D6 |
| 6 | MPI | 20 | D5 |
| 7 | NC | 21 | D4 |
| 8 | NC | 22 | D3 |
| 9 | A2 | 23 | NC |
| 10 | A1 | 24 | D2 |
| 11 | A0 | 25 | D1 |
| 12 | X1/CLK | 26 | NC |
| 13 | X2 | 27 | D0 |
| 14 | RESET | 28 | WRN |

# Universal Asynchronous Receiver/Transmitter (UART) 2691

## BLOCK DIAGRAM



## PIN DESCRIPTION

| MNEMONIC | PIN NO. | | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|
| | DIP | LLCC | | |
| D0–D7 | 22–15 | 27, 25, 24, 22–18 | I/O | **Data Bus:** Active-high 8-bit bidirectional 3-state data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is high, the data bus is in the 3-state condition. |
| CEN | 14 | 17 | I | **Chip Enable:** Active-low input. When low, data transfers between the CPU and the UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A2 inputs. When CEN is high, the UART is effectively isolated from the data bus and D0–D7 are placed in the 3-state condition. |
| WRN | 28 | 28 | I | **Write Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the data bus to be transferred to the register selected by A0–A2. The transfer occurs on the trailing (rising) edge of the signal. |
| RDN | 1 | 2 | I | **Read Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the register selected by A0–A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN. |
| A0–A2 | 8–6 | 11–9 | I | **Address Inputs:** Active-high address inputs to select the UART registers for read/write operations. |
| RESET | 11 | 14 | I | **Reset:** Master reset. A high on this pin clears the status register (SR), the interrupt mask register (IMR), and the interrupt status register (ISR), sets the mode register pointer to MR1, and places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (high) state. |
| INTRN | 13 | 16 | O | **Interrupt Request:** This active-low output is asserted upon occurrence of one or more of seven maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s). This open–drain output requires a pull-up resistor. |
| X1/CLK | 9 | 12 | I | **Crystal 1:** Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip. |
| X2 | 10 | 13 | I | **Crystal 2:** Connection for other side of crystal. If an external source is used instead of a crystal, this connection should be open. (See Figure 5) |
| RxD | 2 | 3 | I | **Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock. |
| TxD | 3 | 4 | O | **Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (high) condition when the transmitter is idle or disabled and when the UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock. |
| MPO | 4 | 5 | O | **Multi-Purpose Output:** One of the following functions can be selected for this output pin by programming the auxiliary control register:<br>**RTSN –** Request to send active-low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full.<br>**C/TO –** The counter/timer output.<br>**TxC1X –** The 1X clock for the transmitter.<br>**TxC16X –** The 16X clock for the transmitter.<br>**RxC1X –** The 1X clock for the receiver.<br>**RxC16X –** The 16X clock for the receiver.<br>**TxRDY –** The transmitter holding register empty signal. Active-low output.<br>**RxRDY/FFULL –** The receiver FIFO not empty/full signal. Active-low output. |
| MPI | 5 | 6 | I | **Multi-Purpose Input:** This pin can serve as an input for one of the following functions:<br>**GPI –** General purpose input. The current state of the pin can be determined by reading the ISR.<br>**CTSN –** Clear-to-send active-low input.<br>**CTCLK –** Counter/timer external clock input.<br>**RTCLK –** Receiver and/or transmitter external clock input. This may be a 1X or 16X clock as programmed by CSR[3:0] or CSR[7:4]. |
| $V_{CC}$ | 24 | 1 | I | **Power Supply:** +5V supply input. |
| GND | 12 | 15 | I | **Ground** |

# Universal Asynchronous Receiver/Transmitter (UART) 2691

## BLOCK DIAGRAM

As shown in the block diagram, the UART consists of: data bus buffer, interrupt control, operation control, timing, receiver and transmitter.

### Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and UART.

### Interrupt Control

A single interrupt output (INTRN) is provided which may be asserted upon occurrence of any of the following internal events:

- Transmit holding register ready
- Transmit shift register empty
- Receive holding register ready or FIFO full
- Change in break received status
- Counter reached terminal count
- Change in MPI input
- Assertion of MPI input

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR can be programmed to select only certain of the above conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. However, the bits of the ISR are not masked by the IMR.

### Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers 1 and 2 are accessed via an auxiliary pointer. The pointer is set to MR1 by RESET or by issuing a reset pointer command via the command register. Any read or write of the mode register while the pointer is at MR1 switches the pointer to MR2. the pointer then remains at MR2 so that subsequent accesses are to MR2, unless the pointer is reset to MR1 as described above.

**Table 1. Register Addressing**

| A2 | A1 | A0 | READ (RDN = 0) | WRITE (WRN = 0) |
|---|---|---|---|---|
| 0 | 0 | 0 | MR1, MR2 | MR1, MR2 |
| 0 | 0 | 1 | SR | CSR |
| 0 | 1 | 0 | Reserved* | CR |
| 0 | 1 | 1 | RHR | THR |
| 1 | 0 | 0 | Reserved* | ACR |
| 1 | 0 | 1 | ISR | IMR |
| 1 | 1 | 0 | CTU | CTUR |
| 1 | 1 | 1 | CTL | CTLR |

NOTE;
*Reserved registers should never be read during operation since they are reserved for internal diagnostics.
ACR = Auxiliary control register
CR = Command register
CSR = Clock select register
CTL = Counter/timer lower
CTLR = Counter/timer lower register
CTU = Counter/timer upper
CTUR = Counter/timer upper register
MR = Mode register A
SR = Status register
THR = Tx holding register

### Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and two clock selectors.

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1/CLK is driven using a configuration similar to the one in Figure 5. In this case, the input high-voltage must be capable of attaining the voltage specified in the DC Electrical Characteristics. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied if the internal BRG is not used.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection by the receiver and transmitter of any of these baud rates or an external timing signal.

The C/T operation is programmed by ACR[6:4]. One of eight timing sources can be used as the input to the C/T. The output of the C/T is available to the clock selectors and can be programmed by ACR[2:0] to be output on the MPO pin.

In the timer mode, the C/T generates a square wave whose period is twice the number of clock periods loaded into the C/T upper and lower registers. The counter ready bit in the ISR is set once each cycle of the square wave. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be affected. In this mode the C/T runs continuously and does not recognize the stop counter command (the command only resets the counter ready bit in the ISR). Receipt of a start C/T command causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a start C/T command. Upon reaching terminal count, the counter ready bit in the ISR is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state and the counter ready bit is cleared when the counter is stopped by a stop counter command. the CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command following a stop counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter may be read by the CPU. It is recommended that the

counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter are read. However, a subsequent start counter command causes the counter to begin a new count cycle using the values in CTUR and CTLR.

## Receiver and Transmitter

The UART is a full-duplex asynchronous receiver/transmitter. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input. Registers associated with the communications channel are: the mode registers (MR1 and MR2), the clock select register (CSR), the command register (CR), the status register (SR), the transmit holding register (THR), and the receive holding register (RHR).

### Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the THR. In the 16X clock mode, this also resynchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous low condition) by issuing a start break command via the CR. The break is terminated by a stop break command.

If the transmitter is disabled, it continues operating until the character currently being transmitted and the character in the THR, if any, are completely sent out. Characters cannot be loaded in the THR while the transmitter is disabled.

### Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a high-to-low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled high, the start bit is invalid and the search for a valid start bit begins again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The data is then transferred to the RHR and the RxRDY bit in the SR is set to a 1. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

## RECEIVER FIFO

The RHR consists of a first-in-first-out (FIFO) queue with a capacity of three characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three queue positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in mode register 1. In the character mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set upon receipt of the start bit of the new (overrunning) character.

## WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the UART incorporates a special mode which provides automatic wake-up of the receiver through address frame recognition for multi-processor communications. This mode is selected by programming bits MR1[4:3] to '11'.

In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and 'wake-up' the CPU [by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]. MR1[2] = 0 transmits a zero in the A/D bit position which identifies the corresponding data bits as data, while MR1[2] = 1 transmits a one in the A/D bit position which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits in the THR.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RHR FIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RHR. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

## MULTI-PURPOSE INPUT PIN

The MPI pin can be programmed as an input to one of several UART circuits. The function of the pin is selected by programming the appropriate control register (MR2[4]), ACR[6:4], CSR [7:4, 3:0]). Only one of the functions may be selected at any given time. If CTS or GPI is selected, a change of state detector provided with the pin is activated. A high-to-low or low-to-high transition of the inputs lasting longer than 25–50us sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This produces a sampling period of slightly more than 25us (assuming a 3.6864MHz oscillator input). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25us if the transition occurs coincident with the first sample pulse. The 50us time refers to the condition where the change of state is just missed and the first change of state is not detected until after an additional 25us.

## MULT-PURPOSE OUTPUT PIN

This pin can be programmed to serve as a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TxRDY output or the RxRDY/FFULL output (see ACR[2:0] – MPO Output Select).

## REGISTERS

The operation of the UART is programmed by writing control words in the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is as described in Table 1.

The contents of certain control registers are initialized to zero on reset (see RESET pin description). Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. The contents of the MR, the CSR, and the ACR should only be changed while the receiver and transmitter are disabled, and certain changes to the ACR should only be made while the C/T is stopped. The bit formats of the UART are shown in Table 2.

## MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via the CR. After reading or writing MR1, the pointers are set at MR2.

**MR1[7] – Receiver Request-to-Send Control**

The bit controls the deactivation of the RTSN output (MPO) by the receiver. This output is normally asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is reasserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

**MR1[6] – Receiver Interrupt Select**

This bit selects either the receiver ready status (RxRDY) or the FIFO full status (FFULL) to be used for CPU interrupts.

**MR1[5] – Error Mode Select**

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis. The status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

**MR1[4:3] – Parity Mode Select**

If with parity or force parity is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR![4:3] = 11 selects the channel to operate in the special wake-up mode.

**MR1[2] – Parity Type Select**

This bit selects the parity type (odd or even) if the with parity mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the force parity mode is programmed. It has no effect if the no parity mode is programmed. In the special wake-up mode, it selects the polarity of the transmitted A/D bit.

**MR1[1:0] – Bits Per Character Select**

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

## MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

**MR2[7:6] – Mode Select**

The UART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

7. Received data is reclocked and retransmitted on the TxD output.
8. The receive clock is used for the transmitter.
9. The receiver must be enabled, but the transmitter need not be enabled.
10. The TxRDY and TxEMT status bits are inactive.
11. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
12. Character framing is checked, but the stop bits are retransmitted as received.
13. A received break is echoed as received until the next valid start bit is detected.
14. CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

When switching in and out of the various modes, the selected mode is activated immediately upon mode selection, even if this occurs

in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of auto-echo or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in auto-echo by assertion o fRxRDY), and the transmitter is enabled, the transmitter is enabled, the transmitter will remain in auto-echo mode until one full stop bit has been retransmitted.

**MR2[5] – Transmitter Request-to–Send Control**

This bit controls the deactivation of the RTSN output (MPO) by the transmitter. This output is normally asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the THR (if any) are completely transmitted (including the programmed number of stop bits) if the transmitter is not enabled. This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Disable transmitter after the last character of the message is loaded in the THR.
6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

## Table 2. Register Bit Formats

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| **MR1 (Mode Register 1)** | | | | | | | |
| **RxRT Control** | **RxINT Select** | **Error Mode** | **Parity Mode** | | **Parity Type** | **Bits per Character** | |
| 0 = no<br>1 = yes | 0 = RxRDY<br>1 = FFULL | 0 = Char<br>1 = Block | 00 = With parity<br>01 = Force parity<br>10 = No parity<br>11 = Special mode | | 0 = Even<br>1 = Odd | 00 = 5<br>01 = 6<br>10 = 7<br>11 = 8 | |
| **MR2 (Mode Register 2)** | | | | | | | |
| **Channel Mode** | | **TxRTS Control** | **CTS Enable Tx** | **Stop Bit Length*** | | | |
| 00 = Normal<br>01 = Auto echo<br>10 = Local loop<br>11 = Remote loop | | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = 0.563<br>1 = 0.625<br>2 = 0.688<br>3 = 0.750 | 4 = 0.813<br>5 = 0.875<br>6 = 0.938<br>7 = 1.000 | 8 =1.563<br>9 = 1.625<br>A = 1.688<br>B = 1.750 | C = 1.813<br>D = 1.875<br>E = 1.938<br>F = 2.000 |
| **NOTE:**<br>*Add 0.5 to values shown for 0–7 if channel is programmed for 5 bits/character. | | | | | | | |
| **CSR (Clock Select Register)** | | | | | | | |
| **Receiver Clock Select** | | | | **Transmitter Clock Select** | | | |
| See Text | | | | See Text | | | |
| **CR (Command Register)** | | | | | | | |
| **Miscellaneous Commands** | | | | **Disable Tx** | **Enable Tx** | **Disable Rx** | **Enable Rx** |
| See Text | | | | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |
| **SR (Channel Status Register)** | | | | | | | |
| **Received Break** | **Framing Error** | **Parity Error** | **Overrun Error** | **TxEMT** | **TxRDY** | **FFULL** | **RxRDY** |
| 0 = No<br>1 = Yes<br>* | 0 = No<br>1 = Yes<br>* | 0 = No<br>1 = Yes<br>* | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |
| **NOTE:**<br>*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4;0]. These bits are cleared by a reset error status command. In character mode they are reset when the corresponding data character is read from the FIFO. | | | | | | | |
| **ACR (Auxiliary Control Register)** | | | | | | | |
| **BRG Set Select** | **Counter/Timer Mode and Source** | | | **Power-Down Mode** | **MPO Pin Function Select** | | |
| 0 = Set 1<br>1 = Set 2 | See Text | | | 0 = On<br>1 = Off | 000 = RTSN<br>001 = C/TO<br>010 = TxC (1X)<br>011 = TxC (16X) | 100 = RxC (1X)<br>101 = RxC (16X)<br>110 = TxRDY<br>111 = RxRDY/FFULL | |

**Table 2. Register Bit Formats** (Continued)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| **ISR (Interrupt Status Register)** | | | | | | | |
| **MPI Pin Change** | **MPI Pin Current State** | **Not used** | **Counter Ready** | **Delta Break** | **RxRDY/ FFULL** | **TxEMT** | **TxRDY** |
| 0 = No<br>1 = Yes | 0 = Low<br>1 = High | | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |
| **IMR (Interrupt Mask Resister)** | | | | | | | |
| **MPI Change Interrupt** | **MPI Level Interrupt** | **Not used** | **Counter Ready Int** | **Delta Break Interrupt** | **RxRDY/FFULL Interrupt** | **TxEMT Interrupt** | **TxRDY Interrupt** |
| 0 = Off<br>1 = On | 0 = Off<br>1 = On | | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On |
| **CTUR (Counter/Timer Upper Register)** | | | | | | | |
| **C/T[15]** | **C/T[14]** | **C/T[13]** | **C/T[12]** | **C/T[11]** | **C/T[10]** | **C/T[9]** | **C/T[8]** |
| | | | | | | | |
| **CTLR (Counter/Timer Lower Register)** | | | | | | | |
| **C/T[7]** | **C/T[6]** | **C/T[5]** | **C/T[4]** | **C/T[3]** | **C/T[2]** | **C/T[1]** | **C/T[0]** |
| | | | | | | | |

**MR2[4] – Clear-to-Send Control**
The sate of this bit determines if the CTSN input (MPI) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (low), the character is transmitted. If it is negated (high), the TxD output remains in the marking state and the transmission is delayed until CTSN goes low. Changes in CTSN while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

**MR2[3:0] – Stop Bit Length Select**
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmittted.

## CSR – Clock Select Register

**CSR[7:4] – Receiver Clock Select**
This field selects the baud rate clock for the receiver as shown in Table 3. The baud rates listed are for a 3.6864MHz crystal or external clock.

**CSR[3:0] – Transmitter Clock Select**
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3.

**Table 3. Baud Rate Selection**

| CSR[3:0]/ [7:4] | ACR[7] = 0 | ACR[7] = 1 |
|---|---|---|
| 0 0 0 0 | 50 | 50 |
| 0 0 0 1 | 110 | 110 |
| 0 0 1 0 | 134.5 | 134.5 |
| 0 0 1 1 | 200 | 150 |
| 0 1 0 0 | 300 | 300 |
| 0 1 0 1 | 600 | 600 |
| 0 1 1 0 | 1,200 | 1,200 |
| 0 1 1 1 | 1,050 | 1,050 |
| 1 0 0 0 | 2,400 | 2,400 |
| 1 0 0 1 | 4,800 | 4,800 |
| 1 0 1 0 | 7,200 | 1,800 |
| 1 0 1 1 | 9,600 | 9,600 |
| 1 1 0 0 | 38.4k | 19.2k |
| 1 1 0 1 | Timer | Timer |
| 1 1 1 0 | MPI – 16X | MPI – 16X |
| 1 1 1 1 | MPI–1X | MPI–1X |

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111.

## CR – Command Register

CR is used to write commands to the UART. Multiple commands can be specified in a single write to CR as long as the commands are non-conflicting, e.g., the enable transmitter and reset transmitter commands cannot be specified in a single command word.

**CR[7:4] – Miscellaneous Commands**
The encoded value of this field may be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the MR pointer to point to MR1.

0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disable and the FIFO is flushed.

0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied

0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[3]) to be cleared to zero.

0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the THR, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break.

0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

1000 Start C/T. In counter or timer modes, causes the contents of CTUR/CTLR to be preset into the counter/timer and starts the counting cycle. In timer mode, any counting cycle in progress when the command is issued is terminated. In counter mode, has no effect unless a stop C/T command was issued previously.

1001 Stop counter. In counter mode, stops operation of the counter/timer, resets the counter ready bit in the ISR, and forces the MPO output high if it is programmed to be the output of the C/T. In timer mode, resets the counter ready bit in the ISR but has no effect on the counter/timer itself or on the MPO output.

1010 Assert RTSN. Causes the RTSN output (MPO) to be asserted (low).

1011 Negate RTSN.Causes the RTSN output (MPO) to be negated (high).

1100 Reset MPI change interrupt. Causes the MPI change bit in the interrupt status register (ISR[7]) to be cleared to zero.

1101 Reserved.

111x Reserved.

**CR[3] – Disable Transmitter**
This command terminates operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

**CR[2] – Enable Transmitter**
Enables operation of the channel A transmitter. The TxRDY status bit will be asserted.

**CR[1] – Disable Receiver**
This command terminates operation of the receiver immediately; a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake-up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

**CR[0] – Enable Receiver**
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

## SR – Channel Status Register

The status register is updated while RDN is negated. Therefore, the bus interface used with this device must not use a static RDN line. The RDN line must be pulsed to allow status register updates.

**SR[7] – Received Break**
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxD line returns to the marking state for at least one half bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the change in break bit in the ISR (ISR[3]) is set. ISR[3] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character time in order for it to be detected.

**SR[6] – Framing Error (FE)**
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

**SR[5]– Parity Error (PE)**
This bit is set when the with parity or force parity mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special wake-up mode, the parity error bit stores the received A/D bit.

**SR[4] – Overrun Error (OE)**
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

**SR[3] – Transmitter Empty (TxEMT)**
This bit will be set when the transmitter underruns, i.e., both the transmit holding register (THR) and the transmit shift register are empty. However, this bit is not set until at least one character has been transmitted. It is set after transmission of the last stop bit of a character, If no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU, or when the transmitter is disabled.

**SR[2] – Transmitter Ready (TxRDY)**
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the THR while the transmitter is disabled will not be transmitted.

**SR[1] – FIFO Full (FFULL)**
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL will be reset by the CPU read and then set by the transfer of the character to the FIFO, which causes all three FIFO positions to be occupied.

**SR[0] – Receiver Ready (RxRDY)**
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, and no more characters are in the FIFO.

## ACR – Auxiliary Control Register

**ACR[7] – Baud Rate Generator Set Select**
This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the receiver and transmitter. See Table 4 for characteristics of the BRG.

**ACR[6:4] – Counter/Timer Mode and Clock Source Select**
This field selects the operating mode of the counter/timer and its clock source as follows:

| ACR [6:4] | Mode | Clock Source |
|---|---|---|
| 0 0 0 | Counter | MPI pin |
| 0 0 1 | Counter | MPI pin divided by 16 |
| 0 1 0 | Counter | TxC–1X clock of the transmitter |
| 0 1 1 | Counter | Crystal or external clock (X1/CLK) divided by 16 |
| 1 0 0 | Timer | MPI pin |
| 1 0 1 | Timer | MPI pin divided by 16 |
| 1 1 0 | Timer | Crystal or external clock (X1/CLK) |
| 1 1 1 | Timer | Crystal or external clock (X1/CLK) divided by 16 |

**ACR[3] – Power-Down Mode Select**
This bit, when set to zero, selects the power-down mode. In this mode, the 2691 oscillator is stopped and all functions requiring this clock are suspended. The contents of all registers are saved. It is recommended that the transmitter and receiver be disabled prior to placing the 2691 in this mode. Note that this bit must be set to a logic 1 after reset.

When the power-down mode is enabled, internal circuitry forces the X1/CLK pin to the low state and the X2 pin to the high state. If an external clock is being used to drive the device, it is recommended that the clock source be three-stated or forced low while the UART is in power-down mode in order to prevent the clock driver from being short circuited.

## Table 4. BRG Characteristics

Crystal or Clock = 3.6864MHz

| Nom Rate (Baud) | Actual 16X* Clock (kHz) | Error (%) |
|---|---|---|
| 50 | 0.8 | 0 |
| 75 | 1.2 | 0 |
| 110 | 1.759 | –0.069 |
| 134.5 | 2.153 | 0.059 |
| 150 | 2.4 | 0 |
| 200 | 3.2 | 0 |
| 300 | 4.8 | 0 |
| 600 | 9.6 | 0 |
| 1050 | 16.756 | –0.260 |
| 1200 | 19.2 | 0 |
| 1800 | 28.8 | 0 |
| 2000 | 32.056 | 0.175 |
| 2400 | 38.4 | 0 |
| 4800 | 76.8 | 0 |
| 7200 | 115.2 | 0 |
| 9600 | 153.6 | 0 |
| 19.2k | 307.2 | 0 |
| 38.4k | 614.4 | 0 |

*Duty cycle of 16X clock is 50% ±1%

**ACR[2:0] – MPO Output Select**
This field programs the MPO output pin to provide one of the following:

000 Request-to-send active-low output (RTSN). This output is asserted and negated via the command register. RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted out or when the receiver FIFO and receiver shift register are full using MR2[5] and MR1[7], respectively.

001 The counter/timer output. In the timer mode, this output is a square wave with a period of twice the value (in clock periods) of the contents of the CTUR and CTLR. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. the output returns to the high state when the counter is stopped by a stop counter command.

010 The 1X clock for the transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a non-synchronized 1X clock is output.

011 The 16X clock for the transmitter. This is the clock selected by CSR[3:0] = 1111.

100 The 1X clock for the receiver, which is the clock that samples the received data. If data is not being received, a non-synchronized 1X clock is output.

101 The 16X clock for the receiver. This is the clock selected by CSR[7:4], and is a 1X clock if CSR[7:4] = 1111.

110 The transmitter register empty signal, which is the complement of SR[2]. Active low output.

111 The receiver ready or FIFO full signal (complement of ISR[2]). Active-low output.

## ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR. This register is cleared when the device is reset.

**ISR[7] – MPI Change-of-State**
This bit is set when a change-of-state occurs at the MPI input pin. It is reset by a reset change interrupt command.

**ISR[6] – MPI Current State**
This bit provides the current state of the MPI pin. This information is latched and reflects the state of the pin at the leading edge of the ISR ready cycle.

**ISR[4] – Counter Ready**
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

**ISR[3] – Change in Break**
This bit, when set, indicates that the receiver has detected the beginning or end of a received break. It is reset when the CPU issues a reset break change interrupt command.

**ISR[2] – Receiver Ready or FIFO Full**
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the FIFO is read and there is no character in the receive shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

**ISR[1] – Transmitter Empty**
This bit is a duplicate of TxEMT (SR[3]).

**ISR[0] – Transmitter Ready**
This bit is a duplicate of TxRDY (SR[2]).

## IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR.

## CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded is $0002_{16}$.

In the timer (programmable divider) mode, the C/T generates a square wave whose period is twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be.

The counter ready status bit (ISR[4]) is set once each cycle of the square wave. The bit is reset by a stop counter command. The command, however, does not stop the C/T. The generated square wave is output on MPO if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR. Counting begins upon receipt of a start C/T

command. Upon reaching the terminal count, the counter ready interrupt bit (ISR[4]) is set. the counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time it goes low.

The output returns to the high state and ISR[4] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_{CC}$ | Voltage from $V_{CC}$ to GND[3] | –0.5 to + 7.0 | V |
| $V_S$ | Voltage from any pin to ground[3] | –0.5 to $V_{CC}$ +10% | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High–level input voltage (except X1/CLK) | 2.0 | | | V |
| $V_{IH}$ | High-level input voltage (X1/CLK) | 4.0 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OL}$ | Low–level output current | | | 2.4 | mA |
| $I_{OH}$ | High-level output current | | | –400 | µA |
| $T_A$ | Operating free air temperature range[2] | –55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS[4, 5], $-55°C \leq T_A \leq 125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[5] | Max | |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = MAX | | | 0.4 | V |
| $V_{OH}$[7] | Output high voltage (except open drain outputs) | $I_{OH}$ = MAX | 2.4 | | | V |
| | Input leakage current | $V_{IN}$ = 0 to $V_{CC}$ | –10 | | 10 | µA |
| $I_{OZH}$ | Output off current, High, 3–State Data Bus | $V_{IN} = V_{CC}$ | –10 | | 10 | µA |
| $I_{OZL}$ | Output off current, Low, 3–State Data Bus | $V_{IN}$ = 0 | –10 | | 10 | µA |
| $I_{XIL}$ | X1/CLK low input current | $V_{IN}$ = 0, X2 floated | –100 | –30 | 0 | µA |
| $I_{XIH}$ | X1/CLK high input current | $V_{IN} = V_{CC}$, X2 floated | 0 | 30 | 100 | µA |
| $I_{X2L}$ | X2 low output current | $V_{OUT}$ = 0, X1/CLK = $V_{CC}$ | –100 | | | µA |
| $I_{X2H}$ | X2 high output current | $V_{OUT} = V_{CC}$, X1/CLK = 0V | | | 100 | µA |
| $I_{CCA}$ | Power supply current, active | | | 1.0 | 3.0 | mA |
| $I_{CCD}$ | Power down current | | | | 500 | µA |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperature, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0V and 2.8V with a transition time of 20ns max. For X1/CLK, this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2V and output voltages of 0.8V and 2V as appropriate.
5. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
6. Test condition for outputs: $C_L$ = 150pF, except interrupt outputs. Test conditions for interrupt outputs: $C_L$ = 50pF, $R_L$ = 2.7kohms to $V_{CC}$.
7. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN. CEN and RDN (also CEN and WRN) are ORed internally. As a consequence, this signal asserted last initiates the cycle and the signal negated first terminates the cycle.
8. If CEN is used as the 'strobing' input, this parameter defines the minimum high time between one CEN and the next. The RDN signal must be negated for $t_{RWD}$ guarantee that any status register changes are valid.
9. Consecutive write operations to the command register require at least three rising edges of the X1 clock between writes.
10. These parameters are guaranteed by design but are not 100% tested.

## AC ELECTRICAL CHARACTERISTICS[4, 5, 6] $-55°C \leq T_A \leq 125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| **Reset timing (Figure 1)** | | | | | |
| $t_{RES}$ | Reset pulse width | 100 | | | ns |
| **Bus timing (Figure 2)[7]** | | | | | |
| $t_{AS}$ | A0–A2 setup time to RDN, WRN low | 10 | | | ns |
| $t_{AH}$ | A0–A2 hold time from RDN, WRN high | 0 | | | ns |
| $t_{CS}$ | CEN setup time to RDN, WRN low | 0 | | | ns |
| $t_{CH}$ | CEN hold time from RDN, WRN high | 0 | | | ns |
| $t_{RW}$ | WRN, RDN pulse width | 150 | | | ns |
| $t_{DD}$ | Data valid after RDN low | | | 125 | ns |
| $t_{DF}$ | Data bus floating after RDN high | | | 110 | ns |
| $t_{DS}$ | Data setup time before WRN high | 50 | | | ns |
| $t_{DH}$ | Data hold time after WRN high | 30 | | | ns |
| $t_{RWD}$ | Time between reads and/or writes[9, 10] | 150 | | | ns |
| **MPI and MPO timing (Figure 3)[7]** | | | | | |
| $t_{PS}$ | MPI input setup time before RDN low | 30 | | | ns |
| $t_{PH}$ | MI input hold time after RDN low | 30 | | | ns |
| $t_{PD}$ | MPO output valid after WRN high | | | 370 | ns |
| **Interrupt timing (Figure 4)** | | | | | |
| $t_{IR}$ | INTRN negated | | | | |
| | Read RHR (RxRDY/FFULL interrupt) | | | 370 | ns |
| | Write THR (TxRDY, TxEMT interrupt) | | | 370 | ns |
| | Reset command (break change interrupt) | | | 370 | ns |
| | Reset command (MPI change interrupt) | | | 370 | ns |
| | Stop C/T command (counter interrupt) | | | 370 | ns |
| | Write IMR (clear of interrupt mask bit) | | | 270 | ms |
| **Clock timing (Figure 5)** | | | | | |
| $t_{CLK}$ | X1/CLK high or low time | 100 | | | ns |
| $f_{CLK}$ | X1/CLK frequency | 2.0 | 3.6864 | 4.0 | MHz |
| $t_{CTC}$ | Counter/timer clock high or low time | 100 | | | ns |
| $f_{CTC}$ | Counter/timer clock frequency | 0[10] | | 4.0 | MHz |
| $t_{RX}$ | RxC high or low time | 220 | | | ns |
| $f_{RX}$ | RxC frequency (16X) | 0[10] | | 2.0 | MHz |
| | RxC frequency (1X) | 0[10] | | 1.0 | MHz |
| $t_{TX}$ | TxC high or low time | 220 | | | ns |
| $f_{TX}$ | TxC frequency (16X) | 0[10] | | 2.0 | MHz |
| | TxC frequency (1X) | 0[10] | | 1.0 | MHz |
| **Transmitter timing (Figure 6)** | | | | | |
| $t_{TXD}$ | TxD output delay from TxC low | | | 350 | ns |
| $t_{TCS}$ | TxC output delay from TxD output data | 0 | | 150 | ns |
| **Receiver timing (Figure 7)** | | | | | |
| $t_{RXS}$ | RxD data setup time to RxC high | 100 | | | ns |
| $t_{RXH}$ | RxD data hold time from RxC high | 100 | | | ns |

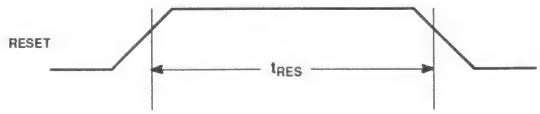



Figure 1. Reset Timing

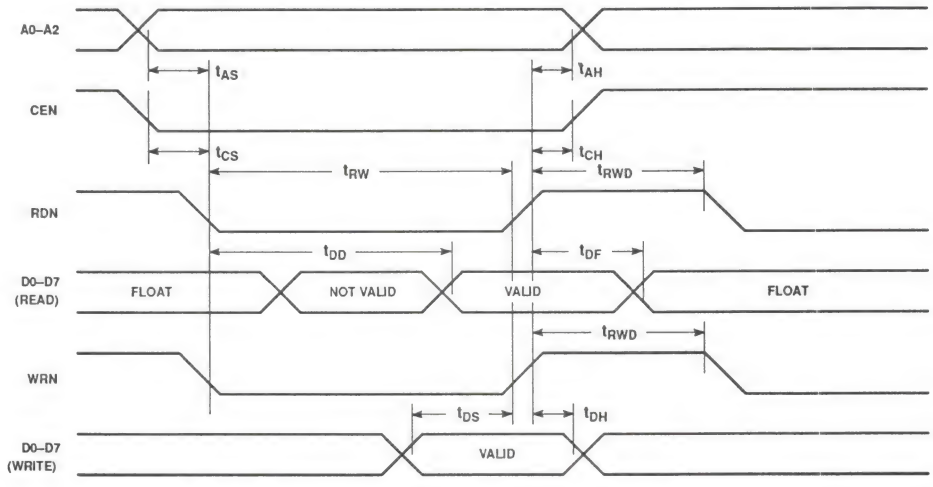



Figure 2. Bus Timing

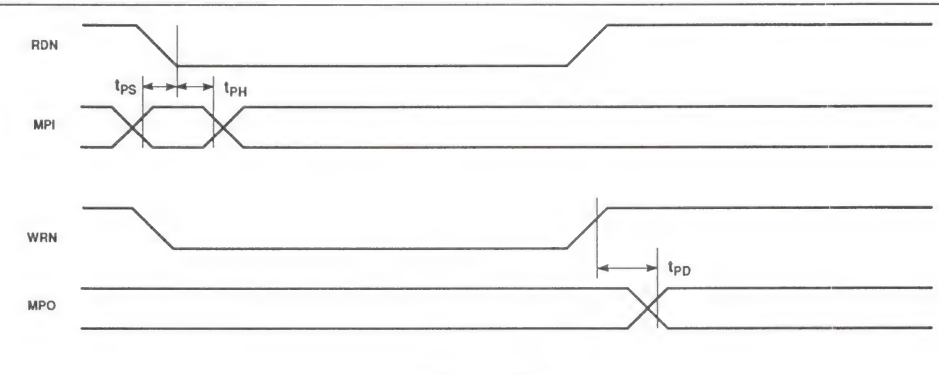
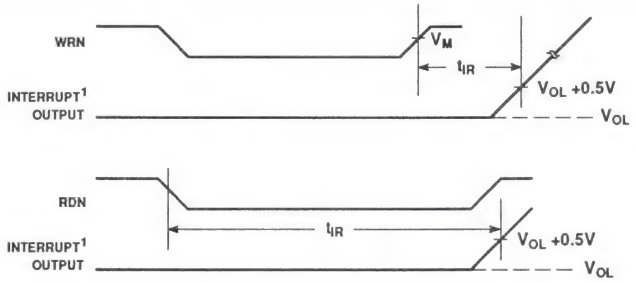



Figure 3. I/O Timing




NOTES:
1. INTRN OR MPO WHEN USED AS INTERRUPT OUTPUTS.
2. THE TEST FOR OPEN DRAIN OUTPUTS IS INTENDED TO GUARANTEE SWITCHING OF THE OUTPUT TRANSISTOR. MEASUREMENT OF THIS RESPONSE IS REFERENCED FROM THE MIDPOINT OF THE SWITCHING SIGNAL, $V_M$, TO A POINT 0.5V ABOVE $V_{OL}$. THIS POINT REPRESENTS NOISE MARGIN THAT ASSURES TRUE SWITCHING HAS OCCURRED. BEYOND THIS LEVEL, THE EFFECTS OF EXTERNAL CIRCUITRY AND TEST ENVIRONMENT ARE PRONOUNCED AND CAN GREATLY AFFECT THE RESULTANT MEASUREMENT.

Figure 4. Interrupt Timing

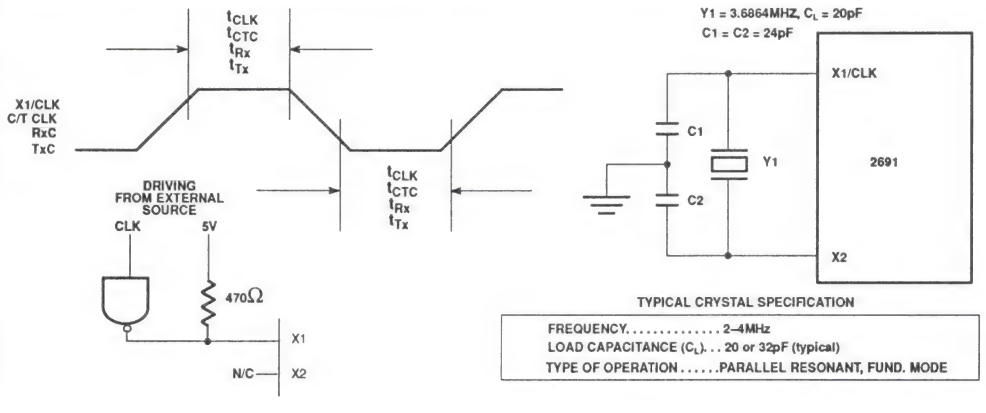



Figure 5. Clock Timing

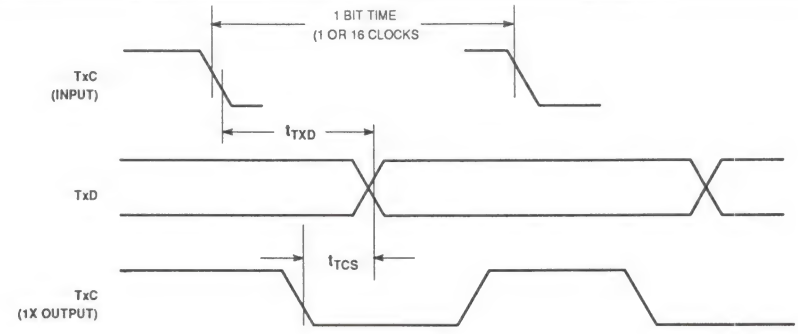



Figure 6. Transmit Timing

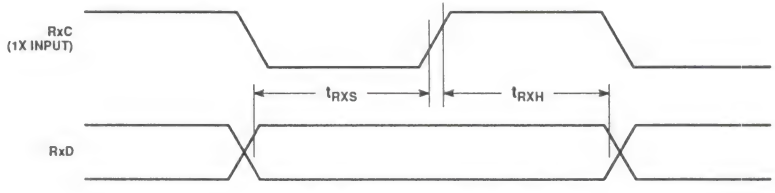



Figure 7. Receive Timing

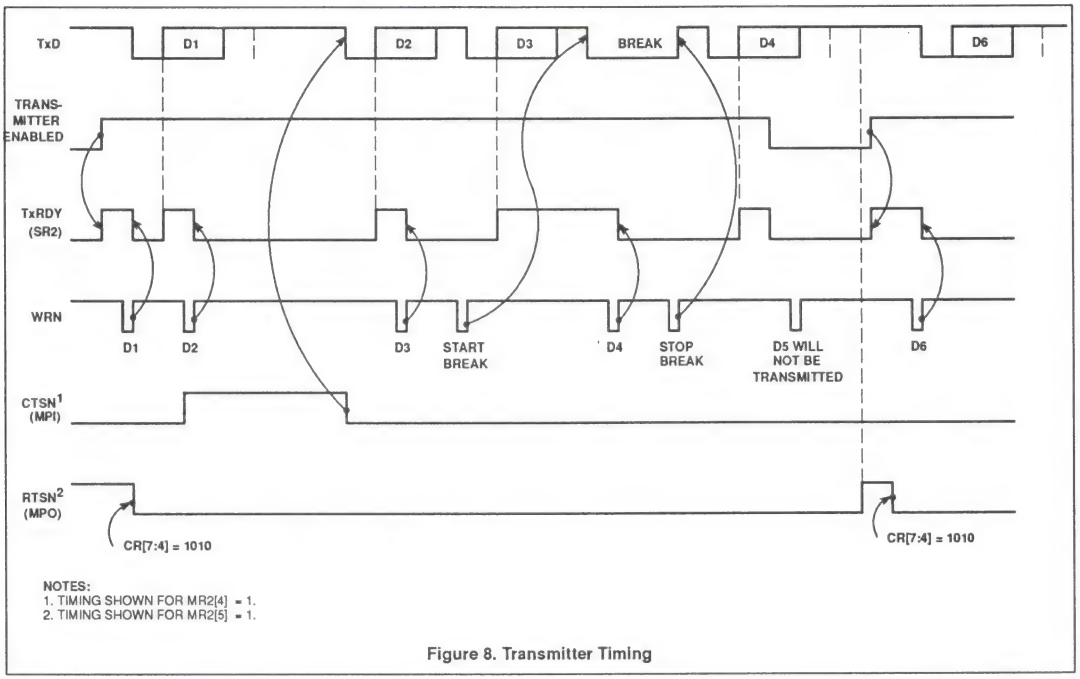



Figure 8. Transmitter Timing

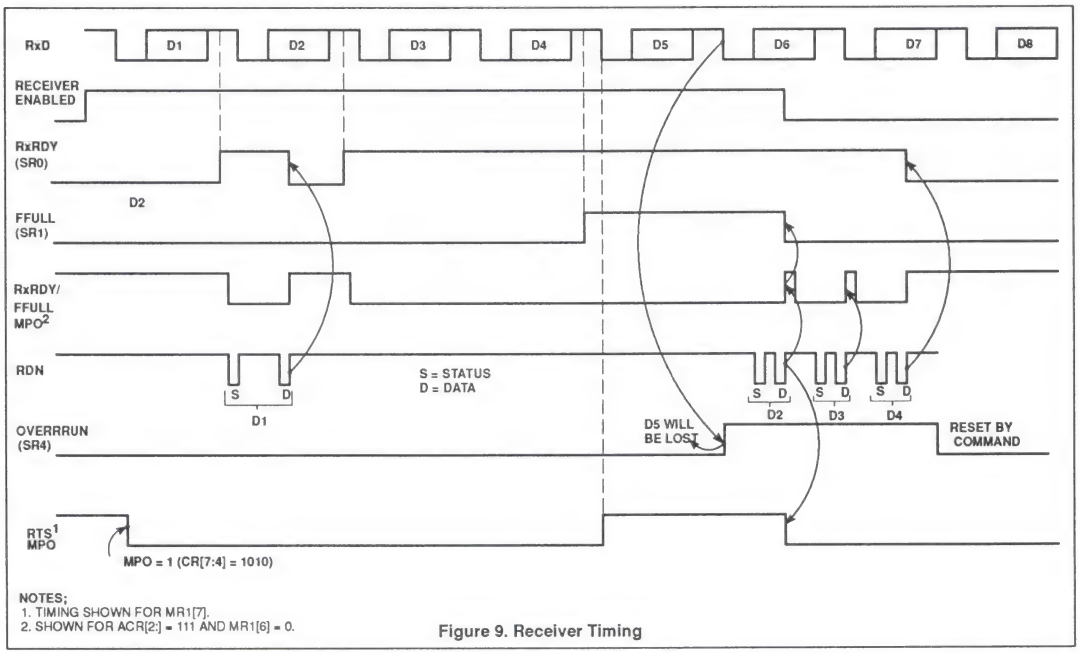



Figure 9. Receiver Timing

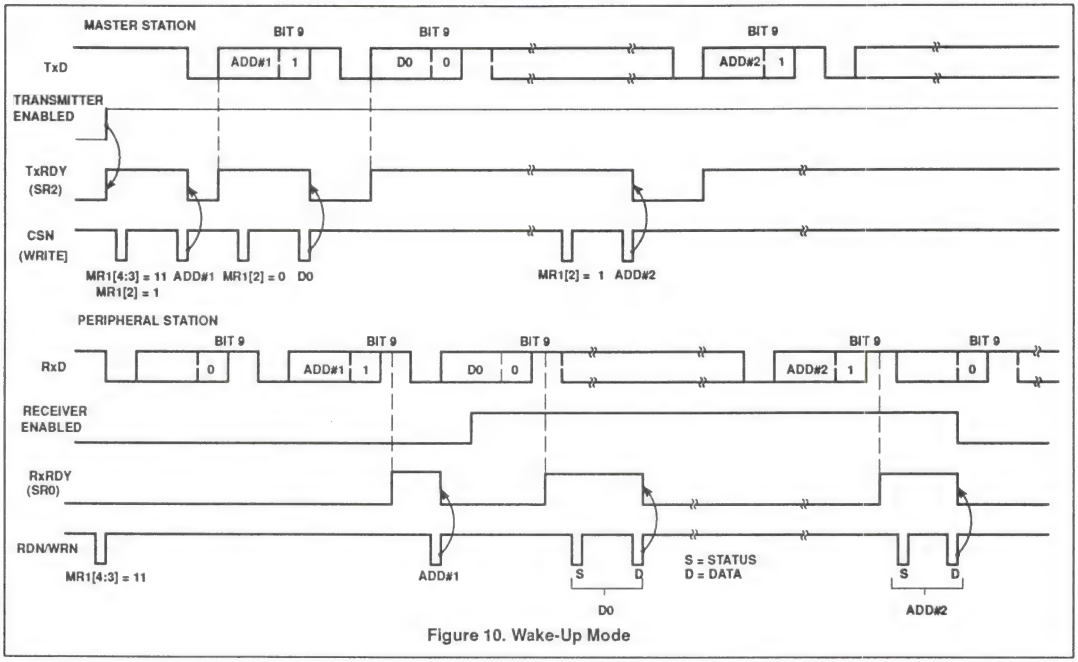



Figure 10. Wake-Up Mode

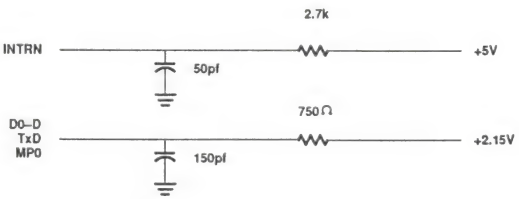



Figure 11. Test Conditions on Outputs

Signetics

# 2692
## Dual Asynchronous Receiver/Transmitter (DUART)

*Product Specification*

**Military Microprocessor Products**

### DESCRIPTION

The Signetics 2692 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

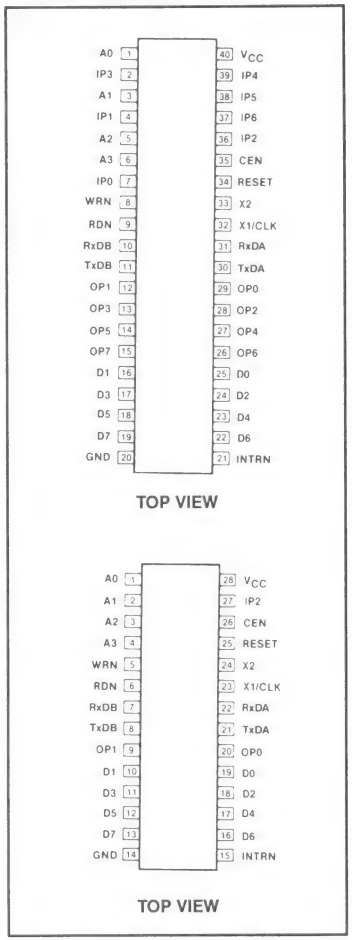
Also provided on the 2692 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The 2692 is available in four package versions: 40-pin and 28-pin, 0.6" wide Ceramic DIPs, a 44-pin LLCC, and a 52-pin Ceramic Flat Package.

### FEATURES

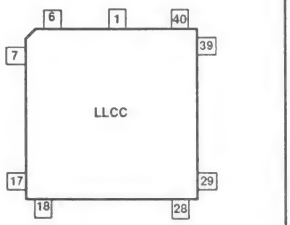
- **Dual full-duplex asynchronous receiver/transmitters**
- **Quadruple buffered receiver data register**
- **Programmable data format**
  - **5 to 8 data bits plus parity**
  - **Odd, even, no parity or force parity**
  - **1, 1.5 or 2 stop bits programmable in 1/16-bit increments**
- **Programmable baud rate for each receiver and transmitter selectable from:**
  - **18 fixed rates: 50 to 38.4k baud**
  - **One user-defined rate derived from programmable counter/timer**
  - **External 1X or 16X clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **Normal (full-duplex)**
  - **Automatic echo**
  - **Local loopback**
  - **Remote loopback**
- **Multifunction 7-bit input port**
  - **Can serve as clock or control inputs**
  - **Change of state detection on four inputs**
- **Multifunction 8-bit output port**
  - **Individual bit set/reset capability**
  - **Outputs can be programmed to be status/interrupt signals**
- **Versatile interrupt system**
  - **Single interrupt output with eight maskable interrupting conditions**
  - **Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs**
- **Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec**
- **Automatic wake-up mode for multidrop applications**
- **Start-end break interrupt/status**

### PIN CONFIGURATIONS

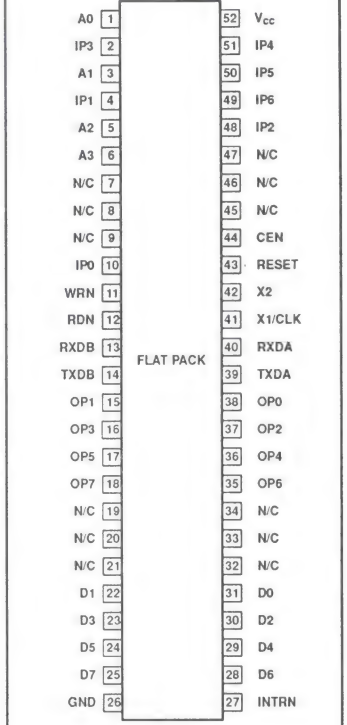



- **Detects break which originates in the middle of a character**
- **On-chip crystal oscillator**
- **Power down mode**
- **Receiver timeout mode**
- **TTL compatible**
- **Single +5V power supply**

## PIN CONFIGURATIONS (Continued)



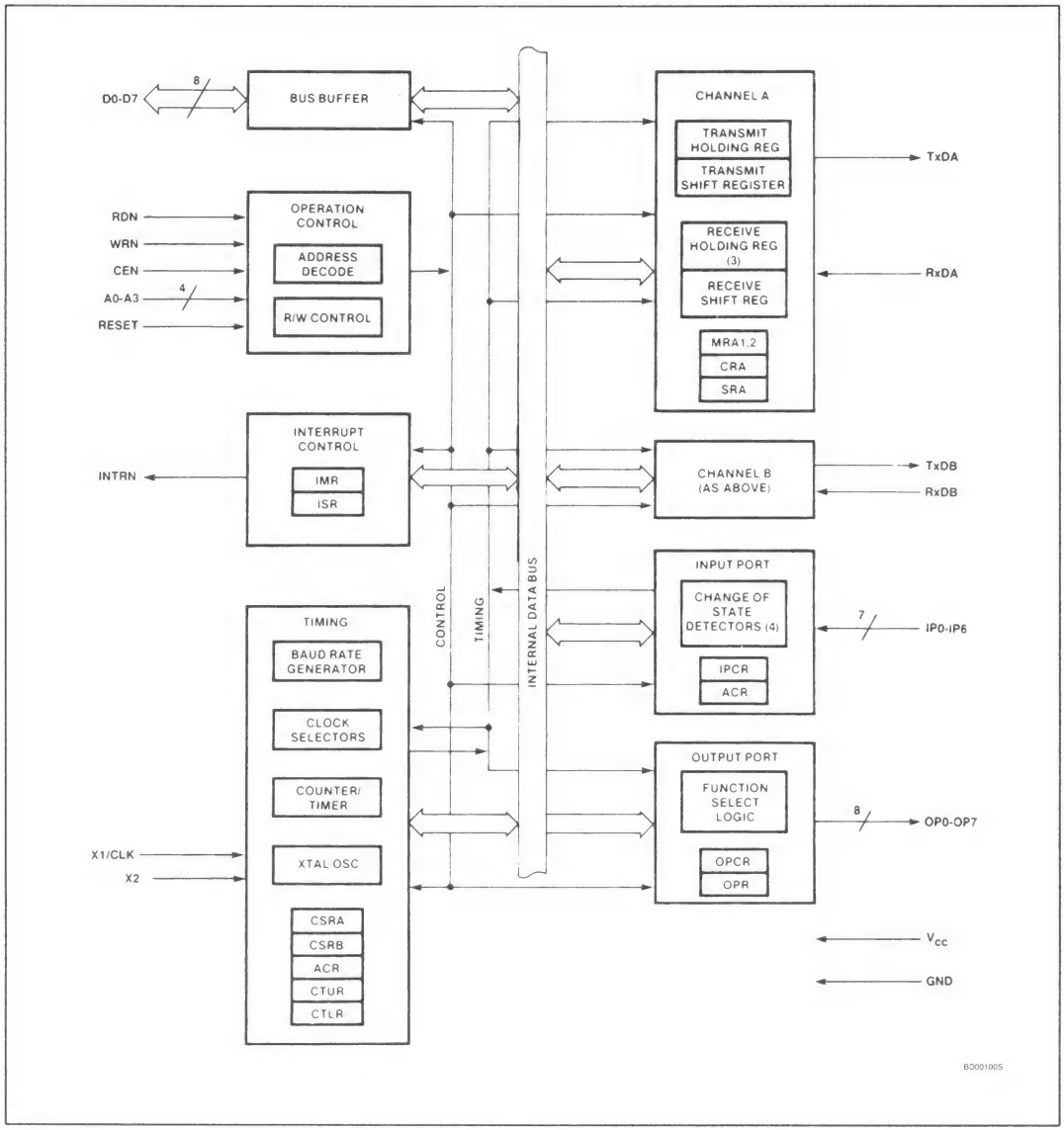

| PIN | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | A0 | 24 | INTRN |
| 3 | IP3 | 25 | D6 |
| 4 | A1 | 26 | D4 |
| 5 | IP1 | 27 | D2 |
| 6 | A2 | 28 | D0 |
| 7 | A3 | 29 | OP6 |
| 8 | IP0 | 30 | OP4 |
| 9 | WRN | 31 | OP2 |
| 10 | RDN | 32 | OP0 |
| 11 | RxDB | 33 | TxDA |
| 12 | NC | 34 | NC |
| 13 | TxDB | 35 | RxDA |
| 14 | OP1 | 36 | X1/CLK |
| 15 | OP3 | 37 | X2 |
| 16 | OP5 | 38 | RESET |
| 17 | OP7 | 39 | CEN |
| 18 | D1 | 40 | IP2 |
| 19 | D3 | 41 | IP6 |
| 20 | D5 | 42 | IP5 |
| 21 | D7 | 43 | IP4 |
| 22 | GND | 44 | $V_{CC}$ |




## ORDERING INFORMATION

| PACKAGE | ORDER CODE |
|---|---|
| 28-Pin Ceramic DIP | 2692/BXA |
| 40-Pin Ceramic DIP | 2692/BQA |
| 44-Pin LLCC | 2692/BUA |
| 52-Pin Flat Pack | 2692/BYA |

## BLOCK DIAGRAM



# Dual Asynchronous Receiver/Transmitter (DUART) 2692

## PIN DESCRIPTION

| SYMBOL | APPLICABLE | | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|
| | 40,44,52 | 28 | | |
| D0-D7 | X | X | I/O | **Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit. |
| CEN | X | X | I | **Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition. |
| WRN | X | X | I | **Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal. |
| RDN | X | X | I | **Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN. |
| A0-A3 | X | X | I | **Address Inputs:** Select the DUART internal registers and ports for read/write operations. |
| RESET | X | X | I | **Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. |
| INTRN | X | X | O | **Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true. |
| X1/CLK | X | X | I | **Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). |
| X2 | X | X | I | **Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin can be left open or connected to ground. |
| RxDA | X | X | I | **Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low. |
| RxDB | X | X | I | **Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low. |
| TxDA | X | X | O | **Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low. |
| TxDB | X | X | O | **Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low. |
| OP0 | X | X | O | **Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit. |
| OP1 | X | X | O | **Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit. |
| OP2 | X | | O | **Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output. |
| OP3 | X | | O | **Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output. |
| OP4 | X | | O | **Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output. |
| OP5 | X | | O | **Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output. |
| OP6 | X | | O | **Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output. |
| OP7 | X | | O | **Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYBN output. |
| IP0 | X | | I | **Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN). |
| IP1 | X | | I | **Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN). |
| IP2 | X | X | I | **Input 2:** General purpose input or counter/timer external clock input. |
| IP3 | X | | I | **Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. |

## PIN DESCRIPTION (Continued)

| SYMBOL | APPLICABLE | | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|
| | 40,44,52 | 28 | | |
| IP4 | X | | I | **Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. |
| IP5 | X | | I | **Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. |
| IP6 | X | | I | **Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. |
| $V_{CC}$ | X | X | I | **Power Supply:** +5V supply input. |
| GND | X | X | I | **Ground** |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |
| $V_{CC}$ | Voltage from $V_{CC}$ to GND[3] | -0.5 to +7.0 | V |
| $V_S$ | Voltage from any pin to GND[3] | -0.5 to $V_{CC}$ +0.5 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High level input voltage (except X1/CLK) | 2.0 | | | V |
| $V_{IH}$ | High level input voltage (X1/CLK) | 4.0 | | | V |
| $V_{IL}$ | Low level input voltage | | | 0.8 | V |
| $I_{OL}$ | Low level output current | | | 2.4 | mA |
| $I_{OH}$ | High level output current | | | -400 | µA |
| $T_A$ | Operating free air temperature range[2] | -55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS[4, 5, 7] $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[6] | Max | |
| $V_{IL}$ | Input Low voltage | | | | 0.8 | V |
| $V_{IH}$ | Input High voltage (except X1/CLK) | | 2.0 | | | V |
| $V_{IH}$ | Input High voltage (X1/CLK) | | 0.8 $V_{CC}$ | | | V |
| $V_{OL}$ | Output Low voltage | $I_{OL}$ = 2.4mA | | | 0.4 | V |
| $V_{OH}$ | Output High voltage (except OD outputs) | $I_{OH}$ = -400µA | $V_{CC}$ -0.5 | | | V |
| $I_{IX1PD}$ | X1/CLK input current - power down | $V_{IN} = 0$ to $V_{CC}$ | -10 | | +10 | µA |
| $I_{ILX1}$ | X1/CLK input Low current - operating | $V_{IN} = 0$ | -75 | | 0 | µA |
| $I_{IHX1}$ | X1/CLK input High current - operating | $V_{IN} = V_{CC}$ | 0 | | 75 | µA |
| $I_{OHX2}$ | X2 output High current - operating | $V_{OUT} = V_{CC}$, X1 = 0 | 0 | | +75 | µA |
| $I_{OHX2S}$ | X2 output High short circuit current - operating | $V_{OUT} = 0$, X1 = 0 | -10 | | -1 | mA |
| $I_{OLX2}$ | X2 output Low current - operating | $V_{OUT} = 0$, X1 = $V_{CC}$ | -75 | | 0 | µA |
| $I_{OLX2S}$ | X2 output Low short circuit current - operating and power down | $V_{OUT} = V_{CC}$, X1 = $V_{CC}$ | 1 | | 10 | mA |
| $I_I$ | Input leakage current: | | | | | |
| | All except input port pins | $V_{IN} = 0$ to $V_{CC}$ | -10 | | +10 | µA |
| | Input port pins | $V_{IN} = 0$ to $V_{CC}$ | -25 | | +10 | µA |
| $I_{OZH}$ | Output Off current High, 3-State data bus | $V_{IN} = V_{CC}$ | | | 10 | µA |
| $I_{OZL}$ | Output Off current Low, 3-State data bus | $V_{IN}$ = 0V | -10 | | | µA |
| $I_{ODL}$ | Open-drain output Low current in Off-State | $V_{IN} = 0$ | -10 | | | µA |
| $I_{ODH}$ | Open-drain output High current in Off-State | $V_{IN} = V_{CC}$ | | | 10 | µA |
| | Power supply current[8] | | | | | |
| | Operating mode | TTL input levels | | | 10 | mA |
| $I_{CC}$ | | CMOS input levels | | | 10 | mA |
| | Power down mode | TTL input levels | | | 3.0 | mA |
| | | CMOS input levels | | | 2.0 | mA |

## AC CHARACTERISTIC[4,5,7]

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ[6] | Max | |
| **Reset Timing (See Figure 1)** | | | | | |
| $t_{RES}$ | RESET pulse width | 1.0 | | | µs |
| **Bus Timing[9] (See Figure 2)** | | | | | |
| $t_{AS}$ | A0-A3 setup time to RDN, WRN Low | 10 | | | ns |
| $t_{AH}$ | A0-A3 hold time from RDN, WRN Low | 100 | | | ns |
| $t_{CS}$ | CEN setup time to RDN, WRN Low | 0 | | | ns |
| $t_{CH}$ | CEN hold time from RDN, WRN High | 0 | | | ns |
| $t_{RW}$ | WRN, RDN pulse width | 225 | | | ns |
| $t_{DD}$ | Data valid after RDN Low | | | 175 | ns |
| $t_{DA}$ | RDN Low to data bus active[12] | 15 | | 110 | ns |
| $t_{DF}$ | Data bus floating after RDN High | | | 125 | ns |
| $t_{DI}$ | RDN High to data bus invalid[12] | 20 | | | ns |
| $t_{DS}$ | Data setup time before WRN High | 100 | | | ns |
| $t_{DH}$ | Data hold time after WRN High | 5 | | | ns |
| $t_{RWD}$ | High time between reads and/or writes[9, 10] | 200 | | | ns |
| **Port Timing[9] (See Figure 3)** | | | | | |
| $t_{PS}$ | Port input setup time before RDN Low | 0 | | | ns |
| $t_{PH}$ | Port input hold time after RDN High | 0 | | | ns |
| $t_{PD}$ | $OP_n$ output valid from WRN High | | | 400 | ns |
| **Interrupt Timing (See Figure 4)** | | | | | |
| | INTRN (or OP3-OP7 when used as interrupts) negated from: | | | | |
| | Read RHR (RxRDY/FFULL interrupt) | | | 300 | ns |
| | Write THR (TxRDY interrupt) | | | 300 | ns |
| $t_{IR}$ | Reset command (break change interrupt) | | | 300 | ns |
| | Stop C/T command (counter interrupt) | | | 300 | ns |
| | Read IPCR (input port change interrupt) | | | 300 | ns |
| | Write IMR (clear of interrupt mask bit) | | | 300 | ns |
| **Clock Timing (See Figure 5)** | | | | | |
| $t_{CLK}$ | X1/CLK High or Low time | 100 | | | ns |
| $f_{CLK}$ | X1/CLK frequency | 2 | 3.6864 | 4 | MHz |
| $t_{CTC}$ | CTCLK (IP2) High or Low time | 100 | | | ns |
| $f_{CTC}$ | CTCLK (IP2) frequency[13] | 0 | | 4 | MHz |
| $t_{RX}$ | RxC High or Low time | 220 | | | ns |
| $f_{RX}$ | RxC frequency (16X)[13] | 0 | | 2 | MHz |
| | (1X)[13] | 0 | | 1 | MHz |
| $t_{TX}$ | TxC High or Low time | 220 | | | ns |
| $f_{TX}$ | TxC frequency (16X)[13] | 0 | | 2 | MHz |
| | (1X)[13] | 0 | | 1 | MHz |
| **Transmitter Timing (See Figure 6)** | | | | | |
| $t_{TXD}$ | TxD output delay from TxC Low | | | 350 | ns |
| $t_{TCS}$ | Output delay from TxC Low to TxD data output | 0 | | 150 | ns |
| **Receiver Timing (See Figure 7)** | | | | | |
| $t_{RXS}$ | RxD data setup time to RxC High | 240 | | | ns |
| $t_{RXH}$ | RxD data hold time from RxC High | 200 | | | ns |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. Test conditions for outputs: $C_L$ = 150pF, except interrupt outputs. Test conditions for interrupt outputs: $C_L$ = 50pF, $R_L$ = 2.7KΩ to $V_{CC}$.
8. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of $V_{CC}$ -0.2V and $V_{SS}$ + 0.2V.
9. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ORed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
10. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for $t_{RWD}$ to guarantee that any status register changes are valid.
11. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
12. Guaranteed by characterization of sample units.
13. Minimum frequencies are not tested but are guaranteed by design.

# Dual Asynchronous Receiver/Transmitter (DUART) 2692

## BLOCK DIAGRAM

The 2692 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

### Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

### Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

### Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

### Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

### Communications Channels A and B

Each communications channel of the 2692 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

### Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4KHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

### Output Port

The 8-bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

## OPERATION

### Transmitter

The 2692 is conditioned to transmit data when the transmitter is enabled through the command register. The 2692 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

## Receiver

The 2692 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

### 2692 Register Addressing

| A3 | A2 | A1 | A0 | READ (RDN = 0) | WRITE (WRN = 0) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Mode Register A (MR1A, MR2A) | Mode Register A (MR1A, MR2A) |
| 0 | 0 | 0 | 1 | Status Register A (SRA) | Clock Select Register A (CSRA) |
| 0 | 0 | 1 | 0 | Reserved | Command Register A (CRA) |
| 0 | 0 | 1 | 1 | Rx Holding Register A (RHRA) | Tx Holding Register A (THRA) |
| 0 | 1 | 0 | 0 | Input Port Change Register (IPCR) | Aux. Control Register (ACR) |
| 0 | 1 | 0 | 1 | Interrupt Status Register (ISR) | Interrupt Mask Register (IMR) |
| 0 | 1 | 1 | 0 | Counter/Timer Upper (CTU) | C/T Upper Register (CRUR) |
| 0 | 1 | 1 | 1 | Counter/Timer Lower (CTL) | C/T Lower Register (CTLR) |
| 1 | 0 | 0 | 0 | Mode Register B (MR1B, MR2B) | Mode Register B (MR1B, MR2B) |
| 1 | 0 | 0 | 1 | Status Register B (SRB) | Clock Select Register B (CSRB) |
| 1 | 0 | 1 | 0 | Reserved | Command Register B (CRB) |
| 1 | 0 | 1 | 1 | Rx Holding Register B (RHRB) | Tx Holding Register B (THRB) |
| 1 | 1 | 0 | 0 | Reserved | Reserved |
| 1 | 1 | 0 | 1 | Input Port (IPR) | Output Port Conf. Register (OPCR) |
| 1 | 1 | 1 | 0 | Start Counter Command | Set Output Port Bits Command |
| 1 | 1 | 1 | 1 | Stop Counter Command | Reset Output Port Bits Command |

## Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

## Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

## PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1X by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1X, switches the pointer to MR2X. The pointer then remains at MR2X, so that subsequent accesses are always to MR2X unless the pointer is reset to MR1X as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'OA' should never be read during normal operation since they are reserved for internal diagnostics.

## MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

**MR1A[7] – Channel A Receiver Request-to-Send Control**

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

**MR1A[6] – Channel A Receiver Interrupt Select**

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

**MR1A[5] – Channel A Error Mode Select**

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

**MR1A[4:3] – Channel A Parity Mode Select**
If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

**MR1A[2] – Channel A Parity Type Select**
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

**MR1A[1:0] – Channel A Bits Per Character Select**
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

## MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

**MR2A[7:6] – Channel A Mode Select**
Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

3. Received data is reclocked and retransmitted on the TxDA output.
4. The receive clock is used for the transmitter.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. The Channel A TxRDY and TxEMT status bits are inactive.
7. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
8. Character framing is checked, but the stop bits are retransmitted as received.
9. A received break is echoed as received until the next valid start bit is detected.
10. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

**MR2A[5] – Channel A Transmitter Request-to-Send Control**
This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

**MR2A[4] – Channel A Clear-to-Send Control**
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

**MR2A[3:0] – Channel A Stop Bit Length Select**
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

### Table 2. Register Bit Formats

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 BIT 3 | BIT 2 | BIT 1 BIT 0 |
|---|---|---|---|---|---|---|
| | RxRTS CONTROL | RxINT SELECT | ERROR MODE | PARITY MODE | PARITY TYPE | BITS PER CHARACTER |
| MR1A MR1B | 0 = No<br>1 = Yes | 0 = RxRDY<br>1 = FFULL | 0 = Char<br>1 = Block | 00 = With Parity<br>01 = Force Parity<br>10 = No Parity<br>11 = Multidrop Mode | 0 = Even<br>1 = Odd | 00 = 5<br>01 = 6<br>10 = 7<br>11 = 8 |

| | BIT 7 BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| | CHANNEL MODE | TxRTS CONTROL | CTS ENABLE Tx | STOP BIT LENGTH* | | | |
| MR2A MR2B | 00 = Normal<br>01 = Auto-Echo<br>10 = Local loop<br>11 = Remote loop | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = 0.563<br>1 = 0.625<br>2 = 0.688<br>3 = 0.750 | 4 = 0.813<br>5 = 0.875<br>6 = 0.938<br>7 = 1.000 | 8 = 1.563<br>9 = 1.625<br>A = 1.688<br>B = 1.750 | C = 1.813<br>D = 1.875<br>E = 1.938<br>F = 2.000 |

**NOTE:**
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

| | BIT 7 BIT 6 BIT 5 BIT 4 | BIT 3 BIT 2 BIT 1 BIT 0 |
|---|---|---|
| | RECEIVER CLOCK SELECT | TRANSMITTER CLOCK SELECT |
| CSRA CSRB | See Text | See Text |

| | BIT 7 BIT 6 BIT 5 BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|
| | MISCELLANEOUS COMMANDS | DISABLE Tx | ENABLE Tx | DISABLE Rx | ENABLE Rx |
| CRA CRB | See Text | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | RECEIVED BREAK* | FRAMING ERROR* | PARITY ERROR* | OVERRUN ERROR | TxEMT | TxRDY | FFULL | RxRDY |
| SRA SRB | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

**NOTE:**
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 BIT 2 | BIT 1 BIT 0 |
|---|---|---|---|---|---|---|
| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 |
| OPCR | 0 = OPR[7]<br>1 = TxRDYB | 0 = OPR[6]<br>1 = TxRDYA | 0 = OPR[5]<br>1 = RxRDY/ FFULLB | 0 = OPR[4]<br>1 = RxRDY/ FFULLA | 00 = OPR[3]<br>01 = C/T OUTPUT<br>10 = TxCB(1X)<br>11 = RxCB(1X) | 11 = OPR[2]<br>01 = TxCA(16X)<br>10 = TxCA(1X)<br>11 = RxCA(1X) |

| | BIT 7 | BIT 6 BIT 5 BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|
| | BRG SET SELECT | COUNTER/TIMER MODE AND SOURCE | DELTA IP 3 INT | DELTA IP 2 INT | DELTA IP 1 INT | DELTA IP 0 INT |
| ACR | 0 = set 1<br>1 = set 2 | See Table 4 | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On |

**Table 2. Register Bit Formats** (Continued)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | DELTA IP 3 | DELTA IP 2 | DELTA IP 1 | DELTA IP 0 | IP 3 | IP 2 | IP 1 | IP 0 |
| IPCR | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | INPUT PORT CHANGE | DELTA BREAK B | RxRDY/ FFULLB | TxRDYB | COUNTER READY | DELTA BREAK A | RxRDY/ FFULLA | TxRDYA |
| ISR | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | IN. PORT CHANGE INT | DELTA BREAK B INT | RxRDY/ FFULLB INT | TxRDYB INT | COUNTER READY INT | DELTA BREAK A INT | RxRDY/ FFULLA INT | TxRDYA INT |
| IMR | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | C/T[15] | C/T[14] | C/T[13] | C/T[12] | C/T[11] | C/T[10] | C/T[9] | C/T[8] |
| CTUR | | | | | | | | |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | C/T[7] | C/T[6] | C/T[5] | C/T[4] | C/T[3] | C/T[2] | C/T[1] | C/T[0] |
| CTLR | | | | | | | | |

## MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## CSRA – Channel A Clock Select Register

**CSRA[7:4] – Channel A Receiver Clock Select**

This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

**CSRA[3:0] – Channel A Transmitter Clock Select**

This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

| CSRA[3:0] | ACR[7] = 0 | ACR[7] = 1 |
|---|---|---|
| 1110 | IP3-16X | IP3-16X |
| 1111 | IP3-1X | IP3-1X |

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

**Table 3. Baud Rate**

| CSRA[7:4] | ACR[7] = 0 | ACR[7] = 1 |
|---|---|---|
| 0000 | 50 | 75 |
| 0001 | 110 | 110 |
| 0010 | 134.5 | 134.5 |
| 0011 | 200 | 150 |
| 0100 | 300 | 300 |
| 0101 | 600 | 600 |
| 0110 | 1,200 | 1,200 |
| 0111 | 1,050 | 2,000 |
| 1000 | 2,400 | 2,400 |
| 1001 | 4,800 | 4,800 |
| 1010 | 7,200 | 1,800 |
| 1011 | 9,600 | 9,600 |
| 1100 | 38.4K | 19.2K |
| 1101 | Timer | Timer |
| 1110 | IP4-16X | IP4-16X |
| 1111 | IP4-1X | IP4-1X |

**NOTE:** The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

## CSRB – Channel B Clock Select Register

**CSRB[7:4] – Channel B Receiver Clock Select**
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

| CSRB[7:4] | ACR[7] = 0 | ACR[7] = 1 |
|---|---|---|
| 1110 | IP6-16X | IP6-16X |
| 1111 | IP6-1X | IP6-1X |

The transmitter clock is always a 16X clock except for CSRB[7:4] = 1111.

**CSRB[3:0] – Channel B Transmitter Clock Select**
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

| CSRB[3:4] | ACR[7] = 0 | ACR[7] = 1 |
|---|---|---|
| 1110 | IP5-16X | IP5-16X |
| 1111 | IP5-1X | IP5-1X |

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

## CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

**CRA[7:4] – Miscellaneous Commands**
The encoded value of this field may be used to specify a single command as follows:

**CRA[6:4] COMMAND**

0000 No command.
0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.
1000 Assert RTSN. Causes the RTSN output to be asserted (Low).
1001 Negate RTSN. Causes the RTSN output to be negated (High).
1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.
1011 Not used.
1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued
1101 Not used.
1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. . It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.
1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

**CRA[3] – Disable Channel A Transmitter**
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

**CRA[2] – Enable Channel A Transmitter**
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

**CRA[1] – Disable Channel A Receiver**
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

**CRA[0] – Enable Channel A Receiver**
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

## CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

## SRA – Channel A Status Register

**SRA[7] – Channel A Received Break**
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

**SRA[6] – Channel A Framing Error**
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

**SRA[5] – Channel A Parity Error**
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

**SRA[4] – Channel A Overrun Error**
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

**SRA[3] – Channel A Transmitter Empty (TxEMTA)**
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

**SRA[2] – Channel A Transmitter Ready (TxRDYA)**
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

**SRA[1] – Channel A FIFO Full (FFULLA)**
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

**SRA[0] – Channel A Receiver Ready (RxRDYA)**
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

## SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## OPCR – Output Port Configuration Register

**OPCR[7] – OP7 Output Select**
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[6] – OP6 Output Select**
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[5] – OP5 Output Select**
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[4] – OP4 Output Select**
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[3:2] – OP3 Output Select**
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

**OPCR[1:0] – OP2 Output Select**
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

## ACR – Auxiliary Control Register

**ACR[7] – Baud Rate Generator Set Select**
This bit selects one of two sets of baud rates to be generated by the BRG:

| | |
|---|---|
| Set 1: | 50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K, and 38.4K baud. |
| Set 2: | 75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud. |

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

**Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz**

| NORMAL RATE (BAUD) | ACTUAL 16X CLOCK (kHz) | ERROR (%) |
|---|---|---|
| 50 | 0.8 | 0 |
| 75 | 1.2 | 0 |
| 110 | 1.759 | -0.069 |
| 134.5 | 2.153 | 0.059 |
| 150 | 2.4 | 0 |
| 200 | 3.2 | 0 |
| 300 | 4.8 | 0 |
| 600 | 9.6 | 0 |
| 1050 | 16.756 | -0.260 |
| 1200 | 19.2 | 0 |
| 1800 | 28.8 | 0 |
| 2000 | 32.056 | 0.175 |
| 2400 | 38.4 | 0 |
| 4800 | 76.8 | 0 |
| 7200 | 115.2 | 0 |
| 9600 | 153.6 | 0 |
| 19.2K | 307.2 | 0 |
| 38.4K | 614.4 | 0 |

**NOTE:**
Duty cycle of 16X clock is 50% ± 1%.

**ACR[6:4] – Counter/Timer Mode And Clock Source Select**
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

**Table 5. ACR 6:4 Field Definition**

| ACR 6:4 | MODE | CLOCK SOURCE |
|---|---|---|
| 000 | Counter | External (IP2) |
| 001 | Counter | TxCA – 1X clock of Channel A transmitter |
| 010 | Counter | TxCB – 1X clock of Channel B transmitter |
| 011 | Counter | Crystal or external clock (X1/CLK) divided by 16 |
| 100 | Timer | External (IP2) |
| 101 | Timer | External (IP2) divided by 16 |
| 110 | Timer | Crystal or external clock (X1/CLK) |
| 111 | Timer | Crystal or external clock (X1/CLK) divided by 16 |

**ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable**
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

## IPCR – Input Port Change Register

**IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State**
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

**IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State**
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

## ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to $00_{16}$ when the DUART is reset.

**ISR[7] – Input Port Change Status**
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

**ISR[6] – Channel B Change In Break**
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

**ISR[5] – Channel B Receiver Ready or FIFO Full**
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

**ISR[4] – Channel B Transmitter Ready**
This bit is a duplicate of TxRDYB (SRB[2]).

**ISR[3] – Counter Ready.**
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

**ISR[2] – Channel A Change In Break**
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

**ISR[1] – Channel A Receiver Ready Or FIFO Full**
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

**ISR[0] – Channel A Transmitter Ready**
This bit is a duplicate of TxRDYA (SRA[2]).

## IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be

asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

## CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3-A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

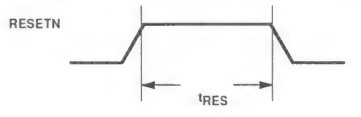



Figure 1. Reset Timing

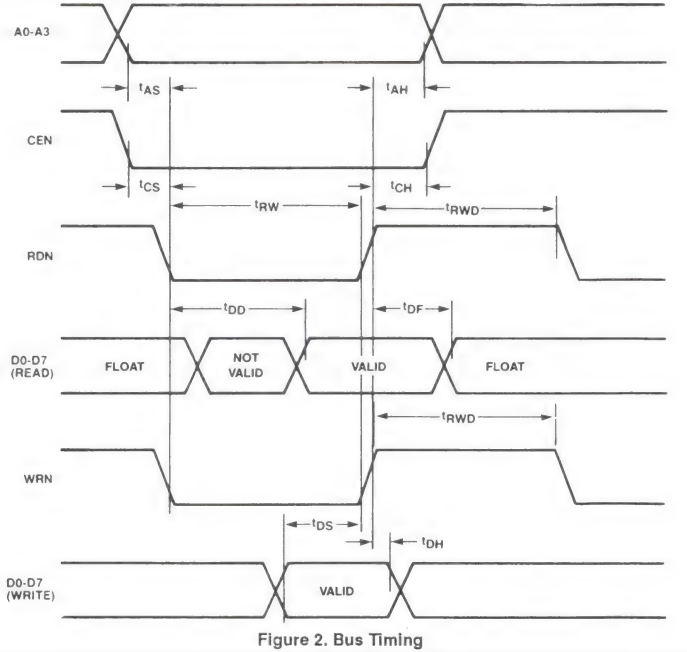



Figure 2. Bus Timing

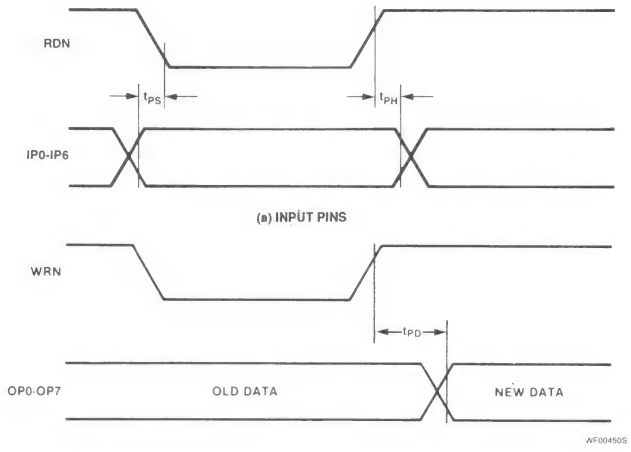
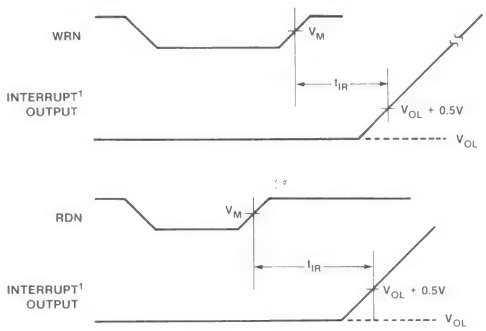
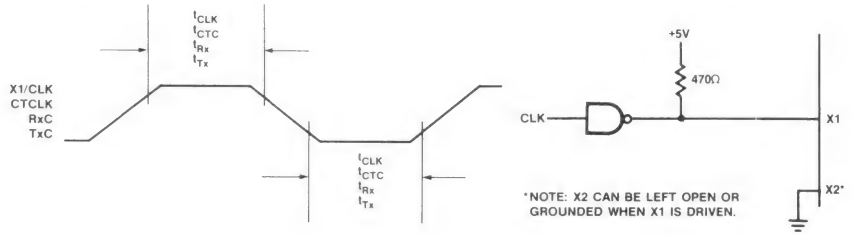


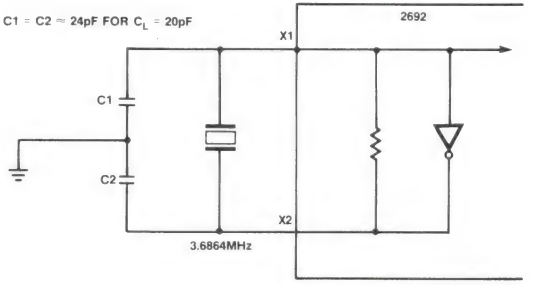

Figure 3. Port Timing




NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, $V_M$, to a point 0.5V above $V_{OL}$. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing




TYPICAL CRYSTAL SPECIFICATION

| | |
|---|---|
| FREQUENCY | 2-4 MHz |
| LOAD CAPACITANCE ($C_L$) | 12-32 pF |
| TYPE OF OPERATION | PARALLEL RESONANT, FUNDAMENTAL MODE |

**Figure 5. Clock Timing**

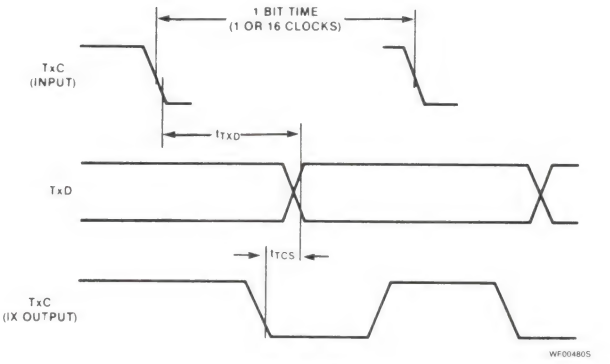



**Figure 6. Transmitter External Clocks**

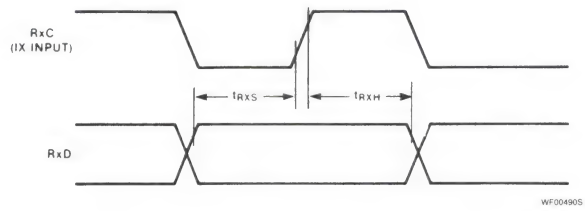
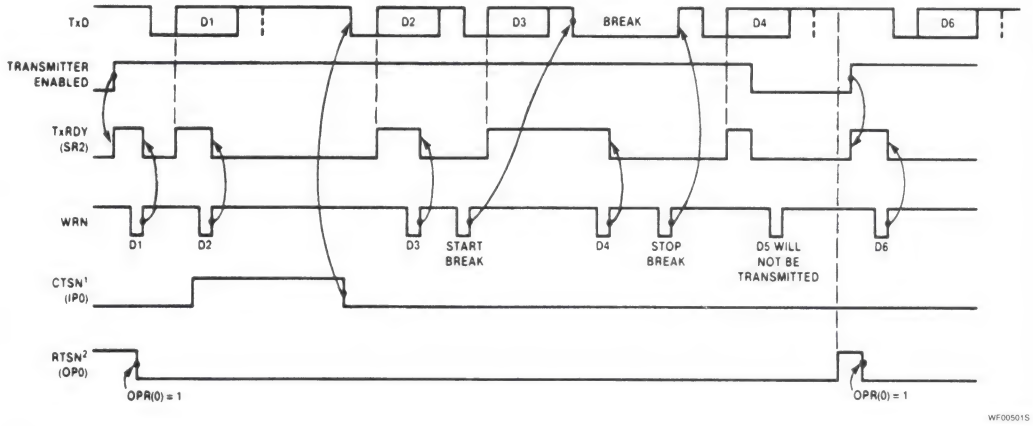
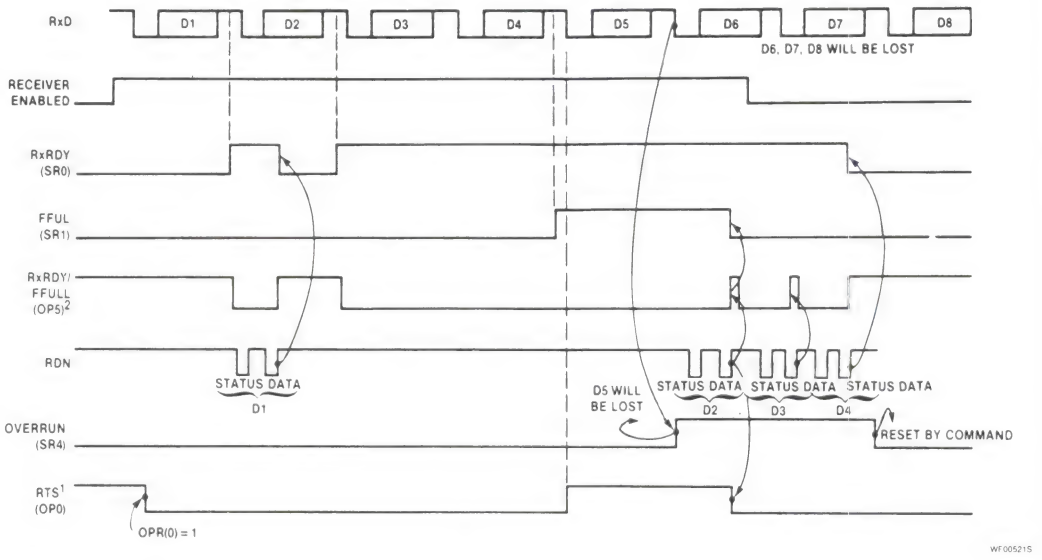



**Figure 7. Receiver External Clock**




**NOTES:**
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

**Figure 8. Transmitter Timing**




NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

**Figure 9. Receiver Timing**

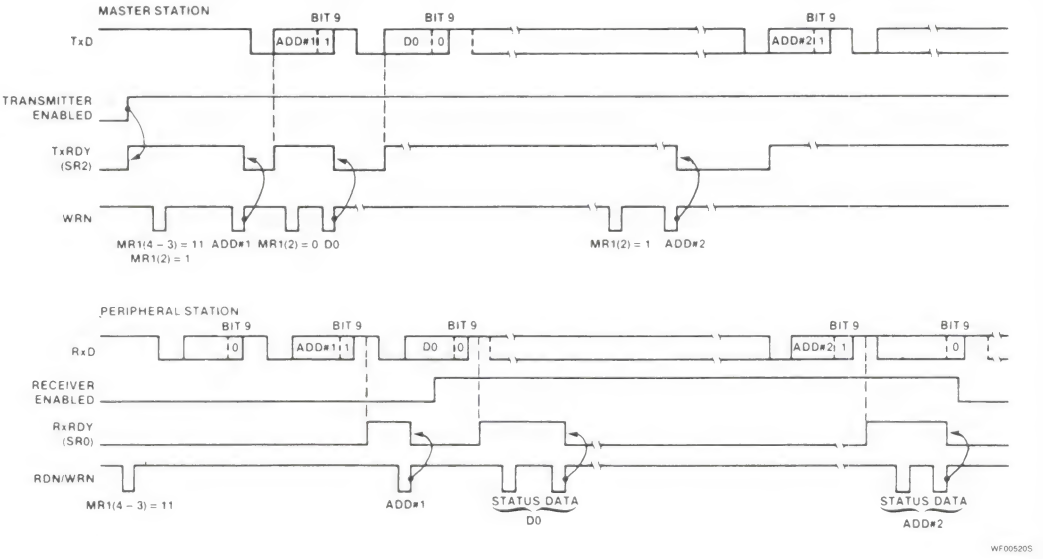



**Figure 10. Wake-Up Mode**

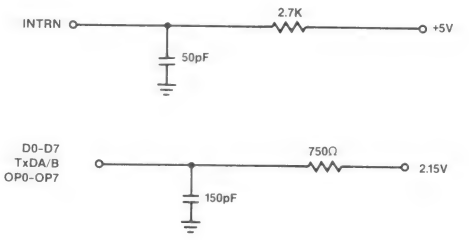



**Figure 11. Test Conditions on Outputs**

Signetics

# 2698B

## Enhanced Octal Universal Asynchronous Receiver/Transmitter (Octal UART)

*Product Specification*

**Military Communications and Industrial Products**

### DESCRIPTION

The Signetics 2698B Enhanced Octal Universal Asynchronous Receiver/Transmitter (Octal UART) is a single chip MOS-LSI communications device that provides eight full-duplex asynchronous receiver/transmitter channels in a single package. It is fabricated with Signetics CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the Octal UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

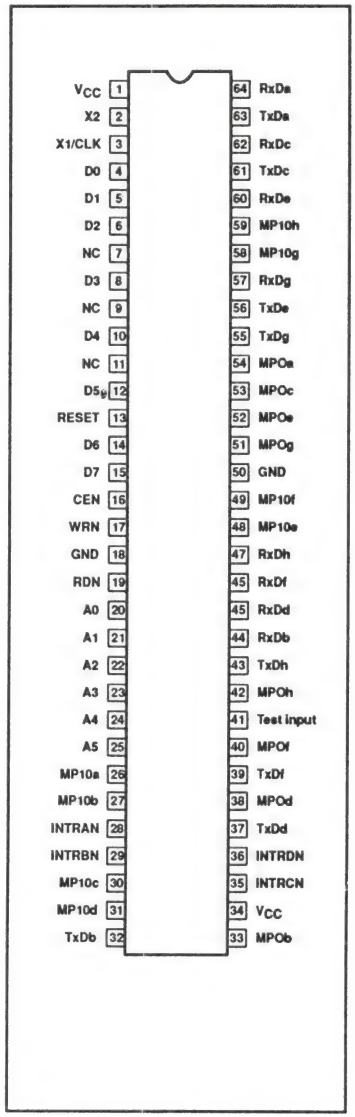
The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The Octal UART is fully TTL compatible and operates from a single +5V power supply.

The 2698B is an upwardly compatible version of the 2698A Octal UART. In LDCC packaging, it is enhanced by the addition of receiver ready or FIFO full status outputs, and transmitter empty status outputs for each channel on 16 multipurpose I/O pins. The multipurpose I/O pins of the 2698B were inputs only on the 2698A.

### FEATURES

- Eight full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud
  - User-defined rates from the programmable counter/timer associated with each of four blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Four multi-function programmable 16-bit counter/timers
- Four interrupt outputs with eight maskable interrupting conditions for each output
- Receiver ready/FIFO full and transmitter ready status available on 16 multi-function pins in LLCC package
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode

### PIN CONFIGURATIONS

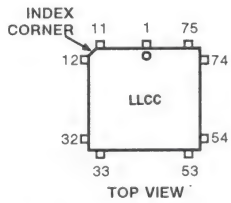


# Enhanced Octal Universal Asynchronous Receiver/Transmitter 2698B

## ORDERING INFORMATION

| DESCRIPTION | ORDERING CODE |
|---|---|
| 84–Pin LLCC | 2698B/BYA |
| 64–Pin Ceramic DIP | 2698B/BXA |
| 84–Pin Ceramic PGA | 2698B/BZA |

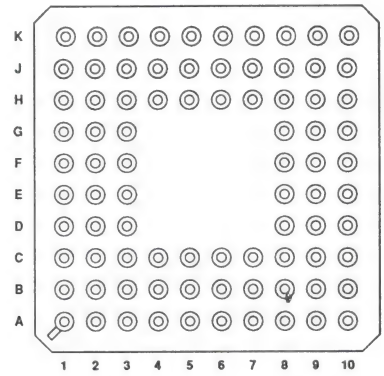
## PIN CONFIGURATION LLCC




TOP VIEW

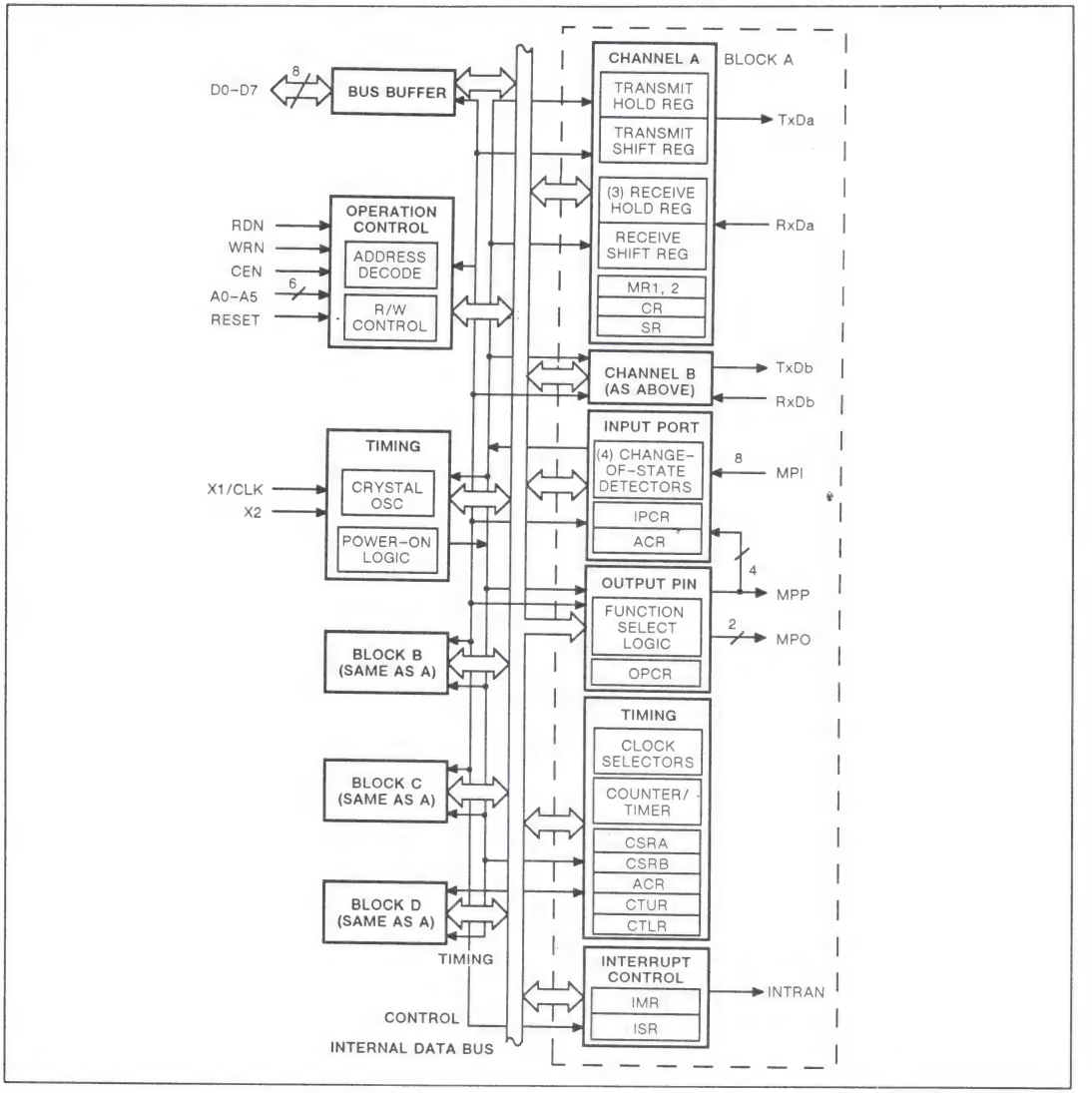
| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | TxDa | 43 | MPOb |
| 2 | MPP2g | 44 | MPP1d |
| 3 | RxDa | 45 | $V_{CC}$ |
| 4 | MPP2h | 46 | INTRCN |
| 5 | $V_{CC}$ | 47 | INTRDN |
| 6 | X2 | 48 | MPP2c |
| 7 | X1/CLK | 49 | TxDd |
| 8 | D0 | 50 | MPP2d |
| 9 | D1 | 51 | MPOd |
| 10 | D2 | 52 | TxDf |
| 11 | D3 | 53 | MPOf |
| 12 | D4 | 54 | MPOh |
| 13 | D5 | 55 | TxDh |
| 14 | MPI1a | 56 | RxDb |
| 15 | RESET | 57 | RxDd |
| 16 | D6 | 58 | RxDf |
| 17 | D7 | 59 | RxDh |
| 18 | CEN | 60 | MPI1e |
| 19 | WRN | 61 | MPI0e |
| 20 | GND | 62 | MPI1f |
| 21 | MPI1b | 63 | MPI0f |
| 22 | RDN | 64 | MPP1e |
| 23 | A0 | 65 | GND |
| 24 | MPP1a | 66 | MPP1f |
| 25 | A1 | 67 | MPOg |
| 26 | MPP1b | 68 | MPP2e |
| 27 | A2 | 69 | MPOe |
| 28 | MPP2a | 70 | MPP2f |
| 29 | A3 | 71 | MPOc |
| 30 | MPP2b | 72 | MPOa |
| 31 | A4 | 73 | TxDg |
| 32 | A5 | 74 | TxDe |
| 33 | MPI0a | 75 | RxDg |
| 34 | MPI0b | 76 | MPI0g |
| 35 | INTRAN | 77 | MPI0h |
| 36 | INTRBN | 78 | MPI1g |
| 37 | MPI0c | 79 | RxDe |
| 38 | MPI1c | 80 | MPIh |
| 39 | MPI0d | 81 | TxDc |
| 40 | MPI1d | 82 | MPP1g |
| 41 | TxDb | 83 | RxDc |
| 42 | MPP1c | 84 | MPP1h |

## PIN CONFIGURATION PGA




| Pin No. | Function | Pin No. | Function | Pin No. | Function |
|---|---|---|---|---|---|
| C3 | D4 | J5 | MPI1d | C10 | MPI3e |
| C2 | D5 | H5 | TXDb | D9 | MP0e |
| B1 | MPI1a | K5 | MPI2c | B10 | MPI3f |
| C1 | RESET | K6 | MP0b | D8 | MPOc |
| D3 | D6 | J6 | MPI2d | A10 | MPOa |
| D2 | D7 | H6 | VCC | C9 | TXDg |
| D1 | CEN | K7 | INTR2N | B9 | TXDe |
| E2 | WRN | K8 | INTR3N | C8 | RXDg |
| E3 | GND | J7 | MPI3c | B8 | MPI0g |
| E1 | MPI1b | K9 | TXDd | A9 | MPI0h |
| F1 | RDN | H7 | MPI3d | A8 | MPI1g |
| F2 | AC | K10 | MP0d | C7 | RXd3 |
| F3 | MPI2a | J8 | TXDf | B7 | MPI1h |
| G1 | A1 | J9 | MP0f | A7 | TXDc |
| H1 | MPI2b | H8 | MP0h | B6 | MPI2g |
| G2 | A2 | H9 | TXDh | C6 | RXDc |
| J1 | MPI3a | J10 | RXDb | A6 | MPI2h |
| G3 | A3 | H10 | RXDd | A5 | TXDa |
| K1 | MPI13b | G8 | RXDf | B5 | MPI13g |
| H2 | A4 | G9 | RXDh | C5 | RXDa |
| J2 | A5 | G10 | MPI1e | A4 | MPI13h |
| H3 | MPI0a | F9 | MPI0e | A3 | VCC |
| J3 | MPI0b | F8 | MPI1f | B4 | X2 |
| K2 | INTR0N | F10 | MPI0f | A2 | X1/CLK |
| K9 | INTR1N | E10 | MPI2e | C4 | D0 |
| H4 | MPIOc | E9 | GND | A1 | D1 |
| J4 | MPI1c | E8 | MPI2f | B3 | D2 |
| K4 | MPI0d | D10 | MP0g | B2 | D3 |

## BLOCK DIAGRAM



## PIN DESCRIPTION

| MNEMONIC | PIN NO. DIP | PIN NO. LDCC | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|
| D0–D7 | 4–6, 8, 10, 12, 14, 15 | 8–13, 16, 17 | I/O | **Data Bus:** Active–High 8-bit bidirectional 3-state data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the Octal UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is High, the data bus is in the 3-state condition. |
| CEN | 16 | 18 | I | **Chip Enable:** Active-Low input. When Low, data transfers between the CPU and the Octal UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A5 inputs. When CEN is High, the Octal UART is effectively isolated from the data bus and D0–D7 are placed in the 3-state condition. |
| WRN | 17 | 19 | I | **Write Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the data bus to be transferred to the register selected by A0–A5. The transfer occurs on the trailing (rising) edge of the signal. |
| RDN | 19 | 22 | I | **Read Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the register selected by A0–A5 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN. |
| A0–A5 | 20–25 | 23, 25, 27, 29, 31, 32 | I | **Address Inputs:** Active-High address inputs to select the Octal UART registers for read/write operations. |
| RESET | 13 | 15 | I | **Reset:** Master reset. A High on this pin clears the status register (SR), clears the interrupt mask register (IMR), clears the interrupt status register (ISR), clears the output port configuration register (OPCR), places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (High) state, and stops the counter/timer. |
| INTRAN–INTRDN | 28, 29, 35, 36 | 35, 36, 46, 47 | O | **Interrupt Request:** This active-Low open drain output is asserted on occurrence of one or more of eight maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s). |
| X1/CLK | 3 | 7 | I | **Crystal 1:** Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip. |
| X2 | 2 | 6 | I | **Crystal 2:** Connection for other side of crystal. If an external source is used instead of a crystal, this connection should be left open (see Figure 7). |
| RxDa–RxDh | 64, 44, 62, 45, 60, 46, 57, 47 | 3, 56, 83, 57, 79, 58, 75, 59 | I | **Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock. |
| TxDa–TxDh | 63, 32, 61, 37, 56, 39, 55, 43 | 1, 41, 81, 49, 74, 52, 73, 55 | O | **Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is idle or disabled and when the Octal UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock. |
| MPOa–MPOh | 54, 33, 53, 38, 52, 40, 51, 42 | 72, 43, 71, 51, 69, 53, 67, 54 | O | **Multi-Purpose Output:** One of the following functions can be selected for this output pin by programming the auxiliary control register:<br>**RTSN –** Request to send active-Low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full.<br>**C/TO –** The counter/timer output.<br>**TxC1X –** The 1X clock for the transmitter.<br>**TxC16X –** The 16X clock for the transmitter.<br>**RxC1X –** The 1X clock for the receiver.<br>**RxC16X –** The 16X clock for the receiver.<br>**TxRDY –** Transmitter holding register empty signal.<br>**RxRDY/FFULL –** Receiver FIFO not empty/full signal. |
| MPI0a–MPI0h | 26, 27, 30, 31, 48, 49, 58, 59 | 33, 34, 37, 39, 61, 63, 76, 77 | I | **Multi-Purpose Input 0:** This pin can be programmed to serve as an input for one of the following functions:<br>**GPI –** General purpose input. The current state of the pin can be determined by reading the IPCR or input port register.<br>**CTSN –** Clear-to-send active-Low input. |

## PIN DESCRIPTION (Continued)

| MNEMONIC | PIN NO. DIP | PIN NO. LDCC | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|
| MPI1a–MPI1h | NC | 14, 21, 38, 40, 60, 62, 78, 80 | I | **Multi–Purpose Input 1:** This pin can be programmed to serve as an input for one of the following functions:<br>**GPI –** General putpose input. The current state of the pin can be determined by reading the IPCR or input port register.<br>**CTCLK –** Counter/timer external clock input. Only channels a, c, e, and g change to C/T inputs; channels b, d, f, and h stay GPI. |
| MPP1a–MPP1h | NC | 24, 26, 42, 44, 64, 66, 82, 84 | I/O | **Multi–Purpose Pin 1:** This pin can be programmed to serve as an input or output for the following functions:<br>**GPI –** General purpose input: This is the default condition for this pin. The current state of the pin can be determined by reading the input port register.<br>**TCLK:** Transmitter external clock input. This may be a 1X or 16X clock as programmed by CSR[3:0].<br>**TxRDY:** Active-Low open drain output. Transmitter holding register empty signal. This function is selected for this pin by programming OPCR[7] – 1. |
| MPP2a–MPP2h | NC | 28, 30, 48, 50, 68, 70, 2, 4 | I/O | **Multi–Purpose Pin 2:** This pin can be programmed to serve as an input or output for the following functions:<br>**GPI:** General putpose input: This is the default condition for this pin. The current state of the pin can be determined by reading the input port register.<br>**RCLK:** Receiver external clock input. This may be a 1X or 16X clock as programmed by CSR[7:4].<br>**RxRDY.FFULL:** Active-Low open drain output. Receiver FIFO not empty/full signal. This function is selecteed for this pin by programming OPCR[7] – 1. |
| Test Input | 41 | – | I | **Test Input:** This pin is used as an input for test purposes at the factory while in test mode. This pin can be treated as 'N/C' by the user. It can be tied high, tied low, or left open. |
| $V_{CC}$ | 1, 34 | 5, 45 | I | **Power Supply:** +5V supply input. |
| GND | 18, 50 | 20, 65 | I | **Ground** |

## BLOCK DIAGRAM

As shown in the block diagram, the Octal UART consists of: data bus buffer, interrupt control, operation control, timing, and eight receiver and transmitter channels. The eight channels are divided into four different blocks, each block independent of each other (see Figure 1).

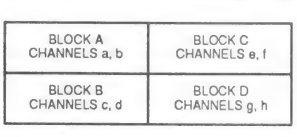



**Figure 1. Channel Architecture**

### Channel Blocks

There are four blocks (Figure 1), each containing two sets of receiver/transmitters. In the following discussion, the description applies to Block A which contains channels a and b. However, the same information applies to all channel blocks.

### Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the Octal UART.

### Interrupt Control

A single interrupt output per block (INTRN) is provided which is asserted on occurrence of any of the following internal events:

- Transmit holding register ready for each channel
- Receive holding register ready or FIFO full for each channel
- Change in break received status for each channel
- Counter reached terminal count
- Change in MPI input

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR can be programmed to select only certain conditions, of the above, to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. However, the bits of the ISR are not masked by the IMR. The transmitter ready status and the receiver ready or FIFO full status can be proveded on MPP1a, MPP1b, MPP2a, and MPP2b by setting OPCR[7]. these outputs are not masked by IMR.

### Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers 1 and 2 are accessed via an auxiliary pointer. The pointer is set to MR1 by RESET or by issuing a reset pointer command via the command register. Any read or write of the mode register while the pointer is at MR1 switches the pointer to MR2. The pointer then remains at MR2 so that subsequent accesses are to MR2, unless the pointer is reset to MR1 as already described.

### Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer for each block, and two clock selectors.

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1 must be driven and X2 left floating as shown in Figure 7. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

**Table 1. Register Addressing**

| A5 | A4 | A3 | A2 | A1 | A0 | READ (RDN=0) | WRITE (WRN=0) | A5 | A4 | A3 | A2 | A1 | A0 | READ (RDN=0) | WRITE (WRN=0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | MR1a, MR2a | MR1a, MR2a | 1 | 0 | 0 | 0 | 0 | 0 | MR1e, MR2e | MR1e, MR2e |
| 0 | 0 | 0 | 0 | 0 | 1 | SRa | CSRa | 1 | 0 | 0 | 0 | 0 | 1 | SRe | CSRe |
| 0 | 0 | 0 | 0 | 1 | 0 | Reserved* | CRa | 1 | 0 | 0 | 0 | 1 | 0 | Reserved* | CRe |
| 0 | 0 | 0 | 0 | 1 | 1 | RHRa | THRa | 1 | 0 | 0 | 0 | 1 | 1 | RHRe | THRe |
| 0 | 0 | 0 | 1 | 0 | 0 | IPCRA | ACRA | 1 | 0 | 0 | 1 | 0 | 0 | IPCRC | ACRC |
| 0 | 0 | 0 | 1 | 0 | 1 | ISRA | IMRA | 1 | 0 | 0 | 1 | 0 | 1 | ISRC | IMRC |
| 0 | 0 | 0 | 1 | 1 | 0 | CTUA | CTURA | 1 | 0 | 0 | 1 | 1 | 0 | CTUC | CTURC |
| 0 | 0 | 0 | 1 | 1 | 1 | CTLA | CTLRA | 1 | 0 | 0 | 1 | 1 | 1 | CTLC | CTLRC |
| 0 | 0 | 1 | 0 | 0 | 0 | MR1b, MR2b | MR1b, MR2b | 1 | 0 | 1 | 0 | 0 | 0 | MR1f, MR2f | MR1f, MR2f |
| 0 | 0 | 1 | 0 | 0 | 1 | SRb | CSRb | 1 | 0 | 1 | 0 | 0 | 1 | SRf | CSRf |
| 0 | 0 | 1 | 0 | 1 | 0 | Reserved* | CRb | 1 | 0 | 1 | 0 | 1 | 0 | Reserved* | CRf |
| 0 | 0 | 1 | 0 | 1 | 1 | RHRb | THRb | 1 | 0 | 1 | 0 | 1 | 1 | RHRf | THRf |
| 0 | 0 | 1 | 1 | 0 | 0 | Reserved* | Reserved* | 1 | 0 | 1 | 1 | 0 | 0 | Reserved* | Reserved* |
| 0 | 0 | 1 | 1 | 0 | 1 | Input port A | OPCRA | 1 | 0 | 1 | 1 | 0 | 1 | Input port C | OPCRC |
| 0 | 0 | 1 | 1 | 1 | 0 | Start C/T A | Reserved* | 1 | 0 | 1 | 1 | 1 | 0 | Start C/T C | Reserved* |
| 0 | 0 | 1 | 1 | 1 | 1 | Stop C/T A | Reserved* | 1 | 0 | 1 | 1 | 1 | 1 | Stop C/T C | Reserved* |
| 0 | 1 | 0 | 0 | 0 | 0 | MR1c, MR2c | MR1c, MR2c | 1 | 1 | 0 | 0 | 0 | 0 | MR1g, MR2g | MR1g, MR2g |
| 0 | 1 | 0 | 0 | 0 | 1 | SRc | CSRc | 1 | 1 | 0 | 0 | 0 | 1 | SRg | CSRg |
| 0 | 1 | 0 | 0 | 1 | 0 | Reserved* | CRc | 1 | 1 | 0 | 0 | 1 | 0 | Reserved* | CRg |
| 0 | 1 | 0 | 0 | 1 | 1 | RHRc | THRc | 1 | 1 | 0 | 0 | 1 | 1 | RHRg | THRg |
| 0 | 1 | 0 | 1 | 0 | 0 | IPCRB | ACRB | 1 | 1 | 0 | 1 | 0 | 0 | IPCRD | ACRD |
| 0 | 1 | 0 | 1 | 0 | 1 | ISRB | IMRB | 1 | 1 | 0 | 1 | 0 | 1 | ISRD | IMRD |
| 0 | 1 | 0 | 1 | 1 | 0 | CTUB | CTURB | 1 | 1 | 0 | 1 | 1 | 0 | CTUD | CTURD |
| 0 | 1 | 0 | 1 | 1 | 1 | CTLB | CTLRB | 1 | 1 | 0 | 1 | 1 | 1 | CTLD | CTLRD |
| 0 | 1 | 1 | 0 | 0 | 0 | MR1d, MR2d | MR1d, MR2d | 1 | 1 | 1 | 0 | 0 | 0 | MR1h, MR2h | MR1h, MR2h |
| 0 | 1 | 1 | 0 | 0 | 1 | SRd | CSRd | 1 | 1 | 1 | 0 | 0 | 1 | SRh | CSRh |
| 0 | 1 | 1 | 0 | 1 | 0 | Reserved* | CRd | 1 | 1 | 1 | 0 | 1 | 0 | Reserved* | CRh |
| 0 | 1 | 1 | 0 | 1 | 1 | RHRd | THRd | 1 | 1 | 1 | 0 | 1 | 1 | RHRh | THRh |
| 0 | 1 | 1 | 1 | 0 | 0 | Reserved* | Reserved* | 1 | 1 | 1 | 1 | 0 | 0 | Reserved* | Reserved* |
| 0 | 1 | 1 | 1 | 0 | 1 | Input port B | OPCRB | 1 | 1 | 1 | 1 | 0 | 1 | Input port D | OPCRD |
| 0 | 1 | 1 | 1 | 1 | 0 | Start C/T B | Reserved* | 1 | 1 | 1 | 1 | 1 | 0 | Start C/T D | Reserved* |
| 0 | 1 | 1 | 1 | 1 | 1 | Stop C/T B | Reserved* | 1 | 1 | 1 | 1 | 1 | 1 | Stop C/T D | Reserved* |

**NOTE:**
*Reserved registers should never be read during normal operation since they are reserved for internal diagnostics.

ACR = Auxiliary control register
CR = Command register
CSR = Clock select register
CTL = Counter/timer lower
CTLR = Counter/timer lower register
CTU = Counter/timer upper
CTUR = Counter/timer upper register
MR = Mode register
SR = Status Register
THR = Tx holding register
RHR = Rx holding register
IPCR = Input port change register
ISR = Interrupt status register
IMR = Interrupt mask register
OPCR= Output port configuration registerr

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

There are four C/Ts in the Octal UART, one for each block. The C/T operation is programmed by ACR[6:4]. One of eight timing sources can be used as the input to the C/T. The output of the C/T is available to the clock selectors and can also be programmed by OPCR[2:0] for channel a and OPCR[6:4] for channel b, to be output on the MPOa or MPOb pin respectively.

A register read address is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop counter/timer command for each timer. For example, to issue a stop counter command for the counter-timer in block B, a read of address '1F' must be performed. See Table 1 for register addressing.

In the timer mode, the C/T generates a square wave whose period is twice the number of clock periods loaded into the C/T upper and lower registers. The counter ready bit in the ISR is set once each cycle of the square wave. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be affected. In this mode the C/T runs continuously and does not recognize the stop C/T command (the command only resets the counter ready bit in the ISR). Receipt of a start C/T command causes the counter to ter-

minate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a start counter command. Upon reaching terminal count, the counter ready bit in the ISR is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and the counter ready bit is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command following a stop counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter are read. However, a subsequent start counter command causes the counter to begin a new count cycle using the values in CTUR and CTLR.

## Receiver and Transmitter

The Octal UART has eight full-duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

Registers associated with the communications channel are the mode registers (MR1 and MR2), the clock select register (CSR), the command register (CR), the status register (SR), the transmit holding register (THR), and the receive holding register (RHR).

### Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the THR. In the 16X clock mode, this also resynchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous Low condition) by issuing a start break command via the CR. The break is terminated by a stop break command. If the transmitter is disabled, it continues operating until the characters currently being transmitted and the character in the THR, if any, are completely sent out. Characters cannot be loaded in the THR while the transmitter is disabled.

### Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode).

If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver samples the input. This continues at one bit time intervals, at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The data is then transferred to the RHR and the RxRDY bit in the SR is set to a one. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

## TIMEOUT MODE

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know when there is data left in the FIFO, The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after one C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received.

## RECEIVER FIFO

The RHR consists of a first-in-first-out (FIFO) with a capacity of three characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR, outputs the data at the top of the FIFO. After the read cycle, the data

FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

## WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the Octal UART incorporates a special mode which provides automatic wake-up of the receiver through address frame recognition for multiprocessor communications. This mode is selected by programming bits MR1[4:3] to '11'.

In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and 'wake-up' the CPU [by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]; MR1[2] = 0 transmits a zero in the A/D bit position which identifies the corresponding data bits as data; MR1[2] = 1 transmits a one in the A/D bit position which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits in the THR.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RHR FIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RHR. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

## MULTI-PURPOSE INPUT PIN AND MULTI-PURPOSE I/O PINS

The inputs to this unlatched 8-bit port for each block can be read by the CPU, by performing a read operation as shown in Table 1. A High input results in a logic one, while a Low input results in a logic zero. When the input port pins are read on the 84-pin LLCC, they will appear on the data bus in alternating pairs (i.e., DB0 = MP10a, DB1 = MPI1a, DB2 = MPI0b, DB3 = MPI1b, DB4 = MPP1a, DB5 = MPP2a, DB6 = MPP1b, DB7 = MPP2b. Although this example is shown for input port 'A', all ports will have a similar order).

The MPI pin can be programmed as an input to one of several Octal UART circuits. The function of the pin is selected by programming the appropriate control register. Change-of-state detectors are provided for MPI0 and MPI1 for each channel in each block. A High-to-Low or Low-to-High transition of the inputs lasting longer than 25 to 50µs sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register.

The input port pulse detection circuitry uses a 38.4KHz sampling clock, derived from one of the baud rate generator taps. This produces a sampling period of slightly more than 25µs (assuming a 3.6864MHz oscillator input). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples be observed at the new logic level. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. (The 50µs time refers to the condition where the change-of-state is just missed and the first change of state is not detected until after an additional 25µs.)

The multi-purpose pins can be programmed as inputs or outputs using OPCR[7]. When programmed as inputs, the functions of the pins are selected by programming the appropriate control registers. When programmed as outputs, the two MPP1 pins (per block) will provide the transmitter ready (TxRDY) status for each channel and the MPP2 pins will provide the receiver ready or FIFO full (RxRDY/FFULL) status for each channel.

## MULT-PURPOSE OUTPUT PIN

This pin can be programmed to serve as a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TxRDY output or the RxRDY/FFULL output (see OPCR[2:0] and OPCR[6:4] – MPO Output Select).

## REGISTERS

The operation of the Octal UART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is described in Table 1.

The bit formats of the Octal UART registers are depicted in Table 2. These are shown for block A. The bit format for the other blocks is the same.

## MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via the CR. After reading or writing MR1, the pointers are set at MR2.

**MR1[7] – Receiver Request-to-Send Control**

This bit controls the deactivation of the RTSN output (MPO) by the receiver. This output is manually asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is reasserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

**MR1[6] – Receiver Interrupt Select**

This bit selects either the receiver ready status (RxRDY) or the FIFO full status (FFULL) to be used for CPU interrupts.

**MR1[5] – Error Mode Select**
This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

**MR1[4:3] – Parity Mode Select**
If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake-up mode.

**MR1[2] – Parity Type Select**
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special 'wake-up' mode, it selects the polarity of the transmitted A/D bit.

**MR1[1:0] – Bits Per Character Select**
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

## MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

**MR2[7:6] – Mode Select**

The Octal UART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

7. Received data is reclocked and retransmitted on the TxD output.
8. The receive clock is used for the transmitter.
9. The receiver must be enabled, but the transmitter need not be enabled.
10. The TxRDY and TxEMT status bits are inactive.
11. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
12. Character framing is checked, but the stop bits are retransmitted as received.
13. A received break is echoed as received until the next valid start bit is detected.
14. CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled.

## Table 2. Register Bit Formats

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|

**MR1 (Mode Register 1)**

| RxRTS Control | RxINT Select | Error Mode | Parity Mode | Parity Type | Bits per Character |
|---|---|---|---|---|---|
| 0 = No<br>1 = Yes | 0 = RxRDY<br>1 = FFULL | 0 = Char<br>1 = Block | 00 = With parity<br>01 = Force parity<br>10 = No parity<br>11 = Special mode | 0 = Even<br>1 = Odd | 00 = 5<br>01 = 6<br>10 = 7<br>11 = 8 |

**MR2 (Mode Register 2)**

| Channel Mode | TxRTS Conrol | CTS Enable Tx | Stop Bit Length* |
|---|---|---|---|
| 00 = Normal<br>01 = Auto-echo<br>10 = Local loop<br>11 = Remote loop | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = 0.563 4 = 0.813 8 = 1.563 C = 1.813<br>1 = 0.625 5 = 0.875 9 = 1.625 C = 1.875<br>2 = 0.688 6 = 0.938 A = 1.688 E = 1.938<br>3 = 0.750 7 = 1.000 B = 1.750 F = 2.000 |

NOTE:
*Add 0.5 to values shown above for 0–7, if channel is programmed for 5 bits/char.

**CSR (Clock Select Register)**

| Receiver Clock Select | Transmitter Clock Select |
|---|---|
| See text | See text |

**CR (Command Register)**

| Miscellaneous Commands | Disable Tx | Enable Tx | Disable Rx | Enable Rx |
|---|---|---|---|---|
| See text | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

**SR (Status Register)**

| Rec'd. Break | Framing Error | Parity Error | Overrun Error | TxEMT | TxRDY | FFULL | RxRDY |
|---|---|---|---|---|---|---|---|
| 0 = No<br>1 = Yes* | 0 = No<br>1 = Yes* | 0 = No<br>1 = Yes* | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

NOTE:
*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. In character mode, they must be reset when the corresponding data character is read from the FIFO.

**OPCR (Output Port Configuration Register)**

| MPP Function Select | MPOb Pin Function Select | Power–Down Mode | MPOa Pin Function Select |
|---|---|---|---|
| 0 = input<br>1 = output | 000 = RTSN<br>001 = C/TO<br>010 = TxC (1X)<br>011 = TxC (16X)<br>100 = RxC (1X)<br>101 = RxC (16X0<br>110 = TxRDY<br>111 = RxRDY/FF | 0 = Off<br>1 = On* | 000 = RTSN<br>001 = C/TO<br>010 = TxC (1X)<br>011 = TxC (16X)<br>100 = RxC (1X)<br>101 = RxC (16X)<br>110 = TxRDY<br>111 = RxRDY/FF |

NOTE:
*Only OPCR[3] in block A controls the power-down mode.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TXD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

When switching in and out of the various modes, the selected mode is activated at the completion of all transmitted and received characters. Likewise, if a mode is deselected, the device will switch out of the mode at the completion of all transmit and/or receive characters.

**MR2[5] – Transmitter Request-to–Send Control**

This bit controls the deactivation of the RTSN output (MPO) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the THR (if any) are completely transmitted (includes the programmed number of stop bits if the transmitter is not enabled). This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Verify the next to last character of the message is being sent by waiting until transmitter ready is asserted. Disable transmitter after the last character of the message is loaded in the THR.

**Table 2. Register Bit Formats** (Continued)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|

**ACR (Auxiliary Control Register)**

| BRG Set Select | Counter/Timer Mode and Source | | Delta MPI1bINT | Delta MPI0bINT | Delta MPI1aINT | Delta MPI0aINT |
|---|---|---|---|---|---|---|
| 0 = set 1<br>1 = set 2 | See text | | 0 = off<br>1 = on | 0 = off<br>1 = on | 0 = off<br>1 = on | 0 = off<br>1 = on |

**IPCR (Input Port Change Register)**

| Delta MPI1b | Delta MPI0b | Delta MPI1a | Delta MPI0a | MPI1b | MPI0b | MPI1a | MPI0a |
|---|---|---|---|---|---|---|---|
| 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High |

**ISR (Interrupt Status Register)**

| MPI Port Change | Delta BREAKb | RxRDY/ FFULLb | TxRDYb | Counter Ready | Delta BREAKa | RxRDY/ FFULLa | TxRDYa |
|---|---|---|---|---|---|---|---|
| 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

**IMR (Interrupt Mask Register)**

| MPI Port Change INT | Delta BREAKb INT | RxRDY/ FFULLb INT | TxRDYb INT | Counter Ready INT | Delta BREAKa INT | RxRDY/ FFULLa INT | TxRDYa INT |
|---|---|---|---|---|---|---|---|
| 0 = off<br>1 = on | 0 = off<br>1 = on | 0 = off<br>1 = on | 0 = off<br>1 = on | 0 = off<br>1 = on | 0 = off<br>1 = on | 0 = off<br>1 = on | 0 = off<br>1 = on |

**CTUR (Counter/Timer Upper Register)**

| C/T[15] | C/T[14] | C/T[13] | C/T[12] | C/T[11] | C/T[10] | C/T[9] | C/T[8] |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

**CTUR (Counter/Timer Lower Register)**

| C/T[7] | C/T[6] | C/T[5] | C/T[4] | C/T[3] | C/T[2] | C/T[1] | C/T[0] |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

**IPR (Input Port Register)**

| MPP2b | MPP1b | MPP2a | MPP1a | MPI1b | MPI0b | MPI1a | MPI0a |
|---|---|---|---|---|---|---|---|
| 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High |

6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

**MR2[4] – Clear-to-Send Control**

The sate of this bit determines if the CTSN input (MPI) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (Low), the character is transmitted. If it is negated (High), the TxD output remains in the marking state and the transmission is delayed until CTSN goes Low. Changes in CTSN, while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

**MR2[3:0] – Stop Bit Length Select**

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one

stop bit and MR2[3] = 1 selects two stop bits to be transmittted.

## CSR – Clock Select Register

**CSR[7:4] – Receiver Clock Select**
When using a 3.6864MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

### Table 3. Baud Rate

| CSR[7:4] | ACR[7] = 0 | ACR[7] = 1 |
|---|---|---|
| 0 0 0 0 | 50 | 75 |
| 0 0 0 1 | 110 | 110 |
| 0 0 1 0 | 134.5 | 38.4k |
| 0 0 1 1 | 200 | 150 |
| 0 1 0 0 | 300 | 300 |
| 0 1 0 1 | 600 | 600 |
| 0 1 1 0 | 1,200 | 1,200 |
| 0 1 1 1 | 1,050 | 2,000 |
| 1 0 0 0 | 2,400 | 2,400 |
| 1 0 0 1 | 4,800 | 4,800 |
| 1 0 1 0 | 7,200 | 1,800 |
| 1 0 1 1 | 9,600 | 9,600 |
| 1 1 0 0 | 38.4k | 19.2k |
| 1 1 0 1 | Timer | Timer |
| 1 1 1 0 | MP2 – 16X | MP2 – 16X |
| 1 1 1 1 | MP2 – 1X | MP2 – 1X |

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111. When MPP2 is selected as the input, MPP2a is for channel a and MPP2b is for channel b.

**CSR[3:] – Transmitter Clock Select**
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3, except as follows:

| CSR[3:0] | ACR[7] = 0 | ACR[7] = 1 |
|---|---|---|
| 1 1 1 0 | MPP1 – 16X | MPP1 – 16X |
| 1 1 1 1 | MPP1 – 1X | MPP1 – 1X |

When MPP1 is selected as the input, MPP1a is for channel a and MPP1b is for channel b.

## CR – Command Register

CR is used to write commands to the Octal UART.

**CR[7:4] – Miscellaneous Commands**
The encoded value of this field can be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the MR pointer to point to MR1.

0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location.

0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2 or 6]) to be cleared to zero.

0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the THR, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break

0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The register in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Reserved.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued.

1101 Reserved.

111x Reserved for testing.

**CR[3] – Disable Transmitter**
This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

**CR[2] – Enable Transmitter**
Enables operation of the transmitter. The TxRDY status bit will be asserted.

**CR[1] – Disable Receiver**
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake–up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

**CR[0] – Enable Receiver**
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

## SR – Channel Status Register

**SR[7] – Received Break**
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the change in break bit in the ISR (ISR[6 or 2]) is set. ISR[6 or 2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

**SR[6] – Framing Error (FE)**
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

**SR[5]– Parity Error (PE)**
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special 'wake-up mode', the parity error bit stores the received A/D bit.

**SR[4] – Overrun Error (OE)**
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

**SR[3] – Transmitter Empty (TxEMT)**
This bit will be set when the transmitter underruns, i.e., both the transmit holding register and the transmit shift register are empty. However, this bit is not set until one character has been transmitted. It is set after transmission of the last stop bit of a character, If no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU, or when the transmitter is disabled.

**SR[2] – Transmitter Ready (TxRDY)**
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the THR while the transmitter is disabled will not be transmitted.

**SR[1] – FIFO Full (FFULL)**
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL is not reset after reading the FIFO once.

**SR[0] – Receiver Ready (RxRDY)**
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, and no more characters are in the FIFO.

## OPCR – Output Port Configuration Register

**OPCR[7] – MPP Function Select**
When this bit is a zero, the MPP pins function as inputs, to be used as general purpose inputs or as receiver or transmitter external clock inputs. When this bit is set, the MPP pins function as outputs. MPP1 will be a TxRDY indicator, and MPP2 will be an RxRDY/FFULL indicator.

**OPCR[6:4] – MPOb Output Select**
This field programs the MPOb output pin to provide one of the following:

000 Request-to-send active-Low output (RTSN). This output is asserted and negated via the command register. Mode RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted out or when the receiver FIFO and receiver shift register are full using MR2[5] and MR1[7], respectively.

001 The counter/timer output. In the timer mode, this output is a square wave with a period of twice the value (in clock periods) of the contents of the CTUR and CTLR. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. The output returns to the High state when the counter is stopped by a stop counter command.

010 The 1X clock for the transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a non-synchronized 1X clock is output.

011 The 16X clock for the transmitter. This is the clock selected by CSR[3:0], and is a 1X clock if CSR[3:0] = 1111.

100 The 1X clock for the receiver, which is the clock that samples the received data. If data is not being received, a non-synchronized 1X clock is output.

101 The 16X clock for the receiver. This is the clock selected by CSR[7:4], and is a 1X clock if CSR[7:4] = 1111.

110 The transmitter register empty signal, which is the same as SR[3].

111 The receiver ready or FIFO full signal.

**OPCR[3] – Power Down Mode Select**
This bit, when set, selects the power-down mode. In this mode, the 2698B oscillator is stopped and all functions requiring this clock are suspended. The contents of all registers are saved. It is recommended that the transmitter and receiver be disabled prior to placing the 2698B in this mode. This bit is reset with RESET asserted. Note that this bit must be set to a logic 1 after power up. Only OPCR[3] in block A controls the power-down mode.

**OPCR[2:0] – MPOa Output Select**
This field programs the MPOa output pin to provide one of the same functions as described in OPCR[6:4].

## ACR – Auxiliary Control Register

**ACR[7] – Baud Rate Generator Set Select**
This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, 19.2k, and 38.4k baud.

The selected set of rates is available for use by the receiver and transmitter.

**ACR[6:4] – Counter/Timer Mode and Clock Source Select**
This field selects the operating mode of the counter/timer and its clock source (see Table 4).

The MPI pin available as the clock source is MPI a,c,e, and g only.

**Table 4. ACR[6:4] Operating Mode**

| [6:4] | Mode | Clock Source |
|---|---|---|
| 0 0 0 | Counter | MPI pin |
| 0 0 1 | Counter | MPI pin divided by 16 |
| 0 1 0 | Counter | TxC–1X clock of the transmitter |
| 0 1 1 | Counter | Crystal or external clock (X1/CLK) divided by 16 |
| 1 0 0 | Timer | MPI pin |
| 1 0 1 | Timer | MPI pin divided by 16 |
| 1 1 0 | Timer | Crystal or external clock (X1/CLK) |
| 1 1 1 | Timer | Crystal or external clock (X1/CLK) divided by 16 |

**ACR[3:0] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State Interrupt Enable**
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register, ISR[7], to be set. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

## IPCR – Input Port Change Register

**IPCR[7:4] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State**
These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

**IPCR[3:0] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State**
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the inputs pins at the time the IPCR is read.

## ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR.

**ISR[7] – MPI Change-of-State**
This bit is set when a change-of-state occurs at the MPI1b, MPI0b, MPI1a, MPI0a input pins. It is reset when the CPU reads the IPCR.

**ISR[6] – Channel b Change in Break**
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

**ISR[5] – Receiver Ready or FIFO Full Channel b**
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read.

If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

**ISR[4] – Transmitter Ready Channel b**
This bit is a duplicate of TxRDY (SR[2]).

**ISR[3] – Counter Ready**
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

**ISR[2] – Channel a Change in Break**
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

**ISR[1] – Receiver Ready or FIFO Full Channel a**
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be ready by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

**ISR[0] – Transmitter Ready Channel a**
This bit is a duplicate of TxRDY (SR[2]).

## IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR.

## CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these reegisters are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at adddress A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a subsequent sttart counter command causes the C/T to terminate the current timing cycle and to begin a new cycle using the values in the CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command read with A3–A0 = H'F'). The command, however, does not stop the C/T. The generated square wave is output on MPO if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching the terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains High until the terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter is read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_{CC}$ | Voltage from $V_{CC}$ to GND[3] | –0.5 to +7.0 | V |
| $V_S$ | Voltage from any pin to ground[3] | –0.5 to $V_{CC}$ +0.5 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High–level input voltage (except X1/CLK) | 2.0 | | | V |
| $V_{IH}$ | High–level input voltage (X1/CLK) | 4.0 | | | V |
| $V_{IL}$ | Low–level input voltage | | | 0.8 | V |
| $I_{OL}$ | Low–level output current | | | 2.4 | mA |
| $I_{OH1}$ | High–level output current | | | –400 | µA |
| $I_{OH2}$ | High–level output current | | | –100 | µA |
| $T_A$ | Operating free air temperature range[2] | –55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS[4] $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OL}$ | Output Low voltage | $V_{CC}$ = MIN, $I_{OL}$ = MAX | | | 0.4 | V |
| $V_{OH}$ | Output High voltage (except OD outputs) | $V_{CC}$ = MIN,<br>$I_{OH1}$ = MAX,<br>$I_{OH2}$ = MAX | $0.8V_{CC}$<br>$0.9V_{CC}$ | | | V<br>V |
| $I_{IL}$ | Input current Low, MPI and MPP pins | $V_{CC}$ = MAX, $V_{IN}$ = 0 | –65 | | | µA |
| $I_{IH}$ | Input current High, MPI and MPP pins | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | 20 | µA |
| $I_I$ | Input leakage current | $V_{CC}$ = MAX, $V_{IN}$ = 0 to $V_{CC}$ | –10 | | 10 | µA |
| $I_{ILX1}$ | X1/CLK input Low current | $V_{CC}$ = MAX, $V_{IN}$ = GND,<br>X2 = open | –100 | | | µA |
| $I_{IHX1}$ | X1/CLK input High current | $V_{IN}$ = $V_{CC}$, X23 = open<br>$V_{CC}$ = MAX | | | 100 | µA |
| $I_{OZH}$ | Output off current High, 3–state data bus | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | 10 | µA |
| $I_{OZL}$ | Output off current Low, 3–state data bus | $V_{CC}$ = MAX, $V_{IN}$ = 0 | –10 | | | µA |
| $I_{ODL}$ | Open–drain output Low current in off state: IRQN | $V_{CC}$ = MAX, $V_{IN}$ = 0 | –10 | | | µA |
| $I_{ODH}$ | Open–drain output High current in off state: IRQN | $V_{IN}$ = $V_{CC}$, $V_{CC}$ = MAX | | | 10 | µA |
| $I_{CC}$ | Power supply current<br>Operating mode | | | | 30 | mA |
| | Power down mode | | | | 2.4 | mA |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of $V_{IL}$ and $V_{IH}$, as appropriate.
5. Test condition for interrupt and MPP outputs: $C_L$ = 50pF, $R_L$ = 2.7kohms to $V_{CC}$. Test conditions for rest of outputs: $C_L$ = 150pF.
6. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
7. If CEN is used as the 'strobing' input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for $t_{RWD}$ guarantee that any status register changes are valid.
8. Consecutive write operations to the command register require at least three rising edges of the X1 clock between writes.
9. This value is not tested, but is guaranteed by design.

## AC ELECTRICAL CHARACTERISTICS[4, 5] $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | FIGURE | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Reset timing** | | | | | | |
| $t_{RES}$ | 3 | Reset pulse width | 200 | | | ns |
| **Bus timing[6]** | | | | | | |
| $t_{AS}$ | 4 | A0–A5 setup time to RDN, WRN Low | 10 | | | ns |
| $t_{AH}$ | 4 | A0–A5 hold time from RDN, WRN High | 100 | | | ns |
| $t_{CS}$[7] | 4 | CEN setup time to RDN, WRN Low | 0 | | | ns |
| $t_{CH}$[7] | 4 | CEN hold time from RDN, WRN High | 0 | | | ns |
| $t_{RW}$ | 4 | WRN, RDN pulse width Low | 225 | | | ns |
| $t_{DD}$ | 4 | Data valid after RDN Low | | | 200 | ns |
| $t_{DF}$ | 4 | Data bus floating after RDN High | | | 80 | ns |
| $t_{DS}$ | 4 | Data setup time before WRN High | 100 | | | ns |
| $t_{DH}$ | 4 | Data hold time after WRN High | 10 | | | ns |
| $t_{RWD}$[8] | 4 | Time between reads and/or writes | 100 | | | ns |
| **MPI and MPO timing[6]** | | | | | | |
| $t_{PS}$ | 5 | MPI or MPP input setup time before RDN Low | 0 | | | ns |
| $t_{PH}$ | 5 | MPI or MPP input hold time after RDN High | 0 | | | ns |
| $t_{PD}$ | 5 | MPO output valid from<br>WRN High<br>RDN Low | | | <br>250<br>250 | <br>ns<br>ns |
| **Interrupt timing** | | | | | | |
| $t_{IR}$ | 6 | INTRN negated or MPP output High from:<br>Read RHR (RxRDY/FFULL interrupt)<br>Write THR (TxRDY, TxEMT interrupt)<br>Reset command (break change interrupt)<br>Reset command (MPI change interrupt)<br>Stop C/T command (counter interrupt)<br>Write IMR (clear of interrupt mask bit) | | | <br>270<br>270<br>270<br>270<br>270<br>270 | <br>ns<br>ns<br>ns<br>ns<br>ns<br>ns |
| **Clock timing** | | | | | | |
| $t_{CLK}$ | 7 | X1/CLK high or low time | 120 | | | ns |
| $f_{CLK}$ | 7 | X1/CLK frequency | 2.0 | 3.6864 | 4.0 | mHz |
| $t_{CTC}$ | 7 | Counter/timer clock high or low time | 120 | | | nS |
| $f_{CTC}$ | 7 | Counter/timer clock frequency | 0[9] | | 4.0 | mHz |
| $t_{RX}$ | 7 | RxC high or low time | 200 | | | nS |
| $f_{RX}$ | 7 | RxC frequency (16X)<br>RxC frequency (1X) | 0[9]<br>0[9] | | 2.0<br>1.0 | mHz<br>mHz |
| $t_{TX}$ | 7 | TxC high or low time | 200 | | | nS |
| $f_{TX}$ | 7 | TxC frequency (16X)<br>TxC frequency (1X) | 0[9]<br>0[9] | | 2.0<br>1.0 | mHz<br>mHz |
| **Transmitter timing** | | | | | | |
| $t_{TXD}$ | 8 | TxD output delay from TxC low | | | 350 | ns |
| $t_{TCS}$ | 8 | TxC output delay from TxD output data | 0 | | 150 | ns |
| **Receiver timing** | | | | | | |
| $t_{RXS}$ | 9 | RxD data setup time to RxC high | 50 | | | ns |
| $t_{RXH}$ | 9 | RxD data hold time from RxC high | 100 | | | ns |

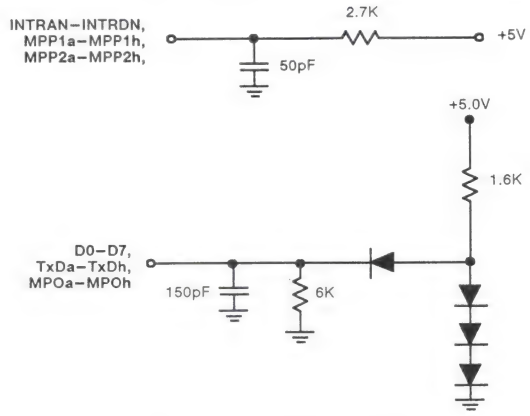



Figure 2. Test Conditions on Outputs

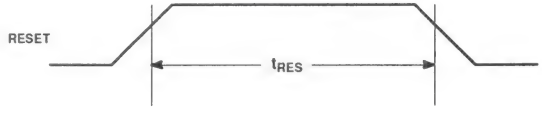



Figure 3. Reset Timing

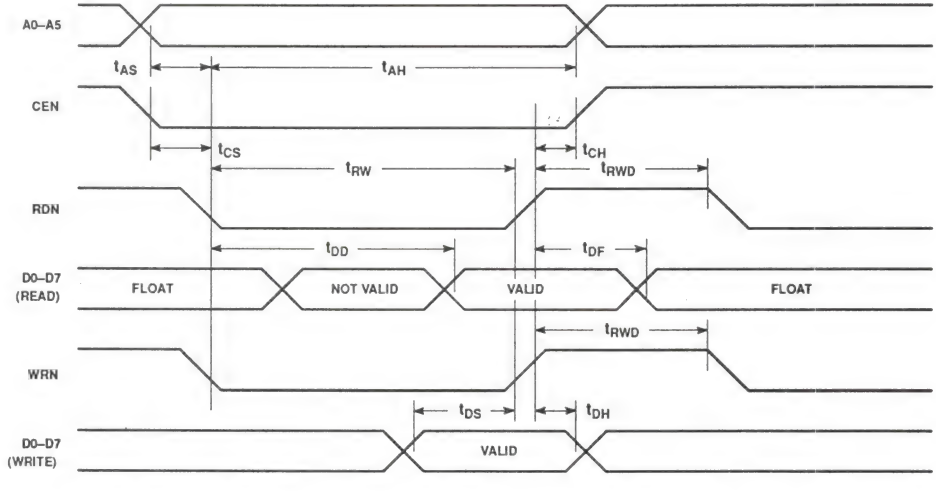



Figure 4. Bus Timing

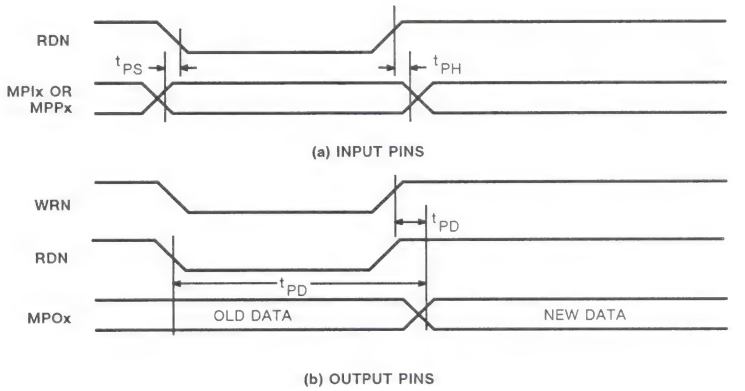
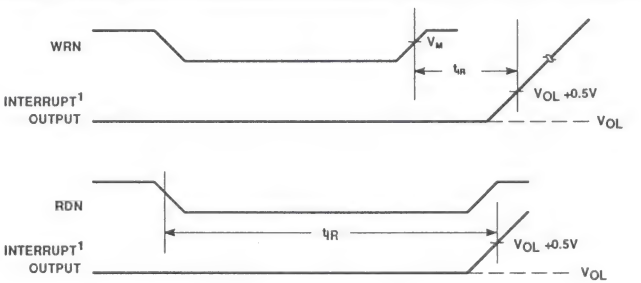
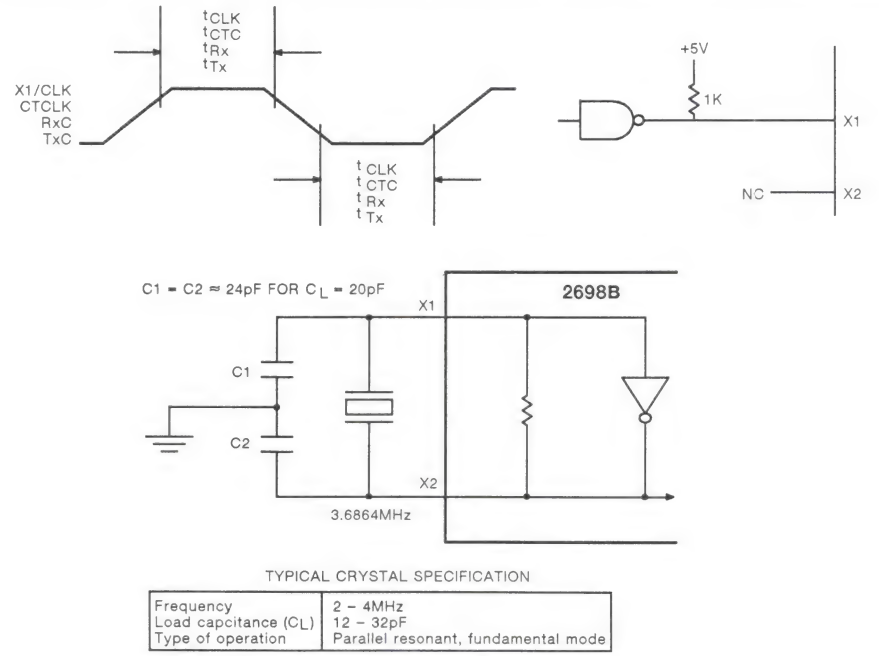



Figure 5. Port Timing




NOTES:
1. INTRN OR MPO WHEN USED AS INTERRUPT OUTPUTS.
2. THE TEST FOR OPEN DRAIN OUTPUTS IS INTENDED TO GUARANTEE SWITCHING OF THE OUTPUT TRANSISTOR. MEASUREMENT OF THIS RESPONSE IS REFERENCED FROM THE MIDPOINT OF THE SWITCHING SIGNAL, $V_M$, TO A POINT 0.5V ABOVE $V_{OL}$. THIS POINT REPRESENTS NOISE MARGIN THAT ASSURES TRUE SWITCHING HAS OCCURRED. BEYOND THIS LEVEL, THE EFFECTS OF EXTERNAL CIRCUITRY AND TEST ENVIRONMENT ARE PRONOUNCED AND CAN GREATLY AFFECT THE RESULTANT MEASUREMENT.

Figure 6. Interrupt Timing




TYPICAL CRYSTAL SPECIFICATION

| | |
|---|---|
| Frequency | 2 – 4MHz |
| Load capcitance (CL) | 12 – 32pF |
| Type of operation | Parallel resonant, fundamental mode |

**Figure 7. Clock Timing**

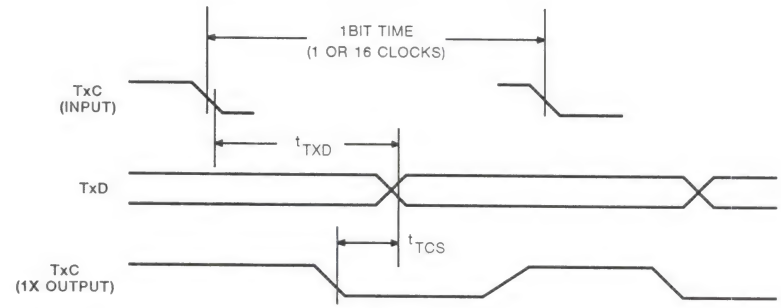



**Figure 8. Transmit Timing**

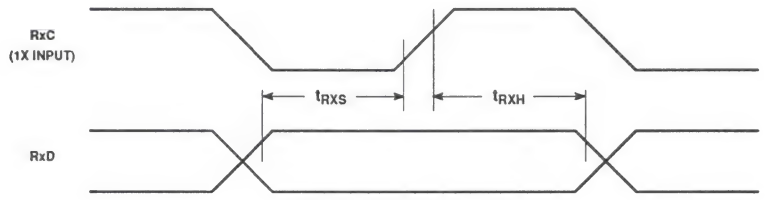
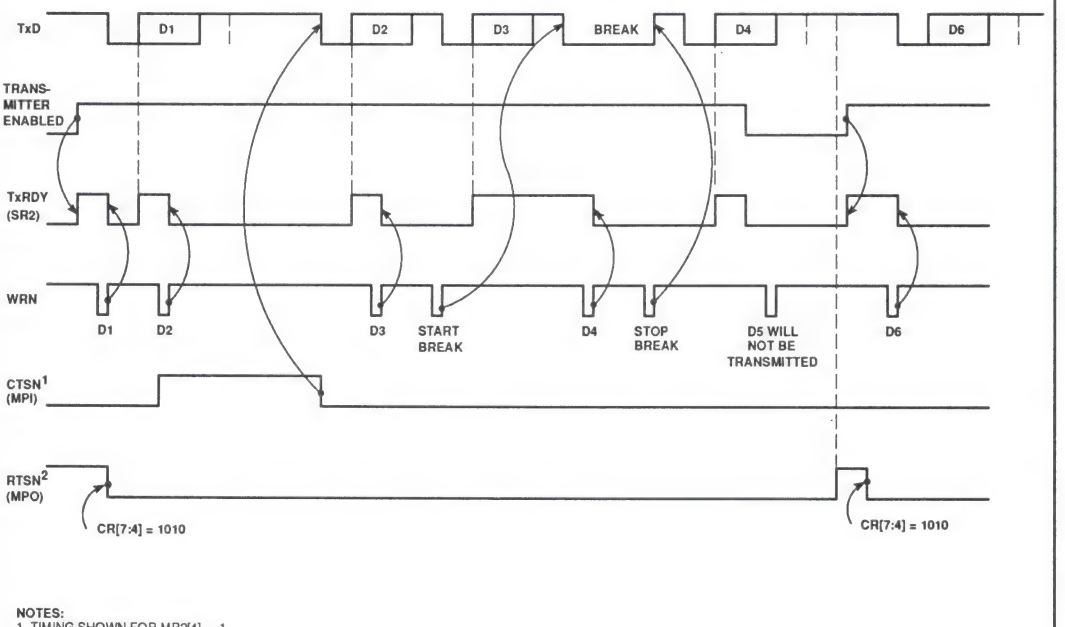



Figure 9. Receive Timing




NOTES:
1. TIMING SHOWN FOR MR2[4] = 1.
2. TIMING SHOWN FOR MR2[5] = 1.

Figure 10. Transmitter Timing

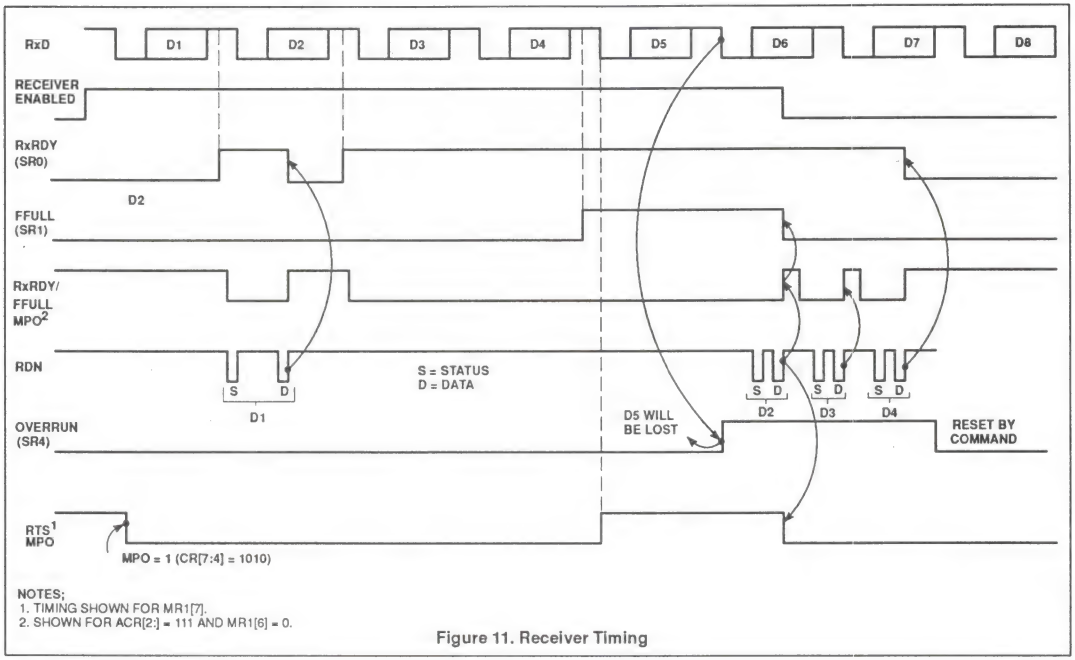



Figure 11. Receiver Timing

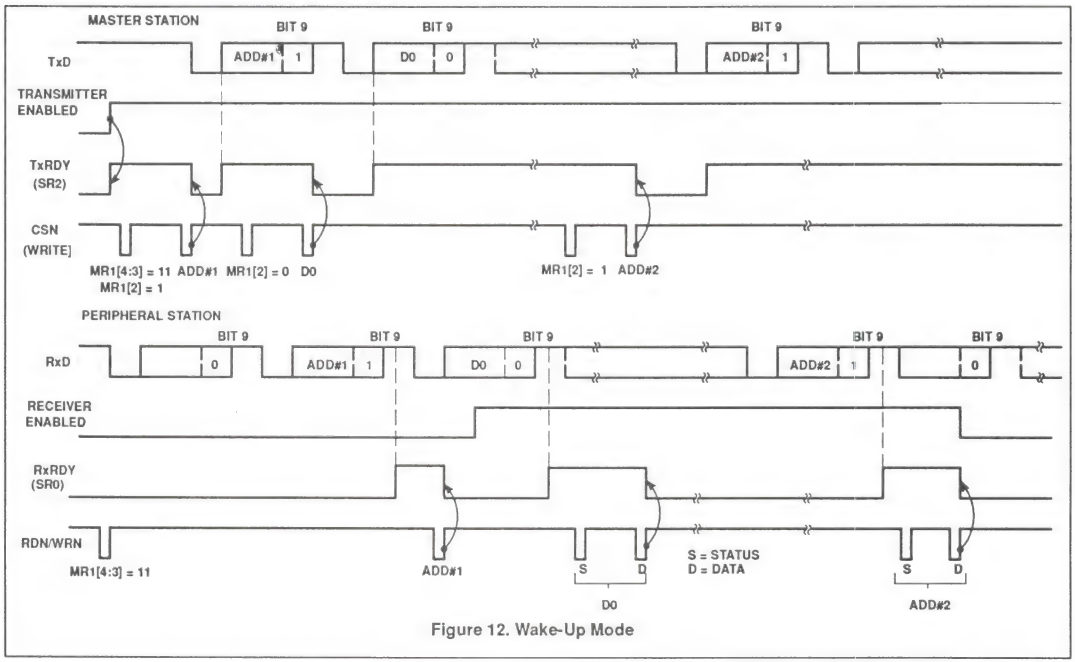



Figure 12. Wake-Up Mode

Signetics

# 68562
## Dual Universal Serial Communications Controller (DUSCC)

*Product Specification*

**Military Microprocessor Products**

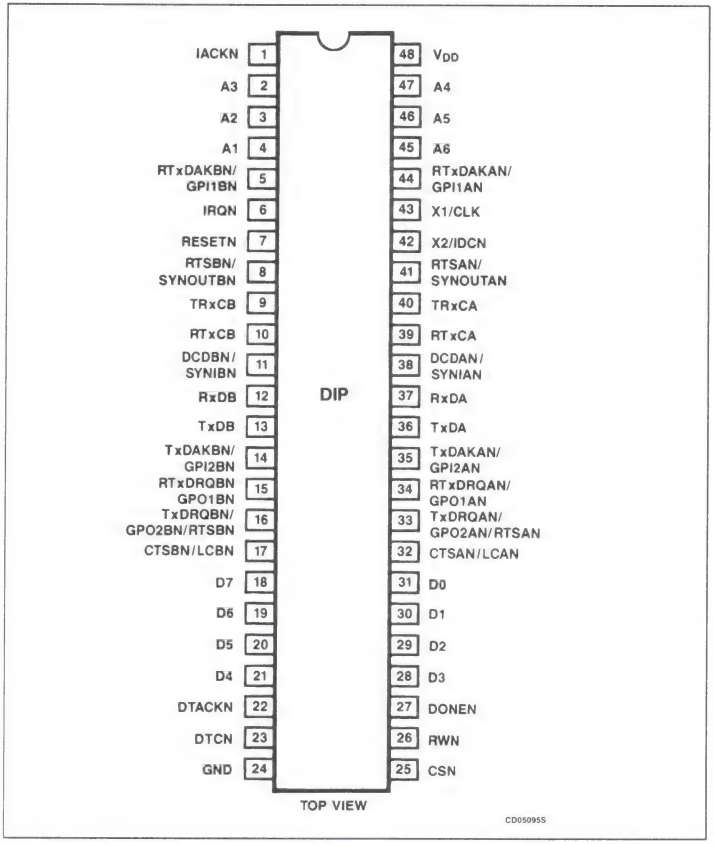
### DESCRIPTION

The Signetics Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multiprotocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented (byte count and byte control) synchronous protocols. The 68562 interfaces to the 68000 MPU via asynchronous bus control signals and is capable of program-polled, interrupt-driven, block-move or DMA data transfers.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a Digital Phase-Locked Loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common Bit Rate Generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

### PIN CONFIGURATION




Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

### ORDERING INFORMATION

| PACKAGES | ORDER CODE |
|---|---|
| 48-Pin Ceramic DIP | 68562/BXA |

# Dual Universal Serial Communications Controller (DUSCC) 68562

## FEATURES

### General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5 – 8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (Frame Check Sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM, FM1, Manchester
- Programmable channel mode: full-half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Half- or full-duplex operation
  - Single or dual address data transfers
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
  - 68000 compatible
- Multifunction programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD programmable autoenables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

### Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2 bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit up to 4Mbps and receive up to 2Mbps data rates

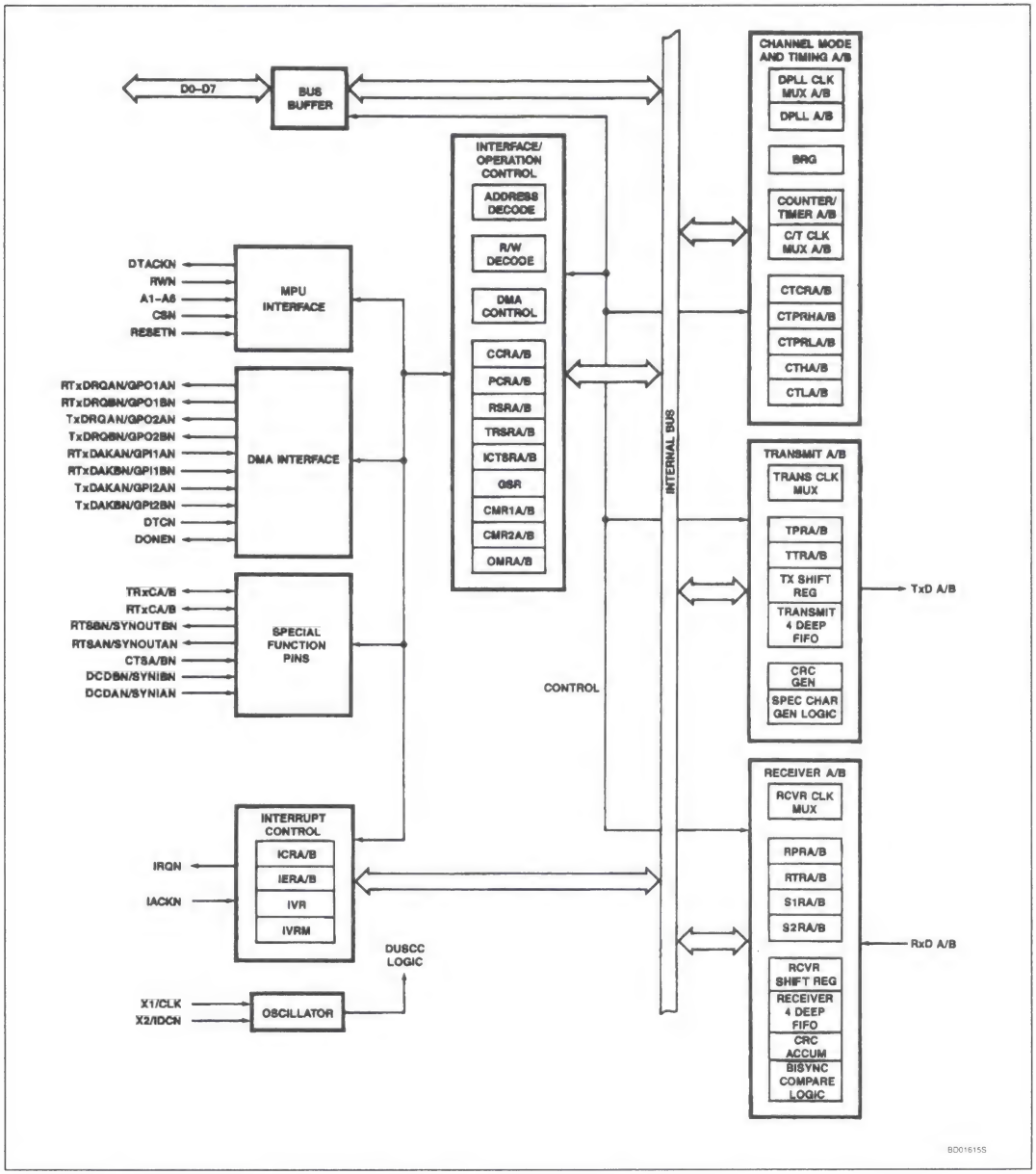
### Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection
- BISYNC Features
  - EBCDIC or ASCII header, test and control messages
  - SYN, DLE stripping
  - EOM (End Of Message) detection and transmission
  - Auto transparency mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text

### Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0 – 7 bits
- Automatic switch to programmed character length for 1 field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS-FLAGs line fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

## BLOCK DIAGRAM



## PIN DESCRIPTION

In this data sheet, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels: these are designated by either an underline or by A/B after the name.

| MNEMONIC | DIP PIN NO. | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| A1 – A6 | 4-2, 45-47 | I | **Address Lines:** Active-High. Address inputs which specify which of the internal registers is accessed for read/write operation. |
| D0 – D7 | 31-28, 21-18 | I/O | **Bidirectional Data Bus:** Active High, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN is Low, during interrupt acknowledge cycles and single-address DMA acknowledge cycles. |
| R/WN | 26 | I | **Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle when a cycle is initiated by assertion of the CSN input. |
| CSN | 25 | I | **Chip Select:** Active-Low input. When Low, data transfers between the CPU and the DUSCC are enabled on D0 – D7 as controlled by the R/WN and A1 – A6 inputs. When CSN is High, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single-address DMA transfers) and D0 – D7 are placed in the 3-State condition. |
| DTACKN | 22 | O | **Data Transfer Acknowledge:** Active-Low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. The signal is negated when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, data is latched with the falling edge of DTCN. DTACKN is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated. When negated, DTACKN becomes an open-drain output and requires an external pull-up resistor. |
| IRQN | 6 | O | **Interrupt Request:** Active-Low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus. |
| IACKN | 1 | I | **Interrupt Acknowledge:** Active-Low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted. |
| X1/CLK | 43 | I | **Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, and external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. |
| X2/IDCN | 42 | I/O | **Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide and interrupt daisy chain active-Low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2, is not used as an interrupt daisy chain output. |
| RESETN | 7 | I | **Master Reset:** Active-Low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1. Reset in asynchronous, i.e., no clock is required. |
| RxDA, RxDB | 37, 12 | I | **Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock. |
| TxDA, TxDB | 36, 13 | O | **Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock. |
| RTxCA, RTxCB | 39, 10 | I/O | **Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X). The maximum external receiver/transmitter clock frequency is 4MHz. |

## PIN DESCRIPTION (Continued)

| MNEMONIC | DIP PIN NO. | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| TRxCA, TRxCB | 40, 9 | I/O | **Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1/2). The maximum external receiver/transmitter clock frequency is 4MHz. |
| CTSA/BN, LCA/BN | 32, 17 | I/O | **Channel A (B) Clear-To-Send Input or Loop Control Output:** Active-Low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the COP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop. |
| DCDA/BN, SYNIA/BN | 38, 11 | I | **Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-Low input, it acts as an enable for the receiver or can be used as a general purpose input for the DCD function, the DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. As an active-Low external sync input, it is used in COP modes to obtain character synchronization without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21. |
| RTxDRQA/BN, GPO1A/BN | 34, 15 | O | **Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-Low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control. |
| TxDRQA/BN, GPO2A/BN, RTSA/BN | 33, 16 | O | **Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-Low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control (see Detailed Operation). |
| RTxDAKA/BN, GPI1A/BN | 44, 5 | I | **Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. For half-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode. |
| TxDAKA/BN, GP12A/BN | 35, 14 | I | **Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode. |
| DTCN | 23 | I | **Device Transfer Complete:** Active-Low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete. |
| DONEN | 27 | I/O | **Done:** Active-Low, open-drain. See Detailed Operation for a description of the function of this pin. |
| RTSA/BN, SYNOUTA/BN | 41, 8 | O | **Channel A (B) Sync Detect or Request-to-Send:** Active-Low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin. |
| $V_{DD}$ | 48 | I | +5V ± 10% power input. |
| GND | 24 | I | Signal and power ground input. |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $P_W$ | Max Power Dissipation | 1.8 | W |
| $T_{STG}$ | Storage Temperature range | -65 to +150 | °C |
| | All voltages with respect to ground[3] | -0.5 to 7.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNITS |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High level input voltage<br>All except X1 and CLK<br>X1 and CLK | <br>2.0<br>2.4 | | <br>V<br>V |
| $V_{IL}$ | Low level input voltage<br>All except X1 and CLK<br>X1 and CLK | | <br>0.8<br>0.4 | <br>V<br>V |
| $I_{IH}$ | Input current High | | -400 | µA |
| $T_A$ | Operating free-air temperature range | -55 | +110 | °C |

## DC CHARACTERISTICS $T_A$ = -55 to +110°C, $V_{CC}$ = 5.0V ± 10%

| SYMBOL | PARAMETER | TEST CONDITIONS[4, 5, 6] | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{CC}$ | Power supply current | $V_{CC}$ = 5.5V | | 325 | mA |
| $V_{OL}$ | Output Low voltage<br>All except DONEN & IRQN | $V_{CC}$ = 4.5V<br>$I_{OL}$ = 5.3mA | | 0.5 | V |
| $V_{OL}$ | Output Low voltage<br>DONEN & IRQN | $V_{CC}$ = 4.5V<br>$I_{OL}$ = 8.8mA | | 0.5 | V |
| $V_{OH}$ | Output High voltage<br>All except DONEN & IRQN | $V_{CC}$ = 4.5V<br>$I_{OH}$ = -400µA | 2.4 | | V |
| $I_{OD}$ | Open-drain output leakage current<br>(DONEN & IRQN) | $V_{CC}$ = 5.5V<br>$V_O$ = 0V to $V_{CC}$ | | 10 | µA |
| $I_{OZ}$ | 3-State output leakage current | $V_O$ = 0V to $V_{CC}$<br>$V_{CC}$ = 5.5V | -10 | 10 | µA |
| $I_{X1L}$ | X1/CLK Low input current | $V_{CC}$ = 5.5V[11]<br>$V_{IN}$ = 0V, X2 floated<br>$V_{IN}$ = 0V, X2 grounded | <br>-5.0<br>-2.0 | | <br>mA<br>mA |
| $I_{X1H}$ | X1/CLK High input current | $V_{CC}$ = 5.5V[11]<br>$V_{IN}$ = $V_{CC}$, X2 floated<br>$V_{IN}$ = $V_{CC}$, X2 grounded | | <br>36.0<br>1.0 | <br>mA<br>mA |
| $I_{X2L}$ | X2 Low input current | $V_{CC}$ = 5.5V[11]<br>$V_{IN}$ = 0V, X1/CLK floated | -100 | | µA |
| $I_{X2H}$ | X2 High input current | $V_{CC}$ = 5.5V[11]<br>$V_{IN}$ = $V_{CC}$, X1/CLK floated | | 100 | µA |
| $I_{IH}$ | Input leakage current | $V_{CC}$ = 5.5V<br>$V_{IN}$ = 5.5V | | 10 | µA |
| $I_{IL}$ | Input Low current<br>All except DTCN, RTxDAKA/B, TxDAKA/B | $V_{CC}$ = 5.5V<br>$V_{IN}$ = 0V | -100 | | µA |
| $I_{IL}$ | Input Low current remaining input pins | $V_{CC}$ = 5.5V<br>$V_{IN}$ = 0V | -10 | | µA |

## AC ELECTRICAL CHARACTERISTICS $T_A$ = -55 to +110°c, $V_{CC}$ = 5V ± 10%[4, 5, 6, 7]

| NO. | FIGURE | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| 1 | 12 | RESETN pulse width | 1.2 | | | µS |
| 2 | 13,15 | A1 - A6 set-up time to CSN Low | 10 | | | nS |
| 3 | 13.15 | A1 - A6 hold time from CSN High | 0 | | | nS |
| 4 | 13,15 | RWN set-up time to CSN Low | 0 | | | nS |
| 5 | 13,15 | RWN hold time to CSN High | 0 | | | nS |
| 6 | 13,15 | CSN High pulse width[7] | 160 | | | nS |
| 7 | 13,16 | CSN or IACKN High from DTACKN Low | 30 | | | nS |
| 7A | 16 | IACKN High to DTACKN High | | | 200 | nS |
| 8 | 13,16 | Data valid from CSN or IACKN Low | | | 300 | nS |
| 9 | 13 | Data bus floating from CSN High[10] | | | 100 | nS |
| 10 | 15 | Data hold time from DTACKN Low[8] | 0 | | | nS |
| 11 | 13,16 | DTACKN Low from read data ready | 0 | | | nS |
| 12 | 13,15 | DTACKN Low from CSN Low | | | 560 | nS |
| 12A | 15 | CSN Low to write data valid | | | 50 | nS |
| 13 | 13,15 | DTACKN High from CSN High | | | 150 | nS |
| 14 | 13,15 | DTACKN high impedance from CSN High | | | 185 | nS |
| 15 | 16 | DTACKN Low from IACKN Low | | | 550 | nS |
| 16 | 17 | GPI input set-up time to CSN Low | 20 | | | nS |
| 17 | 17 | GPI input hold time from CSN Low | 100 | | | nS |
| 18 | 17 | GPO output valid from DTACKN Low | | | 300 | nS |
| 19 | 18 | IRQN High from: | | | | |
| | | Read RxFIFO (RxRDY interrupt) | | | 450 | nS |
| | | Write TxFIFO (TxRDY interrupt)[12] | | | 450 | nS |
| | | Write RSR (Rx condition interrupt)[12] | | | 400 | nS |
| | | Write TRSR (Rx/Tx interrupt)[12] | | | 400 | nS |
| | | Write ICTSR (port change and CT int.)[12] | | | 400 | nS |
| 20 | 19 | X1/CLK High or Low time | 25 | | | nS |
| | | X1/CLK frequency | 2.0 | 14.745 | 16 | MHz |
| | | CTCLK High or Low time | 100 | 6 | | nS |
| | | CTCLK frequency | 0 | | 4 | MHz |
| | | RxC High or Low time | 110 | | | nS |
| | | RxC frequency (16X or 1X)[13] | 0 | | 4 | MHz |
| | | TxC High or Low time | 110 | | | nS |
| | | TxC frequency (16X or 1X) | 0 | | 4 | MHz |
| 21 | 20 | TxD output from TxC input Low (1X) | | | 240 | nS |
| | | (16X) | | | 435 | nS |
| 22 | 20 | TxD output from TxC output Low | | | 50 | nS |
| 23 | 21 | RxD data set-up time to RxC High | 50 | | | nS |
| 24 | 21 | RxD data hold time from RxC High | 50 | | | nS |
| 25 | 22 | IACKN Low to daisy chain Low | | | 200 | nS |
| 26 | 24 | Data valid from receive DMA ACKN | | | 300 | nS |
| 27 | 23,24 | DTCN width | 100 | | | nS |
| 28 | 23,24 | RDYN Low to DTCN Low | 80 | | | nS |
| 29 | 24 | Data bus float from DTCN Low[10] | | | 200 | nS |
| 30 | 23,24 | DMA ACKN Low to RDYN (DTACKN) Low | | | 360 | nS |
| 31 | 23,24 | RDYN High from DTCN Low | | | 230 | nS |
| 32 | 23,24 | RDYN High impedance from DTCN Low | | | 250 | nS |
| 33 | 24 | Receive DMA REQN High from DMA ACKN Low | | | 325 | nS |
| 34 | 24 | Receive DMA ACKN width | 150 | | | nS |
| 35 | 23,24 | Receive DMA ACKN Low to DONEN Low | | | 250 | nS |
| 36 | 23 | Data set-up to DTCN Low | 50 | | | nS |
| 37 | 23 | Data hold from DTCN Low[9] | 50 | | | nS |
| 38 | 23 | Transmit DMA REQN High from ACKN Low | | | 340 | nS |
| 39 | 23 | Transmit DMA ACKN width | 150 | | | nS |
| 40 | 23 | Transmit DMA ACKN Low to DONEN Low output | | | 250 | nS |
| 40A | 23 | DTCN Low DONEN output High | | | 260 | nS |
| 41 | 25 | CSN Low to transmit DONEN Low output | | | 300 | nS |
| 42 | 25 | CSN Low to transmit DMA REQ negated | | | 400 | nS |
| 43 | 25 | CSN Low to receive DONEN Low | | | 300 | nS |
| 44 | 25 | CSN Low to receive DMA REQ negated | | | 400 | nS |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 35°C/W junction to ambient.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For D.C. and functional testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 4.4V All time measurements are referenced at input voltages of 0.2V and 2.4V for all inputs. Output levels are referenced at 1.5V.
6. Test conditions for outputs: $C_L$ = 150pF, except open-drain outputs. Test condition for open-drain outputs: $C_L$ = 50pF to GND, $R_L$ = 2.7kΩ to $V_{CC}$ except DTACKN whose RL - 820Ω to $V_{CC}$ and $C_L$ = 150pF to GND and DONEN which requires $C_L$ = 50pF to GND and RL = 1kΩ to $V_{CC}$.
7. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus cycles are not performed.
8. Execution of the valid command (after it is latched) requires three falling edges of X1 (see Figure 14).
9. In single address DMA mode write operation, data is latched by the falling edge of DTCN.
10. These values were not explicitly tested, they are guaranteed by design and characterization data.
11. X1/CLK and X2 are not tested with a crystal installed.
12. These timings are from the falling edge of DTACKN (not CSN rising).
13. X1/CLK frequency must be at least four times the receiver serial data rate.

## REGISTERS

The addressable registers of the DUSCC are shown in Table 1. The following rules apply to all registers:

3. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle without a write being performed.
4. Unused bits of a defined register are read as zeros, unless ones have been loaded after master reset.
5. Bits that are unused in the chosen mode but are used in others are readable and writable but their contents are ignored in the chosen mode.
6. All registers are addressable as 8-bit quantities. To facilitate operation with the 68000 MOVEP instruction, addresses are ordered such that certain sets of registers may also be accessed as words or long words.

The operation of the DUSCC is programmmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The contents of certain control registers are initialized on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems, e.g., changing the channel mode at an inappropriate time may cause the reception or transmission of an incorrect character. In general, the contents of registers which control transmitter or receiver operation, or the counter/timer, should be changed only when they are not enabled.

The DUSCC registers can be separated into five groups to facilitate their usage:

1. Channel mode configuration and pin description registers.
2. Transmitter and receiver parameter and timing registers.
3. Counter/timer control and value registers.
4. Interrupt control and status registers.
5. Command register.

This arrangement is used in the following description of the DUSCC registers.

### Channel Mode Configuration and Pin Description Registers

There are five registers in this group for each channel. The bit format for each of these registers is contained in Table 2. The primary function of these registers is to define configuration of the channels and the function of the programmable pins. A channel cannot be dynamically reconfigured. Do not write to CMR1 or CMR2 if the receiver or transmitter is enabled.

### Channel Mode Register 1 (CMR1A, CMR1B)

**[7:6] Data Encoding —** These bits select the data encoding for the received and transmitted data:

00 If the DPLL is set to NRZI mode (see DPLL commands), it selects positive logic (1 = High, 0 = Low). If the DPLL is set to FM mode (see DPLL commands), Manchester (bi-phase level) encoding is selected.

01 NRZI. Non-return-to-zero inverted.

10 FM0. Bi-phase space.

11 FM1. Bi-phase mark.

**[5] Extended Control (BOP) —**

0 No. A one-octet control field follows the address field.

1 Yes. A two-octet control field follows the address field.

**[5] Parity (COP/ASYNC), Code Select (BISYNC) —**

0 Even parity if with parity is selected by [4:3] or a 0 in the parity bit position if force parity is selected by [4:3]. In BISYNC protocol mode, internal character comparisons are made using EBCDIC coding.

1 Odd parity if with parity is selected by [4:3] or a 1 in the parity bit position if force parity is selected by [4:3]. In BISYNC protocol mode, internal character comparisons are made using 7-bit plus odd parity ASCII coding. (Note: The receiver should be programmed for 7-bit characters, RPR[1:0] = 11, with no parity, CMR1[4:3] = 00.)

**[4:3] Address Mode (BOP) —** This field controls whether a single octet or multiple octets follow the opening FLAG(s) for both the receiver and the transmitter. This field is activated by selection of BOP secondary mode through the channel protocol mode bits CMR1[2:0] (see Detailed Operation).

00 Single-octet address.

01 Extended address.

10 Dual-octet address.

11 Dual-octet address with group.

**[4:3] Pairty Mode (COP/ASYNC) —** This field selects the parity mode for both the receiver and the transmitter. A parity bit is added to the programed character length if with parity or force parity is selected:

00 No pairty. Required when BISYNC protocol mode is programmed.

01 Reserved.

10 With parity. Odd or even parity is selected by [5].

11 Force parity. The parity bit is forced to the state selected by [5].

**[2:0] Channel Protocol Mode —** This field selects the operational protocol and submode for both the receiver and transmitter:

000 BOP Primary. No address comparison is performed. For receive, all characters received after the opening FLAG(s) are transferred to the FIFO.

001 BOP Secondary. This mode activates the address modes selected by [4:3]. Except in the case of extended address ([4:3] = 01), and address comparison is performed to determine if a frame should be received. Refer to Detailed Operation for details of the various addressing modes. If a valid comparison occurs, the receiver is activated and the address octets and all subsequent received characters of the frame are transferred to the receive FIFO.

010 BOP Loop. The DUSCC acts as a secondary station in a loop. The GO-ON-LOOP and GO-OFF-LOOP commands are used to cause the DUSCC to go on and off the loop. Normally, the TxD output echos the RxD input with a two-bit time delay. If the transmitter is enabled and the 'go active on poll' command has been asserted, the transmitter will begin sending when an EOP sequence consisting of a zero followed by seven ones is detected. The DUSCC changes the last one of the EOP to zero, making it another FLAG, and then operates as described in the Detailed Operation section. The loop sending status bit (TRSR[6]_ is asserted concurrent with the beginning of transmission. The frame should normally be terminated with an EOM followed by an echo of the marking RxD line so that secondary stations further down the loop can append their messages to the messages from up-loop stations by the same process. If the 'go active on poll' command is not asserted, the transmitter remains inactive (other than echoing the received data) even when the EOP sequence is received.

011 BOP Loop without address comparison. Same as normal loop mode except that address field comparisons are disabled. All received frames are transmitted to the CPU.

**Table 1. DUSCC Register Address Map**

| ADDRESS BITS* 6 5 4 3 2 1 | ACRONYM | REGSITER NAME | MODE | AFFECTED BY RESET |
|---|---|---|---|---|
| c 0 0 0 0 0 | CMR1 | Channel Mode Register 1 | R/W | Yes—00 |
| c 0 0 0 0 1 | CMR2 | Channel Mode Register 2 | R/W | Yes—00 |
| c 0 0 0 1 0 | S1R | SYN 1/Secondary Address 1 Register | R/W | No |
| c 0 0 0 1 1 | S2R | SYN 2/Secondary Address 2 Register | R/W | No |
| c 0 0 1 0 0 | TPR | Transmitter Parameter Register | R/W | Yes—00 |
| c 0 0 1 0 1 | TTR | Transmitter Timing Register | R/W | No |
| c 0 0 1 1 0 | RPR | Receiver Parameter Register | R/W | Yes—00 |
| c 0 0 1 1 1 | RTR | Receiver Timing Register | R/W | No |
| c 0 1 0 0 0 | CTPRH | Counter/Timer Preset Register High | R/W | No |
| c 0 1 0 0 1 | CTPRL | Counter/Timer Preset Register Low | R/W | No |
| c 0 1 0 1 0 | CTCR | Counter/Timer Control Register | R/W | Yes—00 |
| c 0 1 0 1 1 | OMR | Output and Miscellaneous Register | R/W | Yes—00 |
| c 0 1 1 0 0 | CTH | Counter/Timer High | R | No |
| c 0 1 1 0 1 | CTL | Counter/Timer Low | R | No |
| c 0 1 1 1 0 | PCR | Pin Configuration Register | R/W | Yes—00 |
| c 0 1 1 1 1 | CCR | Channel Command Register | R/W | No |
| c 1 0 0 X X | TxFIFO | Transmitter FIFO | W | No |
| c 1 0 1 X X | RxFIFO | Receiver FIFO | R | No |
| c 1 1 0 0 0 | RSR | Receiver Status Register | R/W** | Yes—00 |
| c 1 1 0 0 1 | TRSR | Transmitter and Receiver Status Register | R/W** | Yes—00 |
| c 1 1 0 1 0 | ICTSR | Input and Counter/TImer Status Register | R/W** | Yes |
| d 1 1 0 1 1 | GSR | General Status Register | R/W** | Yes—00 |
| c 1 1 1 0 0 | IER | Interrupt Enable Register | R/W | Yes—00 |
| c 1 1 1 0 1 | | Not used | | |
| 0 1 1 1 1 0 | IVR | Interrupt Vector Register— Unmodified | R/W | Yes—0F |
| 1 1 1 1 1 0 | IVRM | Interrupt Vector Register— Modified | R | Yes—0F |
| 0 1 1 1 1 1 | ICR | Interrupt Control Register | R/W | Yes—00 |
| 1 1 1 1 1 1 | | Not used | | |

NOTES:
* c = 0 for Channel A, c = 1 for Channel B.
d = don't care — register may be accessed as either channel.
x = don't care — FIFOs are addressable at any of four adjacent addresses to allow them to be addressed as byte/word/long word with the 68000 MOVEP instruction.
** A write to this register may perform a status resetting operation.

100 COP Dual SYN. Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R and S2R (SYN1-SYN2), including parity bits if any.

101 COP Dual SYN (BISYNC). Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R and S2R (SYN1-SYN2). In this mode, special transmitter and receive logic is activated. Transmitter and receiver character length must be programmed to 8 bits and no parity (see Detailed Operation).

110 COP Single SYN. Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R (SYN1), including parity bit if any. This mode is required when the external sync mode is selected (see description of RPR[4], BOP/COP).

111 Asynchronous. Start/stop format.

## Channel Mode Register 2 (CMR2A, CMR2B)

**[7:6] Channel Connection —** This field selects the mode of operation of the channel. The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character.

00 Normal mode. The transmitter and receiver operate independently in either half- or full-duplex, controlled by the respective enable commands.

01 Automatic echo mode. Automatically retransmits the received data with a half-bit time delay (ASYNC, 16X clock mode) or a two-bit time delay (all other modes). The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receiver clock is used for the transmitter for ASYNC 16X clock mode. For other modes the transmitter clock must be supplied.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and underrun status bits are inactive.
5. The received parity and/or FCS are checked if required, but are not regenerated for transmission, i.e., transmitted parity and/or FCS are as received.
6. In ASYNC mode, character framing is checked, but the stop bits are retransmitted as received. A received break is echoed as received.
7. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

10 Local loopback mode. In this mode:

1. The transmitter data output and clock are internally connected to the receiver.

2. The transmit clock is used for the receiver if NRZI or NRZ encoding is used. For FM or Manchester encoding because the receiver clock is derived from the DPLL, the DPLL source clock must be maintained.
3. The TxD output is held High.
4. The RxD input is ignored.
5. The receiver and transmitter must be enabled.
6. CPU to transmitter and receiver communications continue normally.

11 Reserved.

**[5:3] Data Transfer Interface —** This field specifies the type of data transfer between the DUSCC's Rx and TxFIFOs and the CPU. All interrupt and status functions operate normally regardless of the data transfer interface programmed. Refer to Detailed Operation for details of the various DMA transfer interfaces.

000 Half-duplex single address DMA.

001 Half-duplex dual address DMA.

010 Full-duplex single address DMA.

011 Full-duplex dual address DMA.

100 Wait on receive only. In this mode a read of a non-empty receive FIFO results in a normal bus cycle. However, if the receive FIFO of the channel is empty when a read Rx FIFO cycle is initiated, the DTACKN output remains negated until a character is received and loaded into the FIFO. DTACKN is then asserted and the cycle is completed normally.

101 Wait on transmit only. In this mode a write to a non-full transmit FIFO results in a normal bus cycle. However, if the transmit FIFO of the channel is full when a write TxFIFO cycle is initiated, the DTACKN output remains negated until a FIFO position becomes available for the new character. DTACKN is then asserted and the cycle is completed normally.

110 Wait on transmit and receive. As above for both wait on receive and transmit operations.

111 Polled or interrupt. DMA and wait function of the channel are not activated. Data transfers to the Rx and TxFIFOs are via normal bus read and write cycles in response to polling of the status registers and/or interrupts.

**[2:0] Frame Check Sequence Select —** This field selects the optional frame check sequence (FCS) to be appended at the end of a transmitted frame. When CRC is selected in COP, then no pairty and 8-bit character length must be used. The selected FCS is transmitted as follows:

1. Following transmission of a FIFOed character tagged with the 'send EOM' command.
2. If underrun control (TPR[7:6]) is programmed for TEOM, upon occurrence of an underrun.
3. If TEOM on zero count or done (TPR[4]) is asserted and the counter/timer is counting transmitted characters, after transmission of the character which causes the counter to reach zero count.
4. In DMA mode with TEOM on zero count or done (TPR[4]) set, after transmission of a character if DONEN is asserted when that character was loaded into the TxFIFO by the DMA controller.

000 No frame check sequence.

001 Reserved

010 LRC8: Divsior = $x^8 + 1$, dividend preset to zeros. The Tx sends the calculated LRC non-inverted. The Rx indicates and error if the computed LRC is not equal to 0. Valid for COP modes only.

011 LRC8: Divisor = $x^8 + 1$, dividend preset to ones. The Tx sends the calculated LRC non-inverted. The Rx indicates an error if the computed LRC is not equal to 0. Valid for COP modes only.

100 CRC16: Divisor - $x^{16} + x^{15} + x^2 + 1$, dividend preset to zeros. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the comuted CRC is not equal to 0. Not valid for ASYNC mode.

101 CRC16: Divisor = $x^{16} + x^{15} + x^2 + 1$, dividend preset to ones. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the computed CRC is not equal to 0. Not valid for ASYNC mode.

110 CRC-CCITT: Divisor = $x^{16} + x^{12} + x^5 + 1$, dividend preset to zeros. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the computed CRC is not equal to 0. Not valid for ASYNC mode.

111 CRC-CCITT: Divisor = $x^{16} + x^{12} + x^5 + 1$, dividend preset to ones. The Tx sends the calculated CRC inverted. The Rx indicates an error if the computed CRC is not equal to H'F0B8'. Not valid for ASYNC mode.

## SYN1/Secondary Address 1 Register (S1RA, S1RB)

**[7:0} Character Compare —** In ASYNC mode this register holds a 5- to 8-bit long bit pattern which is ocmpared with received characters. if a match occurs, the character compare status bit (RSR[7]) is set. This field is ignored if the receiver is in a break condition.

In COP modes, this register contains the 5- to 8-bit SYN1 bit pattern, right justified. Parity bit need not be included in the value placed in the register even is parity is specified in CMR1[4:3]. However, a character received with parity error, when parity is specified, will not match. In ASYNC, or COP modes, if parity is specified, then any unused bits in this register must be programmed to zeros. In BOP secondary mode it contains the address used to compare the first received address octet. The register is not used in BOP primary mode or secondary modes where address comparisons are not made, such as when extended addressing is specified.

## SYN2/Secondary Address 2 Register (S2RA, S2RB)

**[7:0]** — This register is not used in ASYNC, COP single SYN, BOP primary modes, BOP secondary modes with single address field, and BOP secondary modes where address comparisons are not made, such as when extended addressing is specified.

In COP dual SYN modes, it contains the 5- to 8-bit SYN2 bit pattern, right justified, Parity bit need not be included in the value placed in the register even if parity is specified in CMR1[4:3]. However, a character received with parity error, when parity is specified, will not match. If parity is specified, then any unused bits in this register must be programmed to zeros. In BOP secondary mode using two address octets, it contains the partial address used to compare the second received address octet.

## Pin Configuration Register (PCRA, PCRB)

This register selects the functions for multipurpose I/O pins.

**[7] X2/IDC —** This bit is defined only for PCRA. It is not used in PCRB.

0 The X2/IDCN pin is used as a crystal connection.

1 The X2/IDCN pin is the interrupt daisy chain output.

**[6] GPO2/RTS —** The function of this pin is programmable only when not operating in full-duplex DMA mode.

## Table 2. Channel Configuration/Pin Definition Registers Bit Formats

CHANNEL MODE REGISTER 1

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | Data Encoding | | Extended Control | Address Mode (BOP) | | Channel Protocol Mode | | |
| (CMR1A, CMR1B) | 00 — NRZ/Manchester<br>01 — NRZI<br>10 — FM0<br>11 — FM1 | | BOP only<br>0 — no<br>1 — yes | 00 — 8-bit<br>01 — extended address<br>10 — 16-bit<br>11 — 16-bit w/group | | 000 — BOP primary<br>001 — BOP secondary<br>010 — BOP loop<br>011 — BOP loop – no adr. comp. | | |
| | | | Parity* | Parity Mode (COP/ASYNC) | | | | |
| | | | 0 — even<br>1 — odd | 00 — no parity<br>01 — reserved<br>10 — with parity<br>11 — force parity | | 100 — COP dual SYN<br>101 — COP dual SYN (BISYNC)<br>110 — COP single SYN<br>111 — asynchronous | | |

NOTE:
* In BISYNC protocol mode, 0 = EBCDIC, 1 = ASCII coding.

CHANNEL MODE REGISTER

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | Channel Connection | | Data Transfer Interface | | | Frame Check Sequence Select | | |
| (CMR2A, CMR2B) | 00 — normal<br>01 — auto echo<br>10 — local loop<br>11 — reserved | | 000 — half-duplex single address DMA<br>001 — half-duplex dual address DMA<br>010 — full-duplex single address DMA<br>011 — full-duplex dual address DMA<br>100 — wait on Rx only<br>101 — wait on Tx only<br>110 — wait on Rx or Tx<br>111 — polled or interrupt | | | 000 — none<br>001 — reserved<br>010 — LRC8 preset 0s<br>011 — LRC8 preset 1s<br>100 — CRC 16 preset 0s<br>101 — CRC 16 preset 1s<br>110 — CRC CCITT preset 0s<br>111 — CRC CCITT preset 1s | | |

SYN1/SECONDARY ADDRESS REGISTER 1

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (S1RA, S1RB) | ASYNC — Character compare (5 – 8 bits)<br>COP — SYN1 (5 – 8 bits)<br>BOP — First address octet | | | | | | | |

SYN2/SECONDARY ADDRESS REGISTER 2

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (S2RA, S2RB) | ASYNC — not used<br>COP — SYN2 (5 – 8 bits)<br>BOP — Second address octet | | | | | | | |

PIN CONFIGURATION REGISTER

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | X2/IDS | GPO2/RTS | SYNOUT/RTS | RTxC Pin | | TRxC Pin | | |
| (PCRA, PCRB) | *<br>0 — X2<br>1 — IDC | 0 — GPO2<br>1 — RTS | 0 — SYNOUT<br>1 — RTS | 00 — input<br>01 — C/T<br>10 — TxCLK 1X<br>11 — RxCLK 1X | | 000 — input<br>001 — XTAL/2<br>010 — DPLL<br>011 — C/T | 100 — TxCLK 16X<br>101 — RxCLK 16X<br>110 — TxCLK 1X<br>111 — RxCLK 1X | |

NOTE:
* PCRA only. Not used in PCRB.

0 The TxDRQN/GPO2N/RTSN pin is a general purpose output. It is Low when OMR[2] is a 1 and High when OMR[2] is a 0.

1 The pin is a request-to-send output (see Detailed Operation). The logical state of the pin is controlled by OMR[0]. When OMR[0] is set, the output is Low.

**[5] SYNOUT/RTS —**

0 The SYNOUTN/RTSN pin is an active-Low output which is asserted one bit time after a SYN pattern (COP modes) in HSRH/HSRL or FLAG (BOP modes) is detected in CCSR. The output remains asserted for one receiver clock period. See Figure 1 for receiver data path.

1 The pin is a request-to-send output (see Detailed Operation). The logical state of the pin is controlled by OMR[0] when OMR[0] is set, the output is Low.

**[4:3] RTxC —**

00 The pin is an input. It must be programmed for input when used as the input for the receiver or transmitter clock, the DPLL, or the C/T.

01 The pin is an output for the counter/timer. Refer to CTCRA/B description.

10 The pin is an output for the transmitter shift register clock.

11 The pin is an output for the receiver shift register clock.

**[2:0] TRxC —**

000 The pin is an input. It must be programmed for input when used as the input for the receiver or transmitter clock, the DPLL, or the C/T.

001 The pin is an output from the crystal oscillator divided by two.

010 The pin is an output for the DPLL output clock.

011 The pin is an output for the counter/timer. Refer to CTCRA/B description.

100 The pin is an output for the transmitter BRG at 16X the rate selected by TTR [3:0].

101 The pin is an output for the receiver BRG at 16X the rate selected by RTR [3:0].

110 The pin is an output for the transmitter shift register clock.

111 The pin is an output for the receiver shift register clock.

## Transmitter and Receiver Parameter and Timing Registers

This set of five registers contains the information which controls the operation of the transmitter and receiver for each channel. Table 3 shows the bit map format for each of these registers. The registers of this group are:

1. Transmitter parameter and timing registers (TPRA/B and TTRA/B)
2. Receiver parameter and timing registers (RPRA/B and RTRA/B)
3. Output and miscellaneous register (OMRA/B).

The first and second group of registers define the transmitter and receiver parameters and timing. Included in the receiver timing registers are the programming parameters for the DPLL. The last register of the group, OMR contains additional transmitter and receiver information and controls the logical state of the output pins when they are not used as a part of the channel configuration.

A channel cannot be dynamically reconfigured. Do not write to the RPR if the receiver is enabled, and do not write to the TPR if the transmitter is enabled.

**Table 3. Transmitter and Receiver Parameter and Timing Register Bit Format**

**TRANSMITTER PARAMETER REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| **(TPRA, TPRB)** | **Underrun Control** | | **Idle** | **TEOM on Zero Cnt or Done** | **Tx RTS Control** | **CTS Enable Tx** | **Tx Character Length** | |
| COP | 00 — FCS-idle<br>01 — reserved<br>10 — MARKs<br>11 — SYNs | | 0 — MARKs<br>1 — SYNs | 0 — no<br>1 — yes | 0 — no<br>1 — yes | 0 — no<br>1 — yes | 00 — 5 bits<br>01 — 6 bits<br>10 — 7 bits<br>11 — 8 bits | |
| | **Underrun Control** | | **Idle** | **TEOM on Zero Cnt or Done** | | | | |
| BOP | 00 — FCS-FLAG-idle<br>01 — reserved<br>10 — ABORT-MARKs<br>11 — ABORT-FLAGs | | 0 — MARKs<br>1 — FLAGs | 0 — no<br>1 — yes | | | | |
| | **Stop Bits Per Character** | | | | | | | |
| ASYNC | 9/16 to 1, 17/16 to 1.5, 25/16 to 2 programmable in 1/16-bit increments | | | | | | | |

**TRANSMITTER TIMING REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (TTRA, TTRB) | External Source | Transmitter Clock Select | | | Bit Rate Select | | | |
| | 0 — RTxC<br>1 — TRxC | 000 — 1X external<br>001 — 16X external<br>010 — DPLL<br>011 — BRG<br>100 — 2X other channel C/T<br>101 — 32X other channel C/T<br>110 — 2X own channel C/T<br>111 — 32X own channel C/T | | | one of sixteen rates from BRG | | | |

**RECEIVER PARAMETER REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (RPRA, RPRB) | not used | not used | not used | Rx RTS Control | Strip Parity | DCD Enable Rx | Rx Character Length | |
| ASYNC | | | | 0 — no<br>1 — yes | 0 — no<br>1 — yes | 0 — no<br>1 — yes | 00 — 5 bits<br>01 — 6 bits | |
| COP | SYN Strip | FCS to FIFO | Auto Hunt & Pad Chk | Ext Sync | Strip Parity | | 10 — 7 bits<br>11 — 8 bits | |
| | 0 — no<br>1 — yes | 0 — no<br>1 — yes | 0 — no<br>1 — yes | 0 — no<br>1 — yes | 0 — no<br>1 — yes | | | |
| | not used | FCS to FIFO | Overrun Mode | not used | All Parity Address | | | |
| BOP | | 0 — no<br>1 — yes | 0 — hunt<br>1 — cont | | 0 — no<br>1 — yes | | | |

**RECEIVER TIMING REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (RTRA, RTRB) | External Source | Receiver Clock Select | | | Bit Rate Select | | | |
| | 0 — RTxC<br>1 — TRxC | 000 — 1X external<br>001 — 16X external<br>010 — BRG<br>011 — C/T of channel<br>100 — DPLL, source = 64X X1/CLK<br>101 — DPLL, source = 32X External<br>110 — DPLL, source = 32X BRG<br>111 — DPLL, source = 32X C/T | | ASYNC protocol mode only | one of sixteen rates from BRG | | | |

**OUTPUT AND MISC REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (OMRA, OMRB) | Tx Residual Character Length | | | TxRDY Activate | RxRDY Activate | OUT 2 | OUT 1 | RTS |
| | 000 — 1 bit<br>001 — 2 bits<br>010 — 3 bits<br>011 — 4 bits<br>100 — 5 bits<br>101 — 6 bits<br>110 — 7 bits<br>111 — same as TPR[1:0] | | | 0 — FIFO not full<br>1 — FIFO empty | 0 — FIFO not empty<br>1 — FIFO full | Bit Pin<br>0 — H<br>1 — L | Bit Pin<br>0 — H<br>1 — L | Bit Pin<br>0 — H<br>1 — L |

## Transmitter Parameter Register (TPRA, TPRB)

**[7:6] Underrun Control —** In BOP and COP modes, this field selects the transmitter response in the event of an underrun (i.e., the TxFIFO is empty).

00 Normal end of message termination. In BOP, the transmitter sends the FCS (if selected by CMR2[2:0]) followed by a FLAG and then either MARKs or FLAGs, as specified by [5]. In COP, the transmitter sends the FCS (if selected by CMR2[2:0]) and then either MARKs or SYNs, as specified by [5].

01 Reserved.

10 In BOP, the transmitter sends an ABORT (11111111) and then places the TxD output in a marking condition until receipt of further instructions. In COP, the transmitter places the TxD output in a marking condition until receipt of further instructions.

11 In BOP, the transmitter sends an ABORT (11111111) and then sends FLAGs until receipt of further instruction. In COP, the transmitter sends SYNs until receipt of further instructions.

**[5] Idle —** In BOP and COP modes, this bit selects the transmitter output during idle. Idle is defined as the state following a normal end of message until receipt of the next transmitter command.

0 Idle in marking condition.

1 Idle sending SYNs (COP) or FLAGs (BOP).

**[4] Transmit EOM on Zero Count or Done —** In BOP and COP modes, the assertion of this bit causes the end of message (FCS in COP, FCS-FLAG in BOP) to be transmitted upon the following events:

1. If the counter/timer is counting transmitted characters, after transmission of the character which causes the counter to reach zero count. (DONEN is also asserted as an output if the channel is in a DMA operation.)
2. If the channel is operating in DMA mode, after transmission of a character if DONEN was asserted when that character was loaded into the TxFIFO by the DMA controller.

**[7:4] Stop Bits per character —** In ASYNC mode, this field programs the length of the stop bit appended to the transmitted character as shown in Table 4.

**Table 4 Stop Bits — Transmitted Character**

| [7:4] | 5 BITS/ CHAR | 6, 7 or 8 BITS/CHAR |
|---|---|---|
| 0000 | 1.063 | 0.563 |
| 0001 | 1.125 | 0.625 |
| 0010 | 1.188 | 0.688 |
| 0011 | 1.250 | 0.750 |
| 0100 | 1.313 | 0.813 |
| 0101 | 1.375 | 0.875 |
| 0110 | 1.438 | 0.938 |
| 0111 | 1.500 | 1.000 |
| 1000 | 1.563 | 1.563 |
| 1001 | 1.625 | 1.625 |
| 1010 | 1.688 | 1.688 |
| 1011 | 1.750 | 1.750 |
| 1100 | 1.813 | 1.813 |
| 1101 | 1.875 | 1.875 |
| 1110 | 1.938 | 1.938 |
| 1111 | 2.000 | 2.000 |

Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16-bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16-bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled) in all cases.

If an external 1X clock (or a 2X clock for counter/timer) is used for the transmitter, [7] = 0 selects one stop bit and [7] = 1 selects two stop bits to be transmitted. If Manchester, NRZI, or FM data encoding is selected, only integral stop bit lengths should be used.

**[3] Transmitter Request-to-Send Control —** This bit controls the deactivation of the RTSN output by the transmitter (see Detailed Operation).

0 RTSN is not affected by status of transmitter.

1 RTSN changes state as a function of transmitter status.

**[2] Clear-to-Send Enable Transmitter —** The state of this bit determines if the CTSN input controls the operation of the channel's transmitter (see Detailed Operation). The duration of CTS level change is described in the discussion of ICTSR[4].

0 CTSN has no affect on the transmitter.

1 CTSN affects the state of the transmitter.

**[1:0] Transmitted Bits per Character —** This field selects the number of data bits per character to be transmitted. The character length does not includes the start, parity, and stop bits in ASYNC or the parity bit in COP. In BOP modes the character length for the address and control field is always 8 bits, and the value of this field only applies to the information (I) field, except for the last character of the I field, whose length is specified by OMR[7:5].

## Transmitter Timing Register (TTRA, TTRB)

**[7] External Source —** This bit selects the RTxC pin or the TRxC pin of the channel as the transmitter clock input when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0 External input form RTxC pin.

1 External input from TRxC pin.

**[6:4] Transmitter Clock Select —** This field selects the clock for the transmitter.

000 External clock from TRxC or RTXC at 1X the shift (baud) rate.

001 External clock from TRXC or RTxC at 16X the shift rate.

010 Internal clock from the phase-locked loop at 1X the bit rate. It should be used only in half-duplex operation since the DPLL will periodically resync itself to the received data if in full-duplex operation.

011 Internal clock from the bit rate generator at 32X the shift rate. The clock signal is divided by two before use in the transmitter which operates at 16X the baud rate. Rate selected by [3:0].

100 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 2X the shift rate.

101 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 32X the shift rate.

110 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 2X the shift rate.

111 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate.

**[3:0] Bit Rate Select —** This field selects an output from the bit rate generator to be used by the transmitter circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 5. With a crystal or external clock of 14.7456MHz the bit rates are as given in Table 5 (this input is divided by two before being applied to the oscillator circuit).

**Table 5. Receiver/Transmitter Baud Rates**

| [3:0] | BIT RATE | [3:0] | BIT RATE |
|---|---|---|---|
| 0000 | 50 | 1000 | 1050 |
| 0001 | 75 | 1001 | 1200 |
| 0010 | 110 | 1010 | 2000 |
| 0011 | 134.5 | 1011 | 2400 |
| 0100 | 150 | 1100 | 4800 |
| 0101 | 200 | 1101 | 9600 |
| 0110 | 300 | 1110 | 19.2K |
| 0111 | 600 | 1111 | 38.4K |

## Receiver Parameter Resgister (RPRA, RPRB)

**[7] SYN Stripping** — This bit controls the DUSCC processing in COP modes of SYN 'character patterns' that occur after the initial character synchronization. Refer to Detailed Operation of the receiver for details and definition of SYN 'patterns', and their accumulation of FCS.

0 Strip only leading SYN 'patterns' (i.e. before a message).

1 Strip all SYN 'patterns' (including all odd DLE's in BISYNC transparent mode).

**[6] Transfer Received FCS to FIFO** — In BISYNC and BOP modes, the assertion of this bit causes the received FCS to be loaded into the RxFIFO. When this bit is set, BOP mode operates correctly only if a minimum of two extra FLAGs (without shared zeros) are appended to the frame. If the FCS is specified to be transferred to the FIFO, the EOM status bit will be tagged onto the last byte of the FCS instead of to the last character of the message.

0 Do not transfer FCS to RxFIFO.

1 Transfer FCS to RxFIFO.

**[5] Auto-Hunt and Pad Check (BISYNC)** — In BISYNC mode, the assertion of this bit causes the receiver to go into hunt for character sync mode after detecting certain End-Of-Message (EOM) characters. These are defined in the Detailed Operations section for COP receiver operation. After the EOT and NAK sequences, the receiver also does a check for a closing PAD of four 1s.

0 Disable auto-hunt and PAD check.

1 Enable auto-hunt and PAD check.

**[5] Overrun Mode (BOP)** — The state of this control bit determines the operation of the receiver in the event of a data overrun, i.e., when a character is received while the RxFIFO and the Rx shift register are both full.

0 The receiver terminates receiving the current frame and goes into hunt phase, looking for a FLAG to be received.

1 The receiver continues receiving the current frame. The overrunning character is lost. (The five characters already assembled in the RxFIFO and Rx shift register are protected).

**[4] Receiver Request-to-Send Control (ASYNC)** — See Detailed Operation.

0 Receiver does not control RTSN output.

1 Receiver can negate RTSN output.

**[4] External Sync (COP)** — In COP single SYN mode, the assertion of this bit enables external character synchronization and receipt of SYN patterns is not required. In order to use this feature, the DUSCC must be programmed to COP single SYN mode, CMR 1[2:0] = 110, which is used to set up the internal data paths. In all other respects, however, the external sync mode operation is protocol transparent. A negative signal on the DCDN/SYNIN pin will cause the receiver to establish synchronization on the next rising edge of the receiver clock. Character assembly will start at this edge with the RxD input pin considered to have the second bit of data. The sync signal can then be negated. Receipt of the Active-High external sync input causes the SYN detect status bit (RSR[2]) to be set and the SYNBOUTN pin to be asserted for one bit time. When this mode is enable, the internal SYN (COP mode) detection and special character recognition (e.g., IDLE, STX, ETX, etc.) circuits are disabled. Character assembly begins as if in the I-field with character length as programmed in RPR[1:)]. Incoming COP frames with parity specified optionally can have it stripped by programming RPR[3]. The user must wait at least eight bit times after Rx is enabled before applying the SYNIN signal. This time is required to flush the internal data paths. The receiver remains in this mode and further external sync pulses are ignored until the receiver is disabled and then reenabled to resynchronize or to return to normal mode. See Figure 2.

0 External sync not enabled.

1 External sync enabled.

Note that EXT SYNC and DCD ENABLE Rx cannot be asserted simultaneously since they use the same pin.

**[3] Strip Parity** — In COP and ASYNC modes with parity enabled, this bit controls whether the received parity bit is stripped from the data placed in the receiver FIFO. It is valid ony for programmed character lengths of 5, 6, and 7 bits. If the bit is stripped, the corresponding bit in the received data is set to zero.

0 Transfer parity bit as received.

1 Stop parity bit from data.

**[3] All Parties Address** — In BOP secondary modes, the assertion of this bit causes the receiver to 'wake-up' upon receipt of the address H'FF' or H'FF, FF', for single- and dual-octet address modes, respectively, in addition to its normal station address. This feature allows all stations to receive a message.

0 Don't recognize all parties address.

1 Recognize all parties address.

**[2] DCD Enable Receiver** — If this bit is asserted, the DCDN/SYNIN input must be Low in order for the receiver to operate. If the input is negated (goes High) while a character is being received, the receiver terminates receipt of the current message (this action in effect disables the receiver). If DCD is subsequently asserted, the receiver will search for the start bit, SYN pattern, or FLAG, depending on the channel protocol. (Note that the change of input can be programmed to generate an interrupt; the duration of the DCD level change is described in the discussion of the input and counter/timer status register (CTSR[5]).

0 DCD not used to enabled receiver.

1 DCD used to enabled receiver.

EXT SYNC and DCD ENABLE Rx cannot be asserted simultaneously since they use the same pin.

**[1:0] Received Bits per Character** — This field selects the number of data bits per character to be assembled by the receiver. The character length does not include the start, parity, and stop bits in the ASYNC or the parity bit in COP. In BOP modes, the character length for the address and control field is always 8 bits, and the value of this field only applies to the information field. If the number of bits assembled for the last character of the I-field is less than the value programmed in this field, RCL not zero (RSR[0]) is asserted and the actual number of bits received is given in TRSR[2:0].

## Receiver Timing Register (RTRA, RTRB)

**[7] External Source** — This bit selects the RTxC pin or the TRxC pin of the channel as the receiver or DPLL clock input, when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0 External input form RTxC pin.

1 External input form TRxC pin.

**[6:4] Receiver Clock Select** — This field selects the clock for the receiver.

000 External clock from TRxC or RTxC at 1X the shift (baud) rate.

001 External clock fromTRxC or RTxC at 16X the shift rate. Used for ASYNC mode only.

010 Internal clock from the bit rate generator at 32X the shift rate. Clock is divided by two before used by the receiver logic, which operates at 16X the baud rate. Rate selected by [3:0]. Used for ASYNC mode only.

011 Internal clock from counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate. Clock is divided by two before use in the receiver logic. Used for ASYNC mode only.

100 Internal clock from the digital phase-locked loop. The clock for the DPLL is a 64X clock from the crystal oscillator or system clock input. (The input to the oscillator is divided by two).

101 Internal clock from the digital phase-locked loop. The clock for the DPLL is an external 32X clock from the RTxC or TRxC pin, as selected by [7].

110 Internal clock from the digital phase-locked loop. The clock for the DPLL is a 32X clock from the BRG. The frequency is programmed by [3:0].

111 Internal clock from the digital phase-locked loop. The clock for the DPLL is a 32X clock from the counter/timer of the channel.

**[3:0] Bit Rate Select —** This field selects an output from the bit rate generator to be used by the receiver circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 5.

## Output and Miscellaneous Register (OMRA, OMRB)

**[7:5] Transmitted Residual Character Length —** In BOP modes, this field determines the number of bits transmitted for the last character in the information field. This length applies to:

- The character in the transmit FIFO accompanied by the FIFOed TEOM command.
- The character loaded into the FIFO by the DMA controller if DONEN is simultaneously asserted and TPR[4] is asserted.
- The character loaded into the FIFO which causes the counter to reach zero count when TPR[4] is asserted.

The length of all other characters in the frame's information field is selected by TPR[1:0]. If this field is 111, the number of bits in the last character is the same as programmed in TPR[1:0].

**[4] TxRDY Activate Mode —**

0 FIFO not full. The channel's TxRDY status bit is asserted each time a character is transferred from the transmit FIFO to the transmit shift register. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is automatically negated.

1 FIFO empty. The channel's TxRDY status bit is asserted when a character transfer from the transmit FIFO to the transmit shift register causes the FIFO to become empty. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is negated.

If the TxRDY status bit is reset by the CPU, it will remain negated regardless of the current state of the transmit FIFO, until it is asserted again due to the occurrence of one of the above conditions.

**[3] RxRDY Activate Mode —**

0 FIFO not empty. The channel's RxRDY status bit is asserted each time a character is transferred from the receive shift register to the receive FIFO. If not reset by the CPU, RxRDY remains asserted until the receive FIFO is empty, at which time it is automatically negated.

1 FIFO full. The channel's RxRDY status bit is asserted when a character transfer from the receive shift register to the receive FIFO causes the FIFO to become full. If not reset by the CPU, RxRDY reamins asserted until the FIFO is empty, at which time it is negated.

The RxRDY status bit will also be asserted, regardless of the receiver FIFO full condition, when an end-of-message character is loaded in the RxFIFO (BOP/BISYNC), when a BREAK condition (ASYNC mode) is detected in RSR[2], or when the counter/timer is programmed to count received characters and the character which causes it to reach zero is loaded in the FIFO (all modes). (Refer to the Detailed Operation of the receiver.)

If reset by the CPU, the RxRDY status bit will remain negated, regardless of the current state of the receiver FIFO, until it is asserted again due to one of the above conditions.

**[2] General Purpose Output 2 —** This general purpose bit is used to control the TxDRQN/GPO2/RTSN pin, when it is used as an output. The output is High when the bit is a 0 and is Low when the bit is a 1.

**[1] General Purpose Output 1 —** This bit is used to control the RTxDRQN/GPO1N output, which is a general purpose output when the channel is not in DMA mode. The output is High when the bit is a 0 and is Low when the bit is a 1.

**[0] Request-to-Send Output —** This bit controls the TxDRQN/GPO2N/RTSN and SYNOUTN/RTSN pin, when either is used as a RTS output. The output is High when the bit is a 0 and is Low when the bit is a 1.

## Counter/Timer Control and Value Registers

There are five registers in this set consisting of the following:

1. Counter/timer control register (CTCRA/B).
2. Counter/timer preset Highland Low registers (CTPRHA/B, CTPRLA/B).
3. Counter/timer (current value) High and Low registers (CTHA/B, CTLA/B)

The format of each of the registers of this set is contained in Table 6. The control register contains the operational information for the counter/timer. The preset registers contain the count which is loaded into the counter/timer circuits. The third group contains the current value of the counter/timer as it operates.

## Counter/Timer Control Register (CTCRA/CTCRB)

**[7] Zero Detect Interrupt —** This bit determines whether the assertion of the C/T ZERO COUNT status bit (ICTSR[6]) causes an interrupt to be generated.

0 Interrupt disabled.

1 Interrupt enabled if master interrupt enabled (ICR[1] or ICR[0]) is asserted.

**[6] Zero Detect Control —** This bit determines the action of the counter upon reaching zero count.

0 The counter/timer is preset to the value contained in the counter/timer preset registers (CTPRL, CTPRH) at the next clock edge.

1 The counter/timer continues counting without preset. The value at the next clock edge will be H'FFFF'.

**[5] Counter/Timer Output Control —** This bit selects the output waveform when the counter/timer is selected to be output on TRxC or RTxC.

1 The output is a single clock positive width pulse each time the C/T reaches zero count. (The duration of this pulse is one clock period.)

0 The output toggles each time the C/T reaches zero count. The output is cleared to Low by either of the preset counter/timer commands.

**[4:3] Clock Select —** This field selects whether the clock selected by [2:0] is prescaled prior to being applied to the input of the C/T.

00 No prescaling.

01 Divide clock by 16.

10 Divide clock by 32.

11 Divide clock by 64.

**[2:0] Clock Source —** This field selects the clock source for the counter/timer.

000 RTxC pin. Pin must be programmed as input.

001 TRxC pin. Pin must be programmed as input.

010 Source is the crystal oscillator or system clock input divided by four.

011 This selects a special mode of operation. In this mode the counter, after receiving the 'start C/T' command, delays the start of counting until the RxD input goes Low. It continues counting until the RxD input goes High, then stops and sets the C/T zero count status bit. The CPU can use the value in the C/T to determine the bit rate of the incoming data. The clock is the crystal oscillator or system clock input divided by four.

100 Source is the 32X BRG output selected by RTR[3:0] of own channel.

101 Source is the 32X BRG output selected by TTR[3:0] of own channel.

110 Source is the internal signal which loads received characters from the receive shift register into the receiver FIFO. When operating in this mode, the FIFOed EOM status bit (RSR[7]) shall be set when the character which causes the count to go to zero is loaded into the receive FIFO.

111 Source is the internal signal which transfers characters from the data bus into the transmit FIFO. When operating in this mode, and if the TEOM on zero count or done control bit (TPR[4]) is asserted, the FIFOed send EOM command will be automatically asserted when the character which causes the count to go to zero is loaded into the transmit FIFO.

## Table 6. Counter/Timer Control and Value Register Bit Formats

COUNTER/TIMER CONTROL REGISTER

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (CTCRA, CTCRB) | Zero Detect Interrupt | Zero Detect Control | Output Control | Prescaler | | Clock Source | | |
| | 0 — disable<br>1 — enabled | 0 — preset<br>1 — continue | 0 — square<br>1 — pulse | 00 — 1<br>01 — 16<br>10 — 32<br>11 — 64 | | 000 — RTxC pin<br>001 — TRxC pin<br>010 — X1/CLK divided by 4<br>011 — X1/CLK divided by 4 gated by RxD<br>100 — Rx BRG<br>101 — Tx BRG<br>110 — Rx characters<br>111 — Tx characters | | |

COUNTER/TIMER PRESET REGISTER HIGH

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (CTPRHA, CTPRHB) | Most significant bits of counter/timer preset value. | | | | | | | |

COUNTER/TIMER PRESET REGISTER LOW

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (CTPRLA, CTPRLB) | Least significant bits of counter/timer preset value. | | | | | | | |

COUNTER/TIMER REGISTER HIGH

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (CTHA, CTHB) | Most significant bits of counter/timer. | | | | | | | |

COUNTER/TIMER REGISTER LOW

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (CTLA, CTLB) | Least significant bits of counter/timer. | | | | | | | |

### Counter/Timer Preset High Register (CTPRHA, CTPRHB)

**[7:0] MSB —** This regsiter contains the eight most significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset regsiter command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is negated. The minimum 16-bit counter/timer preset value is H'0002'.

### Counter/Timer Preset Low Register (CTPRLA, CTPRLB)

**[7:0] LSB —** This register contains the eight least significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset register command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is negated. The minimum 16-bit counter/timer preset value is H'0002'.

### Counter/Timer High Register (CTHA, CTHB)

**[7:0] MSB —** A read of this 'register' provides the eight most significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read in order to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

### Counter/Timer Low Register (CTLA, CTLB)

**[7:0] LSB —** A read of this 'register' provides the eight least significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read, in order to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

### Interrupt Control and Status Registers

This group of registers define mechanisms for communications between the DUSCC and the processor and contain the device status information. Four registers, available for each channel, and four common device registers comprise this group which consists of the following:

1. Interrupt Enable Register (IERA/B).
2. Receiver Status Register (RSRA/B).
3. Transmitter and Receiver Status Register (TRSRA/B).
4. Input and Coutner/Timer Status Register (ICTSRA/B).
5. Interrupt Vector Register (IVR) and Modified Interrupt Vector Register (IVRM).
6. Interrupt control register (ICR).
7. General status register (GSR)

See Table 7 for bit formats and Figure 3 for table relationships.

### Interrupt Enable Register (IERA, IERB)

This register controls whether the assertion of bits in the channel's status registers causes an interrupt to be generated. An additional condition for an interrupt to be generated is that the channel's master interrupt enabled bit, ICR[0] or ICR[1], be asserted.

**[7] DCD/CTS —**

0 Interrupt not enabled.

1 Interrupt generated if ICTSR[4] or ICTSR[5] are asserted.

**[6] TxRDY —**

0 Interrupt not enabled.

1 Interrupt generated if TxRDY (GSR[1] or GSR[5] for Channels A and B, respectively) is asserted.

**[5] TRSR 73 —**

0 Interrupt not enabled.

1 Interrupt generated if bits 7, 6, 5, 4 or 3 of the TRSR are asserted.

**[4] RxRDY —**

0 Interrupt not enabled.

1 Interrupt generated if RxRDY (GSR[0] or GSR[4] for Channels A and B, respectively) is asserted.

**[3] RSR 76 —**

0 Interrupt not enabled.

1 Interrupt generated if bits 7 or 6 of the RSR are asserted.

**[2] RSR 54 —**

0 Interrupt not enabled.

1 Interrupt generated if bits 5 or 4 of the RSR are asserted.

**[1] RSR 32 —**

0 Interrupt not enabled.

1 Interrupt generated if bits 3 or 2 of the RSR are asserted.

### Table 7. Interrupt Control and Status Register Bit Format

RECEIVER STATUS REGISTER

| | *BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (RSRA, RSRB) ASYNC | # Char compare | RTS negated | Overrun error | not used | BRK end detect | BRK start detect | # Framing error | # Parity error |
| COP | # EOM detect + | PAD error + | Overrun error | not used | not used | Syn detect | # CRC error | # Parity error |
| BOP | # EOM detect | Abort detect | Overrun error | Short frame detect | Idle detect | Flag detect | # CRC error | # RCL not zero |
| LOOP | # EOM detect | Abort/EOP detect | Overrun error | Short frame detect | Turn-around detect | Flag detect | # CRC error | # RCL not zero |

NOTES:
# Status bit is FIFOed.
+ COP BISYNC mode only
* All modes indicate character count complete.

**Table 7. Interrupt Control and Status Register Bit Format** (Continued)

**TRANSMITTER AND RECEIVER STATUS REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (TRSRA, TRSRB) ASYNC | Transmitter empty | CTS underrun | not used | Send break ack | DPLL error | not used | not used | not used |
| COP | Transmitter empty | CTS underrun | Frame complete | Send SOM ack | DPLL error | not used | Rx hunt mode | Rx xpnt mode |
| BOP | Transmitter empty | CTS underrun / Loop sending* | Frame complete | Send SOM/ abort ack | DPLL error | Rx Residual Character Length: 000 — 0 bit; 001 — 1 bits; 010 — 2 bits; 011 — 3 bits | | 100 — 4 bits; 101 — 5 bits; 110 — 6 bits; 111 — 7 bits |

NOTE:
* Loop mode only.

**INPUT AND COUNTER/TIMER STATUS REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (ICTSRA, ICTSRB) | C/T running | C/T zero count | Delta DCD | Delta CTS/LC | DCD | CTS/LC | GPI2 | GPI1 |

**INTERRUPT ENABLE REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (IERA, IERB) | DCD/CTS | TxRDY | TRSR [7:3] | RxRDY | RSR[7:6] | RSR [5:4] | RSR [3:2] | RSR [1:0] |
| | 0 — no 1 — yes | 0 — no 1 — yes | 0 — no 1 — yes | 0 — no 1 — yes | 0 — no 1 — yes | 0 — no 1 — yes | 0 — no 1 — yes | 0 — no 1 — yes |

**INTERRUPT VECTOR REGISTER AND INTERRUPT VECTOR MODIFIED REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (IVR, IVRM) | 8-bit interrupt vector | | | | | | | |

**GENERAL STATUS REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (GSR) | Channel B | | | | Channel A | | | |
| | External or C/T Status | Rx/Tx status | TxRDY | RxRDY | External or C/T status | Rx/Tx status | TxRDY | RxRDY |

**INTERRUPT CONTROL REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (ICR) | Channel A/B Interrupt Priority | | Vector Mode | | Bits to Modify | Vector Includes Status | Channel A Master Int Enable | Channel B Master Int Enable |
| | 00 — Channel A<br>01 — Channel B<br>10 — interleaved A<br>11 — interleaved B | | 00 — vectored<br>01 — vectored<br>10 — vectored<br>11 — non vectored | | 0 — 2:0<br>1 — 4:2 | 0 — no<br>1 — yes | 0 — no<br>1 — yes | 0 — no<br>1 — yes |

**[0] RSR 10 —**

0 Interrupt not enabled.

1 Interrupt generated if bits 1 or 0 of the RSR are asserted.

## Receiver Status Register (RSRA, RSRB)

This register informs the CPU of receiver status. Bits indicated as 'not used' in a particular mode will read as zero. The logical OR of these bits is presented in GSR[2] or GSR[6] (ORed with the bits of TRSR) for Channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only be performing a write operation to the status register with the bits to be reset being ones in the accompanying data word, or when the RESETN input is asserted, or when a 'reset receiver' command is issued.

Certain status bits are specified as being FIFOed. This means that they occupy positions in a status FIFO that correspond to the data FIFO. As the data is brought to the top of the FIFO (the position read when the RxFIFO is read), the FIFOed status bits are logically ORed with the previous contents of the corresponding bits in the status register. This permits the user to obtain status either character by character or on a block basis. For character by character status, the SR bits should be read and then cleared before reading the character data from RxFIFO. For block status, the status register is initially cleared and then read after the message is received. Asserted status bits can be programmed to generate an interrupt (see Interrupt Enable Register).

**[7] Character Count Complete (All Modes), Character compare (ASYNC), EOM (BISYNC/BOP/LOOP) —** If the counter/timer is programmed to count received characters, this bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. It is also asserted to indicate the following conditions:

ASYNC The character currently at the top of RxFIFO matched the contents of S1R. A character will not compare if it is received with parity error even if the data portion matches.

BISYNC The character currently at the top of the FIFO was either a text message terminator or a control sequence received outside of a text or header field. See Detailed Operation of COP Receiver. If transfer FCS to FIFO (RPR[6]) is set, the EOM will instead be tagged onto the last byte of the FCS. Note that if an overrun occurs during receipt of a message, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. For 2 byte EOM comparisons, only the second byte is tagged (assuming the CRC is not transferred to the FIFO).

BOP, LOOP The character currently at the top of the FIFO was the last character of the frame. If trnasfer FCS to FIFO (RPR[6]) is asserted, the EOM will be tagged instead onto the last byte of the FCS. Note that if an overrun occurs, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. This bit will not be set when an abort is received.

**[6] RTS Negated (ASYNC), PAD Error (BISYNC), ABORT (BOP) —**

ASYNC The RTSN output was negated due to receiving the start bit of a new character while the RxFIFO was full (see RPR[4]).

BISYNC PAD error detected (see RPR[5]).

LOOP An ABORT sequence consisting of a zero followed by seven ones was received after receipt of the first address octet but before receipt of the closing FLAG. The user should read RxFIFO until it is empty and determine if any valid characters from a previous frame are in the FIFO. If no character with a tagged EOM detect ([7]) is found, all characters are from the current frame and should be discarded along with any previously read by the CPU. An ABORT detect causes the receiver to automatically go into search for FLAG state. An abort during a valid frame does not cause the CRC to reset; this will occur when the next frame begins.

LOOP Performs the ABORT detect function as described for BOP without the restriction that the pattern be detected during an active frame. A zero followed by seven ones is the end-of-poll sequence which allows the transmitter to go active if the 'go active on poll' command has been invoked.

**[5] Overrun Error (All Modes) —** A new character was received while the receive FIFO was full and a character was already waiting in the receive shift register to be transferred to the FIFO. the DUSCC protects the five characters previously assembled (four in RxFIFO, one in the Rx shift register) and discards the overrunning character(s). After the CPU reads the FIFO, the character waiting in the RxSR will be loaded into the available FIFO position. This releases the RxSR and a new character assembly will start at the next character boundary. In this way, only valid characters will be assembled, i.e., no partial character assembly will occur regardless of when the RxSR became available during the incoming data stream.

**[4] Short Frame (BOP/LOOP) —**

ASYNC Not used

COP Not used

BOP, LOOP A closing flag was received with missing fields in the frame. See detailed operation for BOP receiver.

**[3] BREAK End Detect (ASYNC), IDLE (BOP), Turnaround (LOOP) —**

ASYNC 1X clock mode: The RxD input has returned to the marking state for at least one period of the 1X receiver clock after detecting a BREAK.
16X clock mode: The RxD input has returned to the marking (High) state for a least one-half bit time after detecting a BREAK. A half-bit time is defined as eight clock cycles of the 16X receiver clock.

COP Not used.

BOP An IDLE sequence consisting of a zero followed by fifteen ones was received. During a valid frame, an abort must precede an idle. However, outside of a valid frame, an idle is recognized and abort is not.

LOOP A turnaround sequence consisting of eight contiguous zeros was detected outside of an active frame. This should normally be used to terminate transmitter operation and return the system to the 'echoing RxD' mode.

**[2] BREAK Start Detect (ASYNC), SYN Detect (COP), FLAG Detect (BOP/LOOP) —**

ASYNC An all zero character, including parity (if specified) and first stop bit, was received. The receiver shall be capable of detecting breaks which begin in the middle of a previous character. Only a single all-zero character shall be put into the FIFO when a break is detected. Additional entries to the FIFO are inhibited until the end of break has been detected (see above) and a new character is received.

COP A SYN pattern was received. Refer to Detailed Operation for definition of SYN patterns. Set one bit time after detection of SYN pattern in HSRH, HSRL. See Figure 1 for receiver data path.

BOP, LOOP A FLAG frequency (01111110) was received. Set one bit time after FLAG is detected in CCSR. See Figure 1 for receiver data path.

**[1] Framing Error (ASYNC), CRC Error (COP/BOP/LOOP) —**

ASYNC At the first stop bit position the RxD input was in the Low (space) state. The receiver only checks for framing error at the nominal center of the first stop bit regardless of the number of stop bits programmed in TPR[7:4]. This bit is not set for BREAKS.

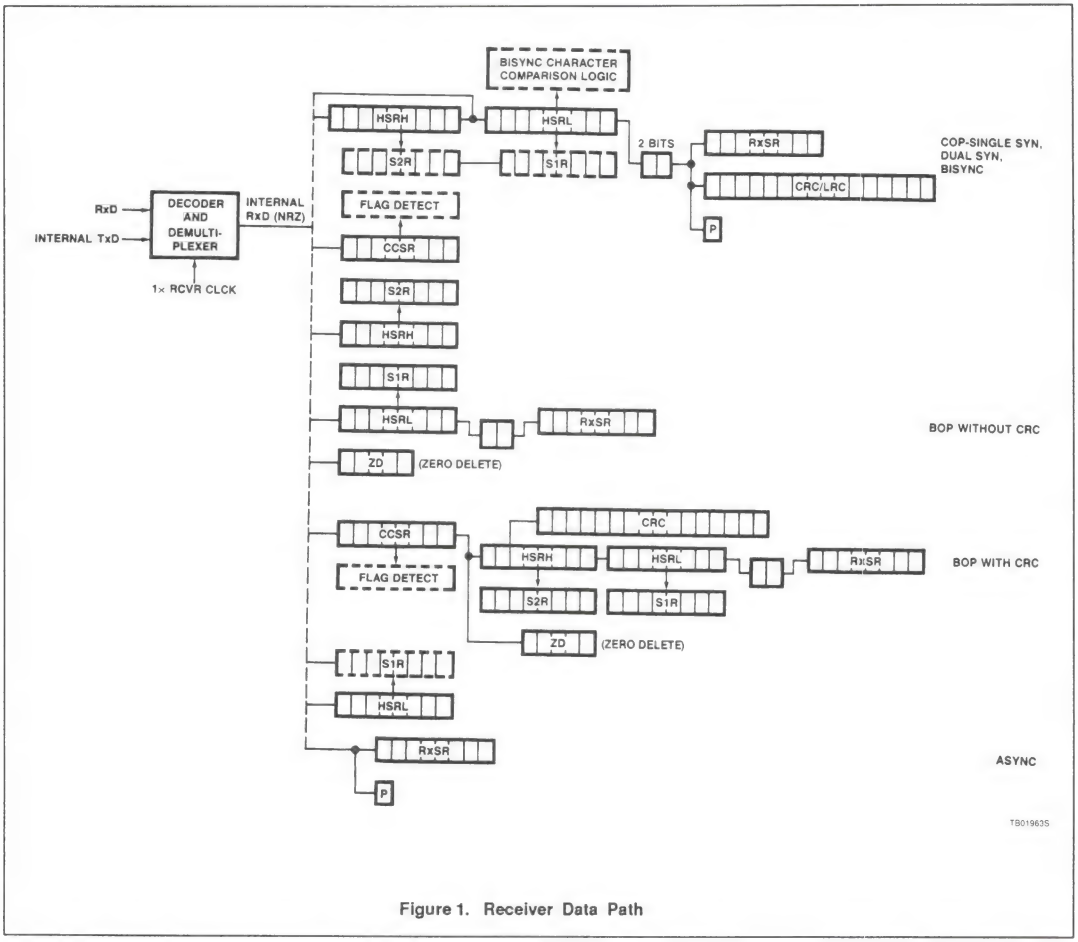



**Figure 1. Receiver Data Path**

COP — In BISYNC COP mode, this bit is set upon receipt of the BCC byte(s), if any, to indicate that the received BCC was in error. The bit is normally FIFOed with the last byte of the frame (the character preceding the first BCC byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last BCC byte. The value of this bit should be ignored for non-test messages or if the received frame was aborted via an ENQ. In non-BISYNC COP modes, the bit is set with each received character if the current value of the CRC checker is not equal to the non-error value (see CMR2[2:0]).

BOP, LOOP — This bit is set upon receipt of the FCS byte(s), if any, to indicate that the received FCS was in error. The bit is normally FIFOed with the last byte of the I field (the character preceding the first FCS byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last FCS byte.

**[0] Parity Error (ASYNC/COP), RCL Not Zero (BOP/LOOP) —**

ASYNC — The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated.

COP — The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated. A SYN or other character received with parity error is treated as a data character. Thus, a SYN with parity error received while in SYN search state will not establish character sync. Characters received with parity error while in the SYN search state will not set the error bit.

BOP, LOOP — The last character of the I field did not have the character length specified in RPR[1:0]. The actual received character length of this byte can be read in TRSR[2:0]. This bit is FIFOed with the EOM character but TRSR[2:0] is not. An exception occurs if the command to transfer the FCS to the FIFO is active. In this case, the bit will be FIFOed with the last byte of the FCS, i.e., with REOM. In the event that re-

sidual characters from two consecutive frames are received and are both in the FIFO, the length in TRSR[2:0] applies to the last received residual character.

## Transmitter/Receiver Status Register (TRSRA, TRSRB)

This register informs the CPU of transmitter and receiver status. Bits indicated as not used in a paritcular mode will read as zero, except for bits [2:0], which may not be zero. The logical-OR of bits [7:3] is presented in GSR[2] or GSR[6] (ORed with the bits of RSR) for channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only:

1. By performing a write operation to the status register with the bits to be reset being ones in the accompanying data word [7:3].
2. When the RESETN input is asserted.
3. For [7:4], when a 'reset transmitter' command is issued.
4. For [3:0], when a 'reset receiver' command is issued.
5. For [2:0], see description in BOP mode.

Asserted status bits in [7:3] can be programmed to generate an interrupt. See IER.

**[7] Transmitter Empty —** Indicates that the transmit shift register has completed serializing a character and found no other character to serialize in the TxFIFO. The bit is not set until at least one character from the transmit FIFO (not including PAD characters in synchronous modes) has been serialized. The transmitter action after transmitter empty depends on operating mode:

ASYNC The TxD output is held in the MARK state until another character is loaded into the TxFIFO. Normal operation then continues.

COP Action is specified by TPR[7:6].

BOP, LOOP Action is specified by TPR[7:6].

**[6] CTS Underrun (ASYNC/COP/BOP), Loop sending (LOOP) —**

ASYNC, COP, BOP This bit is set only if CTS enable Tx (TPR[2]) is asserted. It indicates that the transmit shift register was ready to begin serializing a character and found the CTSN input negated. In ASYNC mode, this bit will be reasserted if cleared by the CPU while the CTSN input is negated.

LOOP Asserted when the go active on poll command has been invoked and an EOP sequence has been invoked and an EOP sequence has been detected, causing the transmitter to go active by changing the EOP to a FLAG (see Detailed Operation of transmitter).

**[5] Frame Complete (COP/BOP) —**

ASYNC Not used.

COP Asserted at the beginning of transmission of the end of message sequence invoked by which is either a TEOM command, or when TPR[4] = 1, or TPR[7:6] = 00. The CPU can invoke the TSOM command after this bit is set to control the number of SYNs between transmitted frames.

BOP Asserted at the beginning of transmission of the end of message sequence which is invoked by either a TEOM command, or when TPR[4] = 1, or TPR[7:6] = 00. The CPU can invoke the TSOM command after this bit is set to control the number of FLAGs between transmitted frames.
In COP/BOP modes, the frame complete status bit is set during the next-to-last bit (on TxD pin) of the last character in the data/information field. In BOP mode, if a 1-bit residual character is selected through OMR[7:5], then this bit is set during the next-to-last bit (on TxD pin) of the last full length character of the information field.

**[4] Send Break Ack (ASYNC)/Send SOM ACK (COP)/Send SOM-Abort Ack (BOP —**

ASYNC Set when the transmitter begins transmission of a break in response to the send break command. If the command is reinvoked, the bit will be set again at the beginning of the next character time. The user can control the length of the break by counting character times through this mechanism.

COP Set when the transmitter begins transmission of a SYN pattern in response to the TSOM or TSOMP command. If the command is reinvoked, the bit will be set again at the beginning of the next transmitted SYN pattern. The user can control the number of SYNs which are sent through this mechanism.

BOP Set when the transmitter begins transmission of a FLAG/ABORT in response to the TSOM or TSOMP or TABRK command. If the command is reinvoked, the bit will be set again at the beginning of the next transmitted FLAG/ABORT. The user can control the number of FLAGs/ABORTs which are sent through this mechanism.

**[3] DPLL Error —** Set while the DPLL is operating in FM mode to indicate that a data transition was not detected within the detection window for two consecutive bits and that the DPLL was forced into search mode. This feature is disabled when the DPLL is specified as the clock source for the transmitter via TTR[6:4].

**[2:0] Received Residual Character Length (BOP) —**

BOP This field should be examined to determine the length of the last character of the I field (character tagged with REOM status bit) if RSR[0] is set to indicate that the length was not equal to the character length specified in RPR[1:0]. This field is negated when a reset receiver or disabled receiver command is issued, or when the first control character for the next frame of data is in HSRL (see Figure 1). Care must be taken to read TRSR[2:0] before these bits are cleared.

**[1] Receiver in Hunt Mode (COP) —**

COP This bit is asserted after the receiver is reset or disabled. It indicates that the receiver is in the hunt mode, searching the data stream for a SYN sequence to establish character synchronization. The bit is negated automatically when character sync is achieved.

**[0] Receiver in Transparent Mode (BISYNC) —**

COP Indicates that a DLE-STX sequence was received and the receiver is operating in BISYNC transparent mode. Set two bit times after detection of STX in HSRL. See Figure 1 for receiver data path. Transparent mode operation is terminated and the bit is negated automatically when one of the terminators for transparent text mode is received (DLE-ETX/ETB/ITB/ENQ).

## Input and Counter/Timer Status Register (ICTSRA, ICTSRB)

This register informs the CPU of status of the counter/timer and inputs. The logical-OR of bits [6:4] is presented in GSR[3] or GSR[7] for Channels A and B, respectively. Unless otherwise specified, bits of this register are reset only:

1. By performing a write operation to the status register with the bits to be reset (ones in the accompanying data word for bits [6:4] only).
2. When the RESETN input is asserted (bits [7:4]) only.

**[7] Counter/Timing Running —** Set when the C/T is started by start C/T command and reset when it is stopped by a stop C/T command.

**[6] Counter/Timer Zero Detect** — Set when the counter/timer reaches zero count, or when the bit length measurement is enabled (CTCR [2:0] = 011) and the RxD input has returned High. The assertion of this bit causes an interrupt to be generated if ICTCR[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

**[5] Delta DCD** — The DCD input is sampled approximately every 6.8µs using the 32X, 4800 baud output from the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the DCD input, lasting at least 17µs, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if IER[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

**[4] Delta CTS/LC** — When not in loop mode, the CTS input is sampled approximately every 6.8µs using the 32X, 4800 baud output form the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the CTS input, lasting at least 17µs, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if IER[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

In SDLC loop mode, this bit is set upon transitions of the LC output. LC is asserted in response to the 'go on-loop' command when the receiver detects a zero followed by seven ones, and negated in response to the 'go off-loop' command when the receiver detects a sequence of eight ones.

**[3:2] State of DCD and CTS** — ICTSRx[3] reflects the state of the DCDxN input pin, while ICTSRx[2] reflects the state of CTSxN. When the bits are 0, the inputs are High, when they are 1, the pins are Low.

**[1:0] Current State of GPI2 and GPI1** — These fields provide the current state of the channels general purpose input pins. The bits valve are latched at the beginning of the read cycle.

## Interrupt Vector Register (IVR) and Modified Vector Register (IVRM)

**[7:0] Register Content** — If ICR[2] = 0, the content of IVR register is output on the data bus when the DUSCC has issued an interrupt request and the responding interrupt acknowledge (IACKN) is received. The value in the IVR is initialized to H'0F' on master reset. If 'vector includes status' is specified by ICR[2] = 1, bit [2:0] or [4:2] (depending on ICR[3]), of the vector are modified as shown in Table 9 to indicate the highest priority interrupt currently active. The priority is programmable through the ICR. This modified vector is stored in the IVRM. When ICR[2] = 1, the content of the IVRM is output on to the data bus on the interrupt acknowledge. The vector is not modified, regardless of the value of ICR[2], if the CPU has not written an initial vector into this register.

Either the modified or unmodified vector can also be read by the CPU via a normal bus read cycle (see Table 1). The vector value is locked at the beginning of the IACK or read cycle until the cycle is completed. If no interrupt is pending, an H'FF' is output when reading the IVRM or the IVR.

## Interrupt Control Register (ICR)

**[7:6] Channel A/B Interrupt Priority** — Selects the relative priority between Channels A and B. The state of this bit determines the value of the interrupt vector (see Interrupt Vector Register). The priority within each channel, from highest to lowest, is as follows:

0 Receiver ready.

1 Transmitter ready

2 Rx/Tx status.

3 External or C/T status.

00 Channel A has the highest priority. The DUSCC interrupt priorities from highest to lowest are as follows: A(0), A(1), A(2), A(3), B(0), B(1), B(2), B(3).

01 Channel B has the highest priority. the DUSCC interrupt priorities from highest to lowest are as follows: B(0), B(1), B(2), B(3), A(0), A(1), A(2), A(3).

10 Priorities are interleaved between channels, but Channel A has the highest priority between events of equal channel priority. The DUSCC interrupt priorities from highest to lowest are as follows: A(0), B(0), A(1), B(1), A(2), B(2), A(3), B(3)

11 Priorities are interleaved between channels, but Channel B has the highest priority between events of equal channel priority. The DUSCC interrupt priorities from highest to lowest are as follows: B(0), A(0), B(1), A(1), B(2), A(2), B(3), A(3).

**Table 8. Interrupt Status Encoding**

| IVRM [2:0]/ [4:2] | HIGHEST PRIORITY INTERRUPT CONDITION |
|---|---|
| 000 | Channel A receiver ready |
| 001 | Channel A transmitter ready |
| 010 | Channel A Rx/Tx status |
| 011 | Channel A external or C/T status |
| 100 | Channel B receiver ready |
| 101 | Channel B transmitter ready |
| 110 | Channel B Rx/Tx status |
| 111 | Channel B external or C/T status |

**[5:4] Vector Mode** — The value of this field determines the response of the DUSCC when the interrupt acknowledge (IACKN) is received from the CPU.

00 or 01 or 10 Vectored mode. Upon interrupt acknowledge, the DUSCC locks its current interrupt status until the end of the acknowledge cycle. If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have an interrupt, it propagates the acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]. Otherwise, the IACKN is ignored. Locking the interrupt status at the leading edge of IACKN prevents a device at High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

11 Non-vectored mode. The DUSCC ignores an IACK if one is received; the interrupt vector is not placed on the data bus. The internal interrupt status is locked when a read of the IVR or IVRM is performed. Except for the absence of the vector on the bus, the DUSCC performs as it does in vectored mode — the vector is prioritized and modified if programmed.

**[3] Vector Bits to Modify** — Selects which bits of the vector stored in the IVR are to be modified to indicate the highest priority interrupt pending in the DUSCC. See Interrupt Vector Register.

0 Modify bits 2:0 of the vector.

1 Modify bits 4:2 of the vector.

**[2] Vector Includes Status** — Selects whether the modified (includes status) (IVRM) or unmodified vector (IVR) is output in response to an interrupt acknowledge (see Interrupt Vector Register).

0 Unmodified vector.

1 Modified vector.

**[1] Channel A Master Interrupt Enable —**

0 Channel A interrupts are disabled.

1 Channel A interrupts are enabled.

**[0] Channel B Master Interrupt Enable —**

0 Channel B interrupts are disabled.

1 Channel B interrupts are enabled.

## General Status Register (GSR)

This register provides a 'quick look' at the overall status of both channels of the DUSCC. A write to this register with 1s at the corresponding bit positions causes TxRDY (bits 5 and 1) and/or RxRDY (bits 4 and 0) to be reset. The other status bits can be reset only by resetting the individual status bits that they point to.

**[7] Channel B External or Coutner/Timer Status —** This bit indicates that one of the following status bits is asserted: ICTSRB[6:4].

**[6] Channel B Receiver or Transmitter Status —** This bit indicates that one of the following status bits is asserted: RSRB[7:)], TRSRB[7:3].

**[5] Channel B Transmitter Ready —** The assertion of this bit indicates that one or more characters may be loaded into the Channel B transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4]. This bit can be asserted only when the transmitter is enabled. Disabling or resetting the transmitter negates TxRDY.

**[4] Channel B Receiver Ready —** The assertion of this bit indicates that one or more characters are available in the Channel B receiver FIFO to be read by the CPU. See description of OMR[3]. RxRDY is initially reset (negated) by a chip reset or when a 'reset Channel B receiver' command is invoked.

**[3] Channel A External or Counter/Timer Status —** This bit indicates that one of the following status bits is asserted: ICTSRA[6:4].

**[2] Channel A Receiver or Transmitter Status —** This bit indicates that one of the following status bits is asserted: RSRA[7:0], TRSRA[7:3].

**[1] Channel A Transmitter Ready —** The assertion of this bit indicates that one or more characters may be loaded into the Channel A transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4]. This bit can be asserted only when the transmitter is enabled. Disabling or resetting the transmitter negates TxRDY.

**[0] Channel A Receiver Ready —** The assertion of this bit indicates that one or more characters are available in the Channel A receiver FIFO to be read by the CPU. See description of OMR[3]. RxRDY is initially reset (negated) by a chip reset or when a 'reset Channel A receiver' command is invoked.

**Channel Command Register (CCRA, CCRB) —** Commands to the DUSCC are entered through the channel command register. The format of that register is shown in Table 9. A read of this register returns the last invoked command (with bits 4 and 5 set to 1).

## Transmitter Commands

0000 Reset transmitter. Causes the transmitter to cease operation immediately. The transmit FIFO is cleared and the TxD output goes into the marking state. Also clears the transmitter status bits (TRSR[7:4]) and resets the TxRDY status bit (GSR[1] or GSR[5] for Channels A and B, respectively). The counter/timer and other registers are not affected.

0001 Resest transmit CRC. This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be reset to its initial state prior to beginning transmission of the appended character.

0010 Enable transmitter. Enables transmitter operation, conditioned by the state of the CTS ENABLE Tx bit, TPR[2]. Has no effect if invoked when the transmitter has previously been enabled.

0011 Disable transmitter. Terminates transmitter operation and places the TxD output in the marking state at the next occurrence of a transmit FIFO empty condition. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted.

0100 Transmit start of message. Used in COP and BOP modes to initiate transmission of a frame after the transmitter is first enabled, prior to sending the contents of the FIFO. Can also be used to precisely control the number of SYN/FLAGs at the beginning of transmission or in between frames.

When the transmitter is first enabled, transmission will not begin untill this command (or the transmit SOM with PAD command, see below) is issued. The command causes the SYN (COP) or FLAG (BOP) pattern to be transmitted. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then reinvoke the command if multiple SYN/FLAGs are to be transmitted. Transmission of the FIFO characters begin when the command is no longer invoked. If the FIFO is empty, SYN/FLAGs continue to be transmitted until a character is loaded into the FIFO, but the status bit (TRSR[4]) is not set. Insertion of SYN/FLAGs between frames can be accomplished by invoking this command after the frame complete status bit (TRSR[5]) has been asserted in response to transmission of the end-of message sequence.

0101 Transmit start of message with opening PAD. Used in COP and BOP modes after the transmitter is first enabled to send a bit pattern for DPLL synchronization prior to transmitting the opening SYN (COP) or FLAG (BOP). the SYN/FLAG is sent at the next occurrence of a transmit FIFO empty condition. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted. While the PAD characters are transmitted, the character length is set to 8 bits, (regardless of the programmed length), and parity generation (COP), zero insertion (BOP) and LRC/CRC accumulation are disabled. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then invoke the transmit SOM command if multiple SYN/FLAGs are to be transmitted.

The TSOM/TSOMP commands, described above, are sampled by the controller in alternate bit times of the transmitter clock. As a consequence, the first bit time of a COP/BOP frame will be transmitted on the TxD pin, after a maximum of three bit times, after the command is issued. (The additional 1-bit delay in the data path is due to the data encoding logic.)

0110 Transmit end-of-message. This command is appended to the next character loaded into the transmit FIFO. It causes the transmitter to send the end-of message sequence (selected FCS in COP modes, FCS-FLAG in BOP modes) after the appended character is transmitted. Frame complete (TRSR[5]) is set when transmission of the FCS begins. This command is also asserted automatically if the TEOM on zero count or one control bit (TPR[4]) is asserted, and the counter/timer is programmed to count transmitted characters when the character which causes the count to go to zero is loaded into the transmit FIFO. TEOM is not recognized if the transmitter FIFO is full.

0111 Transmit Abort BOP/Transmit Break ASYNC. In BOP modes, causes an abort (eight ones) to be transmitted after transmission of the character currently in the shift register is completed. The transmitter then sends MARKs or FLAGs depending on the state of underrun control (TPR[7:6]). Send SOM/abort ack (TRSR[4]) is set when the transmission of the abort begins. If the command is reasserted before transmission of the previous ABORT is completed, the process will be repeated. This can be used to send the idle sequence. The 'transmit SOM' command must be used to initiate transmission of a new message. In either mode, invoking this command causes the transmit FIFO to be flushed (characters are not transmitted).

In ASYNC mode, causes a break (space) to be transmitted after transmission of the character currently in the shift register is completed. Send break ack (TRSR[4]) is set when the transmission of the break begins. The transmitter keeps track of character times. If the command is reasserted, send break ack will be set again at the beginning of the next character time. The user can use this mechanism to control the length of the break in character time multiples. Transmission of the break is terminated by issuing a 'reset Tx' or 'disableTx' command.

1000 Transmit DLE. Used in COP modes only. This command is appended to and FIFOed with the next character loaded into the transmitter FIFO. It causes the transmitter to send a DLE, (EBCDIC H'10', ASCII H'10') prior to transmitting the appended character. If the transmitter is operating in BISYNC transparent mode, the transmitter control logic automatically causes a second DLE to be transmitted whenever a DLE is detected at the top of the FIFO. In this case, the TDLE command should not be invoked. An extra (third) DLE, however, will not be sent if the transmit DLE command is invoked.

1001 Go active on poll. Used in BOP loop mode only. Causes the transmitter, if it is enabled, to begin sending when an EOP sequence consisting of a zero followed by seven ones is detected. The last one of the EOP is changed to zero, making it another FLAG, and then the transmitter operates as described in the detailed operation section. The loop sending status bit (TRSR[6]) is asserted concurrent with the beginning of transmission.

1010 Reset go active on poll. Clears the stored 'go active on poll' command.

1011 Go on-loop. Used in BOP loop mode to control the assertion of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the DUSCC will look for the receipt of a zero followed by seven ones, at which time it will assert the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the DUSCC to break into the loop without affecting loop operation. ' This command must be used to initiate loop mode operation.

1100 Go off-loop. Used in BOP loop mode to control the negation of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the DUSCc will look for the receipt of eight contiguous ones, at which time it will negate the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the DUSCC to get off the loop operation. This command is normally used to terminate loop mode operation.

1101 Exclude from CRC. This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be disabled while the appended character is being transmitted. Thus, that character is not included in the CRC accumulation.

## Receiver Commands

0000 Reset Receiver. Causes the receiver to cease operation, clears the receiver FIFO, clears the data path, and clears the receiver status (RSR[7:0], TRSR[3:0], and either GSR[0] or GSR[4] for Channels A and B, respectively). The counter/timer and other registers are not affected.

0001 Reserved.

0010 Enable receiver. Causes receiver operation to begin, conditioned by the state of the DCD ENABLED Rx bit, RPR[2]. Receiver goes into START, SYN, or FLAG search mode depending on channel protocol mode. Has no effect if invoked when the receiver has previously been enabled.

0011 Disable receiver. Terminates operation of the receiver. Any character currently being assembled will be lost. Does not affect FIFO or any status. While in COP mode, disabling the receiver does not clear the data path; in all other cases, it does.

## Counter/Timer Commands

0000 Start. Starts the counter/timer and prescaler.

0001 Stop. Stops the counter/timer and prescaler. Since the command may be asynchronous with the selected clock source, the counter/timer and/or prescaler may count one or more additional cycles before stopping.

0010 Preset to FFFF. Presets the counter timer to H'FFFF' and the prescaler to its initial value. This command causes the C/T output to go Low.

0011 Preset from CTPRH/CTPRL. Transfers the current value in the counter/timer preset registers to the counter/timer and presets the prescaler to its initial value. This command causes the C/T output to go Low.

## Digital Phase-Locked Loop Commands

0000 Enter Search Mode. This command causes the DPLL counter to be set to the value 15 and the clock output will be forced Low. The counter will be disabled until a transition on the data line is detected, at which point it will start incrementing. After the counter reaches a count of 31, it will reset to zero and cause the clock output to go from Low to High. The DPLL will then continue normal operaton. This allows theDPLL to be locked onto the data without pre-frame transitions. This command should not be used if the DPLL is programmed to supply the clock for the transmitter is active.

0001 Disable DPLL. Disables operation of the DPLL.

0010 Set FM Mode. Sets the DPLL to the FM mode of operation, used when FM0, FM1, or Manchester (NMRZ) is selected by CMR1[7:6].

0011 Set NRZI Mode. Sets the DPLL to the NRZI mode of operation, used when NRZ or NRZI is selected by CMR1[7:6].

0100 Reserved for test.

0101 Reserved for test.

**Table. 9 Command Register Bit Format**

**CHANNEL COMMAND REGISTER**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (CCRA, CCRB) | 00 = Transmitter CMD | | don't care | don't care | **Transmitter Command**<br>0000 — reset Tx<br>0001 — reset TxCRC*<br>0010 — enable Tx<br>0011 — disable Tx<br>0100 — transmit SOM (TSOM)<br>0101 — transmit SOM with PAD (TSOMP)<br>0110 — transmit EOM (TEOM)*<br>0111 — transmit ABORT/BREAK (TABRK)<br>1000 — transmit DLE (TDLE)*<br>1001 — go active on poll<br>1010 — reset go active on poll<br>1011 — go on-loop<br>1100 — go off-loop<br>1101 — exclude form CRC* | | | |
| | 01 = Receiver CMD | | don't care | don't care | **Receiver Command**<br>0000 — reset Rx<br>0001 — reserved<br>0010 — enable Rx<br>0011 — disable Rx | | | |
| | 10 = C/T CMD | | don't care | don't care | **Counter/Timer Command**<br>0000 — start<br>0001 — stop<br>0010 — preset to FFFF<br>0011 — preset from CTPRH/CTPRL | | | |
| | 11 = DPLL CMD | | don't care | don't care | **DPLL Command**<br>oooo — enter search mode<br>0001 — disable DPLL<br>0010 — set FM mode<br>0011 — set NRZI mode<br>0100 — reserved for test<br>0101 — reserved for test | | | |

## DETAILED OPERATION

### Interrupt Control

A single interrupt output (IRQN) is provided which is activated upon the occurrence of any of the following conditions:

Channel A external or C/T special condition

Channel B external or C/T special condition

Channel A Rx/Tx error or special condition

Channel B Rx/Tx error or special condition

Channel A TxRDY

Channel B TxRDY

Channel A RxRDY

Channel B RxRDY

Each of the above conditions occupies a bit in the General Status Register (GSR). If ICR[2] is set, the eight conditions are encoded into three bits which are inserted into bits [2:0] or [4:2] of the interrupt vector register. This forms the content of the IVRM during an interrupt acknowledge cycle. Unmodified and modified vectors can read directly through specified registers. Two of the conditions are the inclusive OR of several other maskable conditions:

- External or C/T special condition: Delta DCD, Delta CTS or C/T zero count (ICTSR[6:4]).
- Rx/Tx error or special condition: any condition in the Receiver Status Register (RSR[7:0]) or a transmitter or DPLL condition in the Transmitter and Receiver Status Register (TRSR[7:3]).

The TxRDY and RxRDY conditions are defined by OMR[4] and OMR[3], respectively. Also associated with the interrupt system are the Interrupt Enable Register (IER), one bit in the Counter/Timer Control Register (CTCR), and the Interrupt Control Register (ICR).

The IER is programmed to enable specified conditions or groups of conditions to cause an interrupt by asserting the corresponding bit. A negated bit prevents an interrupt from occurring when the condition is active and hence masks the interrupt. In addition to the IER, CTCR[7] could be programmed to enable or disable an interrupt upon the C/T zero count condition. The interrupt priorities within a channel are fixed. Priority between channels is controlled by ICR[7:6]. Refer to Table 8 and ICR[7:6].

The ICR contains the master interrupt enables for each channel (ICR[1] andICR[0]) which must be set if the corresponding channel is to cause an interrupt. The CPU vector mode is specified by ICR[5:4] which selects either vectored or non-vectored operation. If vectored mode is selected, the content of the IVR or IVRM is placed on the data bus when IACK is activated. If ICR[2] is set, the content of IVRM is output which contains the content of IVR and the encoded status of the interrupting condition.

Upon receiving an interrupt acknowledge, the DUSCC locks its current interrupt status until the end of the acknowledge cycle. If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have an interrupt, it propagates the

acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]; otherwise, the IACKN is ignored. Locking the interrupt status at the leading edge of IACKN prevents a device at a High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

## DMA Control

The DMA control section provides the interface to allow the DUSCC to operate with an external DMA controller. One of four modes of DMA can be programmed for each channel independently via CMR2[5:3]:

- Half-duplex single address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via a single DMA acknkowledge pin. The data transfer is accomplished in a single bus cycle — the DMA controller places the memory address of the source or destination of the data on the address bus and then issues the acknowledge signal, which causes the DUSCC to either write the data into its transmit FIFO (write request) or to output the contents of the top of the recieve FIFO (read request). The cycle is completed when the DTCN input is asserted by the DMA controller. This mode can be used when channel operation is half-duplex (e.g., BISYNC) and allows a single DMA channel to service the receiver and transmitter. The receiver and transmitter should not be enabled at the same time when half-duplex mode is programmed.
- Half-duplex dual address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via normal bus read and write cycles. The data transfer requires two bus cycles — the DMA controller acquires the data from the source (memory for a Tx DMA or DUSCC for a Rx DMA) on the first cycle and deposits it at the destination (DUSCC for a Tx DMA or memory for a Rx DMA) on the second bus cycle. This mode is used when channel operation is half-duplex (e.g., BISYNC) and allows a single DMA channel to service the receiver and transmitter.
- Full-duplex single address. This mode is similar to half-duplex single address mode but provides separate request and acknowledge pins for the receiver and transmitter.
- Full-duplex dual address. This mode is similar to half-duplex dual address mode but provides duplex dual address mode and provides separate request pins for the receiver and transmitter

Figures 4 through 7 describe operation of the DUSCC in the various DMA environments. Table 10 summarizes pins used for the DMA request and acknowledge function for the transmitter and receiver for the different DMA modes.

The DMA request signals are functionally identical to the TxRDY and RxRDY status signals for each serial channel except that the DMA request signals are negated on the leading edge of the acknowledge signal when the subsequent transfer causes the FIFO to become full (transmitter request) or empty (receiver request).

In non-DMA operation TxRDY and RxRDY signals are automatically negated only after the transfer is completed. The DMA read request can be programmed through OMR[3] be asserted either when any character is in the receive FIFO or only when the receive FIFO is full. Likewise, the DMA write request can be programmed through OMR[4] to be asserted either when the transmit FIFO is not full or only when the transmit FIFO is empty (The transmitter must be enabled for a DMA request to be asserted). The request signals are automatically negated when the respective data transfer cycle is completed and the FIFO becomes full (transmitter request) or empty (receiver request). If a transfer is completed and the FIFO is not left full (transmitter) or empty (receiver), the request stays Low. The request may be negated by the CPU with a status reset write cycle. (Although DONEN terminates all DMA transfers, it has no effect on the requests. The requests are a function of the FIFO status, but they can be negated by writing into the GSR.) When the serial channel is not operating in DMA mode, the request and acknowledge pins for the channel can be programmed for other functions (see Pin Descriptions).

## DMA DONEN Operation

As an input, DONEN is asserted by the DMA controller concurrent with the corresponding DMA acknowledge to indicate to the DUSCC that the character being transferred into the TxFIFO is the last character of the transmission frame. In synchronous modes, the DUSCC can be programmed through TPR[4] to automatically transmit the frame termination sequence (e.g., FCS-FLAG in BOP mode) upon receipt of this signal.

As an output, DONEN is asserted by the DUSCC under the following conditions:

a. In response to the DMA acknowledge for a receiver DMA request if the FIFOed RECEIVED EOM status bit (RSR[7]) is set for the character being transferred.

b. In response to the DMA acknowledge for a receiver DMA request if the counter/timer has been programmed to count transmitted characters and the terminal count has occurred.

## Block Transfers Using DTACK

The DTACKN line may be used to synchronize data transfers to and from the DUSCC utilizing a 'wait' state. Either the receive or the transmitter or both may be programmed for this mode of operation, independently for each channel, via CMR2[5:3].

In this mode, if the CPU attempts a write to the transmit FIFO and an empty FIFO position is not available, the DTACKN line will remain negated until a position empties. The data will then be written into the FIFO and DTACKN will be asserted to signify that the transfer is complete.

Similarly, a read of an empty receive FIFO will be held off until data is available to be transferred. Potentially, this mode can cause the microcomputer system to hang up if, for example, a read request was made and no further data was available.

**Table 10. DMA REQ and ACK Pins for Operational Modes**

| FUNCTION | HALF DUPLEX SINGLE ADDR DMA | HALF DUPLEX DUAL ADDR DMA | FULL DUPLEX SINGLE ADDR DMA | FULL DUPLEX DUAL ADDR DMA |
|---|---|---|---|---|
| RCVR REQ | RTxDRQN | RTxDRQN | RTxDRQN | RTxDRQN |
| TRAN REQ | Same as RCVR REQ | Same as RCVR REQ | TxDRQN | TxDRQN |
| RCVR ACK | RTxDAKN | Normal read RCVR FIFO | RTxDAKN | Normal read RCVR FIFO |
| TRAN ACK | Same as RCVR ACK | Normal write TRAN FIFO | TxDAKN | Normal write TRAN FIFO |

## Timing Circuits

The timing block for each channel consists of a crystal oscillator, a Bit Rate Generator (BRG), a Digital Phase-Locked Loop (DPLL) and a 16-bit Counter/Timer (C/T) (see Figure 8).

### Crystal Oscillator

The crystal oscillator operates directly from a crystal (normally 14.7456MHz if the internal BRG is to be used) connected across the X1/CLK and X2/IDCN pins with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to the X1/CLK pin. This signal is divided by two to provide the internal system clock.

### Bit Rate Generator

The BRG operates from the oscillator or external clock and is capable of generating 16-bit rates. These are available to the receiver, transmitter, DPLL, and C/T. The BRG output is at 32X the base bit rate. Since all sixteen rates are generated simultaneously, each receiver and transmitter may select its bit rate independently. The transmitter and receiver timing registers include a 4-bit field for this purpose (TTR[3:0], RTR[3:0]).

### Digital Phase-Locked Loop

Each channel of the DUSCC includes a DPLL used in synchronous modes to recover clock information from a received data stream. The DPLL is driven by a clock at nominally 32 times the data rate. This clock can be programmed, via RTR[7:4], to be supplied from an external input, from the receiver BRG, from the C/T, or directly from the crystal oscillator.

The DPLL uses this clock, along with the data stream to construct a data clock which may then be used as the DUSCC receive clock, transmit clock, or both. The output of the DPLL is a square wave at 1X the data rate. The derived clock can also be programmed to be output on a DUSCC pin; only the DPLL receiver output clock is available at the TRxC pin. Four commands are associated with DPLL operation: Enter search mode, set FM mode, set NRZI mode, and disable DPLL. The commands are described in the Command Register Description. Waveforms associated with the DPLL are illustrated in Figure 9.

**DPLL NRZI Mode Operation —** This mode is used with NRZ and NRZI data encoding. With this type of encoding, the transitions of the data stream occur at the beginning of the bit cell. The DPLL has a six-bit counter which is incremented by a 32X clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL output clock then rises at a count of 0 and falls at 16. Data is sampled on the rising edge of the clock. When a transition in the data stream is detected, the count length is adjusted by one or two counts, depending on the counter value when the transition occurs (see Table 11). A transition detection at the roll-over point (third column in Figure 11) is treated as a transition occurring at zero count.

The count length adjustments cause the rising edge of the DPLL output block to converge to the nominal center of the bit cell. In the worst case, which occurs when a DPLL pulse is coincident with the data edge, the DPLL converges after 12 data transitions.

For NRZ encoded data, a stream of alternating ones and zeros should be used as a synchronizing pattern. For NRZI encoded data, a stream of zeros should be used.

**Table 11. NRZI Mode Count Length**

| COUNT WHEN TRANSITION DETECTED | COUNT LENGTH ADJUSTMENT | COUNTER RESET AFTER COUNT REACHES |
|---|---|---|
| 0 — 7 | -2 | 29 |
| 8 — 15 | -1 | 30 |
| 16 — 23 | +1 | 32 |
| 24 — 30 | +2 | 33 |
| None detected | 0 | 31 |

**DPLL FM Mode Operation —** FM operation is used with FM0, FM1, and Manchester data encoding. With this type of encoding, transitions in the data stream always occur at the beginning of the bit cell for FM0 and FM1, or at the center of the bit cell for Manchester. The DPLL 6-bit counter is incremented by a 32X clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL receiver clock then rises on a count of 8 and falls on 24. (The DPLL transmitter clock output falls on a count of 16. It rises on a count of 0 if a transition has been detected between count of 16 and 23. For other cases, it rises 1/2 count of the 32X input clock sooner.) This provides a 1X clock with edges positioned at the nominal centers of the two halves of the bit cell. The transition detection circuit is enabled between counts of 8 and 23, inclusive. When a transition is detected, the count length is adjusted by one, depending on when the transition occurs (see Table 12).

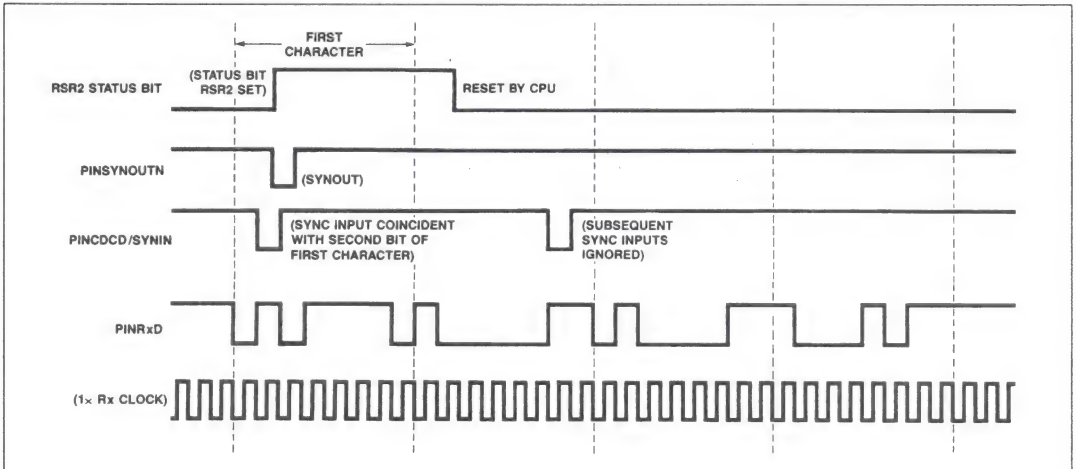



**Figure 2. External Sync Mode**

If a transition is not detected for two consecutive data bits, the DPLL is forced into search mode and the DPLL error status bit (TRSR[3]) is asserted. This feature is disabled when the DPLL output is used only as the transmitter clock.

To prevent the DPLL from locking on the wrong edges of the data stream, an opening PAD sequence should be transmitted. For FM0, a stream of at least 16 ones should be sent initially. For FM1, a minimum stream of 16 zeros should be sent and for Manchester encoding the initial data stream should consist of alternating ones and zeros.

**Table 12. FM Mode Count Length**

| COUNT WHEN TRANSITION DETECTED | COUNT LENGTH ADJUSTMENT | COUNTER RESET AFTER COUNT REACHES |
|---|---|---|
| 8 — 15 | -1 | 30 |
| 16 — 23 | +1 | 32 |
| 24 — 7 | Disabled | |
| None detected | 0 | 31 |

**Counter/Timer**

Each channel of the DUSCC contains a Counter/Timer (C/T) consisting of a 16-bit down counter, a 16-bit preset register, and associated control circuits. Operation of the counter/timer is programmed via the Counter/Timer Control Register (CTCR). There are also four commands associated with C/T operation, as described in the Command Description section.

The C/T clock source, clock prescaling, and operating mode are programmed via CTCR[2:0], CTCR[4:3], and CTCR[6], respectively. The preset register is loaded with minimum of 2 by the CPU and its contents can be transferred into the down counter by a command, or automatically upon reaching terminal count if CTCR[6] is negated. Commands are also available to stop and start the C/T and to preset it to an initial value of FFFF. Counting is triggered by the falling edge of the clocking input. The C/T zero count status bit, ICTSR[6], is set when the C/T reaches the terminal count of zero and ICTSR[7] indicates whether the counter is currently enabled or not.

An interrupt is generated upon reaching zero count if CTCR[7] and the channel's master interrupt enable are asserted. The output of the C/T can be programmed to be output on the channel's RTxC or TRxC pin (via PCR[4:0]) as either a single pulse or a square wave, as programmed in CTCR[5]. The contents of the C/T can be read at any time by the CPU, but the C/T should normally be stopped before this is done. Several C/T operating modes can be selected by programming of the counter/timer control register. Typical applications include:

1. Programmable divider. The selected clock source, optionally prescaled, is divided by the contents of the preset register. The counter automatically reloads itself each time the terminal count is reached. In this mode, the C/T may be programmed to be used as the Rx or Tx bit rate generator, as the input to the DPLL, or it may be output on a pin as either a pulse or a square wave. The C/T interrupt should be disabled in this mode.
2. Periodic interrupt generator. This mode is similar to the programmable divider mode, except that the C/T interrupt is enabled, resulting in a periodic interrupt to the CPU.
3. Delay timer. The counter is preset from the preset register and a clock source, optionally prescaled, is selected. An interrupt is generated upon reaching terminal count. The C/T continues counting without reloading itself and its contents may be read by the CPU to allow additional delay past the zero count to be determined.
4. Character counter. The counter is preset to FFFF by command and the clock source becomes the internal signal used to control loading of the Rx or Tx characters. This operation is selected by CTCR[2:0]. The C/T counts characters loaded into the RxFIFO by the receiver or loaded into the transmit FIFO by the CPU, respectively. The current character count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted. When counting Tx characters, the terminal count condition can be programmed through TPR[4] to cause an end of message sequence to be transmitted. When counting received characters, the FIFOed EOM status bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. The channel's 'reset Tx' or 'reset Rx' commands have no effect on the operation of the C/T.
5. External event counter. The counter is preset to FFFFF by command and an external clock source is selected. The current count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted.
6. Bit length measurement. The counter is preset to FFFF by command and the X1/CLK/4 clock input gated by RxD mode (optionally prescaled) is programmed. The C/T starts counting when RxD goes Low and stops counting when RxD goes High. At this time, ICTSR[6] is set and an interrupt (if enabled) is generated. The resulting count in the counter can be read by the CPU to determine the bit rate of the input data. Normally this function is used for asynchronous operation.

## Communication Channels A and B

Each communication channel of the DUSCC is a full-duplex receiver and transmitter that supports ASYNC, COP, and BOP transmission formats. The bit rate clock for each receiver and transmitter can be selected independently to come from the bit rate generator, C/T, DPLL, or an external input (such as a modem generated clock).

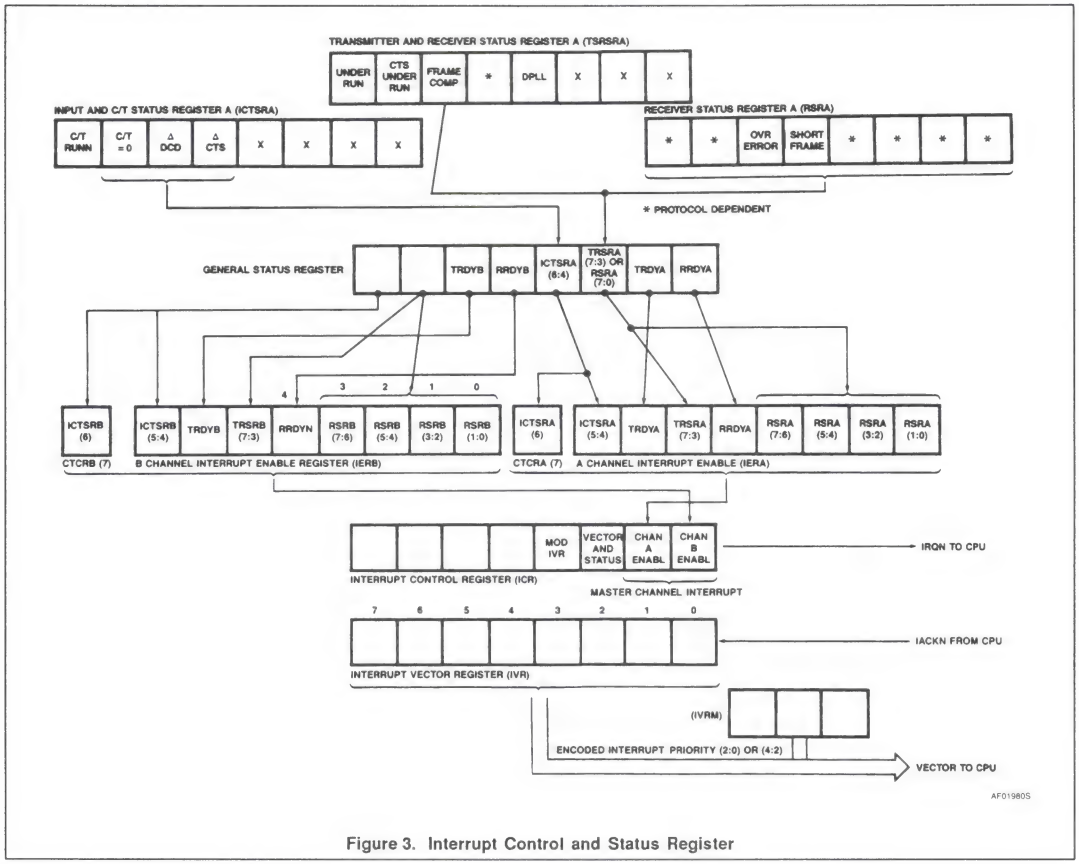



Figure 3. Interrupt Control and Status Register

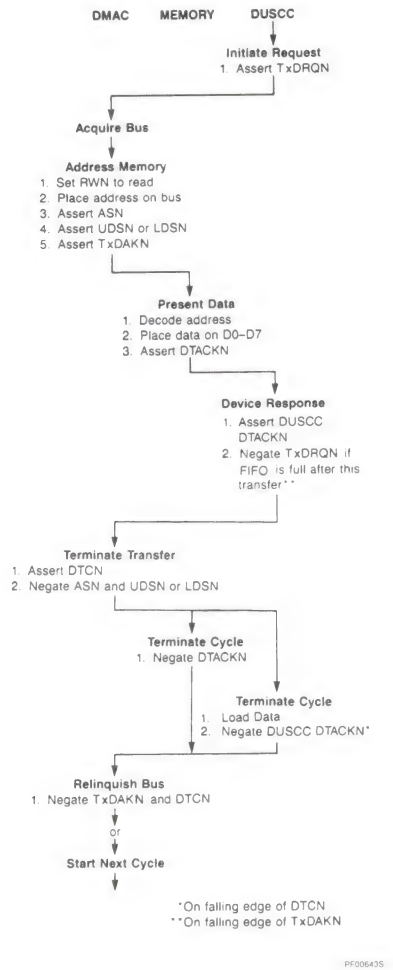



**Figure 4. Transmitter DMA Request Operation — Single Address Mode**

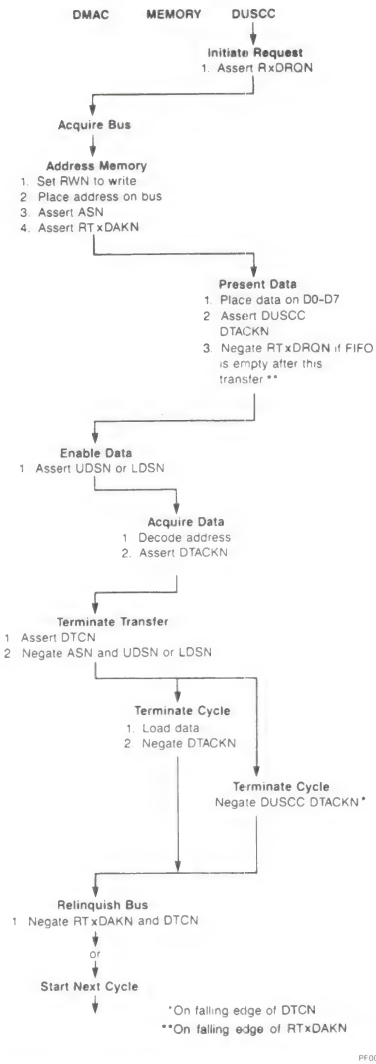



**Figure 5. Receiver DMA Request Operation — Single Address Mode**

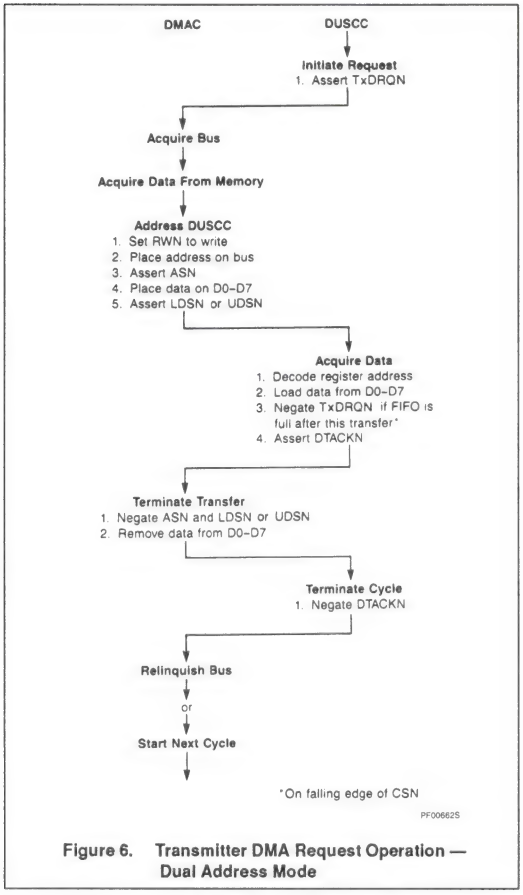



**Figure 6. Transmitter DMA Request Operation — Dual Address Mode**

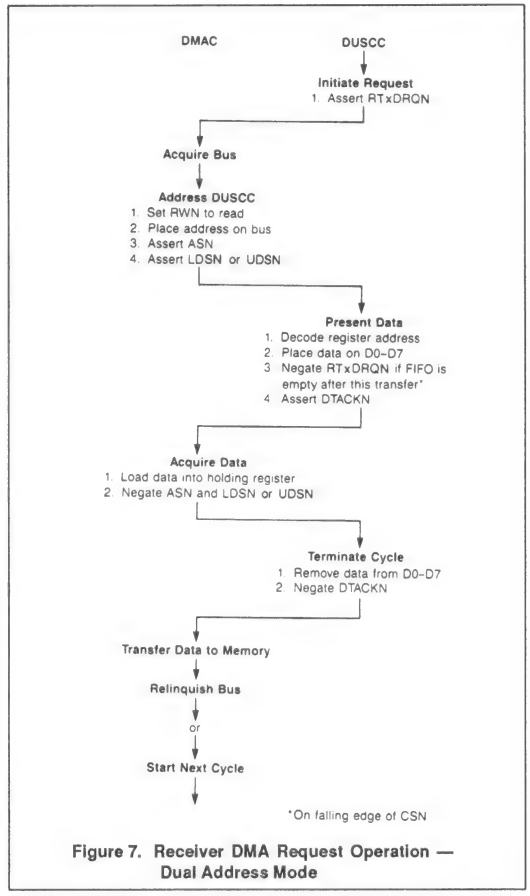
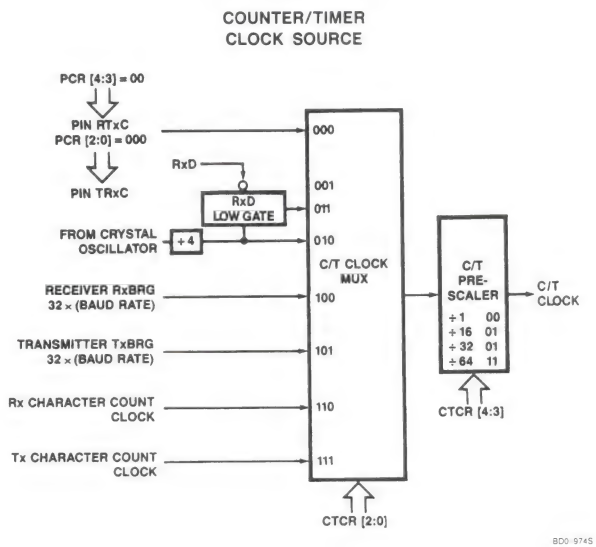
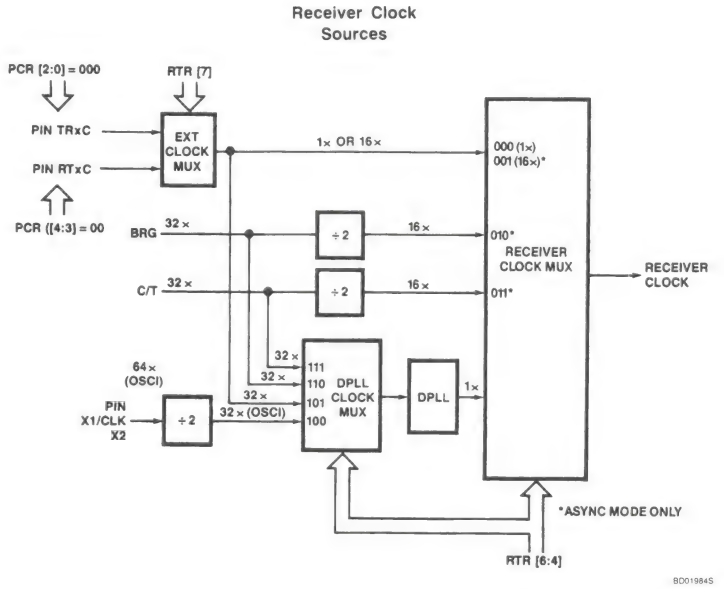


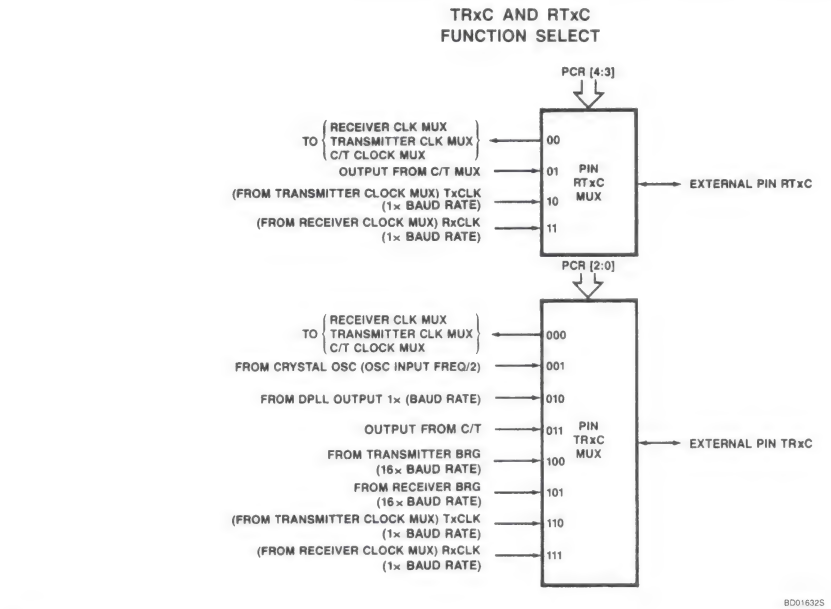

**Figure 7. Receiver DMA Request Operation — Dual Address Mode**




NOTE:
OSCI = crystal or EXT generator input.

Figure 8. Timing Block




**NOTE:**
OSCI = crystal or EXT generator input.

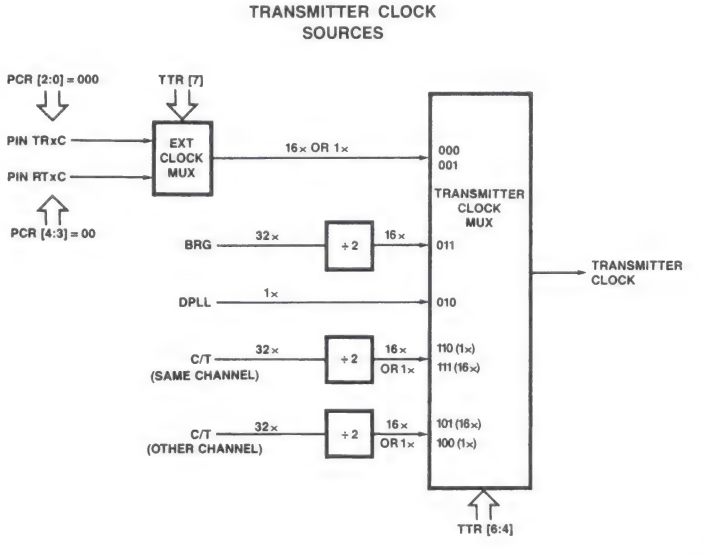



**Figure 8. Timing Block** (Continued)

## TRANSMITTER

### Transmitter TxFIFO and TxRDY

The transmitter accepts parallel data from the data bus and loads it into the TxFIFO, which consists of four 8-bit holding registers. This data is then moved to the Transmitter Shift Register (TxSR) which serializes the data according to the transmission format programmed. The TxSR is loaded from the TxFIFO, from special character logic, or from the CRC/LRC generator. The LSB is transmitted first, which requires right justification of characters by the CPU. TxRDY (GSR[5] or GSR[1]) and underrun (TRSR[7]) indicate the state of the TxFIFO. The TxFIFO may be addressed at any of four consecutive locations (see Table 1) to allow use of multiple byte work instructions. A write to any valid address always writes data to the next empty FIFO location.

TxRDY is set when the transmitter is enabled and there is an empty position in the TxFIFO (OMR[4] = 0) or when the TxFIFO becomes empty (OMR[4] = 1). The CPU may reset TxRDY through a status reset write cycle. If this is done, it will not be reasserted until a character is transferred to the TxST (OMR[4] = 0) or when the TxFIFO becomes empty again (OMR[4] = 1). The assertion of TxRDY, enabling of the IER [6] and the enabling of the channel master interrupt ICR[0] or [1] allow an interrupt to be generated.

If DMA operation is programmed, either RTxDRN (half-duplex) or TxDRQN (full-duplex) follows the state of TxRDY if the transmitter is enabled. These operations differ from normal ready in that the request signal is negated on the leading edge of the DMA acknowledge signal when the subsequent transfer causes the transmit FIFO to become full, while the TxRDY signal is negated only after the transfer is completed. Underrun status TRS[7] set indicates that one or more data character (not PAD characters) have been transmitted and the TxFIFO and TxSR are both empty.

In 'wait on Tx', a write to a full FIFO causes the write cycle to be extended until a FIFO position is available. DTACKN is asserted to acknowledge acceptance of the data. In non-wait modes, if an attempt is made to load data into a full TxFIFO, the TxFIFO data is preserved and the overrun data character(s) is lost. A normal DTACKN will be issued, and no indication of this occurrence is provided. The transmitter is enabled by the enable transmitter command. When the disable transmitter command is issued, the transmitter continues to operate until the TxFIFO becomes empty. The TxRDY does not become valid until the transmitter is enabled. Characters can be loaded into the FIFO while disabled. However, if the FIFO is full when the transmitter is enabled, TxRDY is not asserted.

### TxRTS Control

If TxRTS CONTROL, TPR[3], is programmed, the channel's RTS output is negated 5-bit times after the last bit (stop bit in ASYNC mode) of the last character is transmitted. RTS is normally asserted and negated by writing to OMR[0]. Setting of TPR[3] causes RTS to be reset automatically (if the transmitter is not enabled) after all characters in the transmitter FIFO (if any) are transmitted and five bit times after the 'last character' is shifted out. This feature can be used to automatically terminate the transmission of a message as follows:

- Program auto-reset mode: TPR[3] = 1.
- Enable transmitter.
- Assert RTSN: OMR[0] = 1.
- Send message.
- Disable transmitter after the last character is loaded into the TxFIFO.
- The last character will be transmitted and OMR[0] will be reset five bit times after the last bit, causing RTSN to be negated. The TxD output will remain in the marking state until the transmitter is enabled again.

The 'last bit' in ASYNC is simply the last stop bit of the character. In BOP and COP, the last character is defined either explicitly by either appending it with TEOM or implicitly through the selection of the frame underrun control sequence, TPR[7:6] (Transmitter Parameter Register). Table 13 summarizes the relationship of the selected underrun sequence and the protocol mode.

### Tx CTS Operation

If CTS enable Tx, TPR[2], is set, the CTSN input must be asserted for the transmitter to operate. Changes in CTSN while a character is being transmitted do not affect transmission of that character. However, if the CTS input becomes negated when TPR[2] is set and the transmitter is enabled and ready to start sending a new character, CTS underrun, TRSR[6], is asserted and the TxD output is placed in the marking (High) state. In ASYNC mode, operation resumes when CTSN is asserted again. In COP and BOP modes, the transmission of the message is terminated and operation of the transmitter will not resume until CTS is asserted and a TSOM or TSOMP command is invoked. Prior to issuing the command and retransmitting the message, the transmitter must be reset. After a change-of-state STS is established by the input sampling circuits (refer to the description of ICTSR[4], it is sampled by the Tx controller 1-1/2 bit times before each new character is serialized out of the Tx shift register. (This is 2-1/2 bits before the LSB of the new character appears on the TxD pin; there is an additional 1-bit delay in the transmitter data path due to the data encoding logic.)

### Tx Special Bit Pattern Transmission

The DUSCC provides features transmit special bit patterns (see Table 14).

The TxD pin is held marking after a hardware reset, a reset Tx command, when the transmitter is not enabled, and during underrun/idle, if this feature is selected through TPR[7:5]. The TxD pin is also held marking if the transmitter is enabled, and the TxFIFO is empty (ASYNC), or if a TSOM or TSOMP command has not been issued (SYNC modes).

The following command bits can be appended to characters in the TxFIFO: TEOM, TDLE, exclude from CRC, and reset TxCRC. An invoked command(s) is appended to the next character loaded into the TxFIFO and follows the character through the FIFO until that character is ready to be loaded into the TxSR. The transmitter for the various protocols.

### Tx ASYNC Mode

Serialization begins when the TxFIFO data is loaded into the TxSR. The transmitter first sends a start bit, then the programmed number of bits/character (TPR[1,0]), a parity bit (if specified), and the programmed number of stop bits. following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output goes to marking and the underrun condition (TRSSR[7]) is set.

Transmission resumes when the CPU loads a new character into the TxFIFO or issues a send break command. The send break command clears the TxFIFO and forces a continuous space (Low) on the TxD output after the character in TxSR (if any) is serialized. A send break acknowledge (TRSR[4]) is returned to the CPU to facilitate reassertion of the send break command in order to send an integral number of break characters. The send break condition is cleared when the reset Tx or disable Tx command is issued.

### Tx COP Modes

Transmitter commands associated with all COP modes are: transmit SOM (TSOM, transmit start of message), transmit SOM with PAD (TSOMP0, transmit EO (TEOM, transmit end of message), reset TxCRC, exclude from CTC, and transmit DLE.

A TSOM or send TSOMP command must be issued to start COP transmission. TSOM (without PAD) causes the TxCRC/LRC generator to be initialized and one or two SYN characters from S1R/S2R to be loaded into the TXSR and shifted out on the TxD output. A parity bit, if specified, is appended to each SYN character after the MSB. Send SOM acknowledge (TRSR[4]) is asserted when the SYN output begins. The user may reinvoke the command to

cause multiple SYNs to be transmitted. If the command is not reinvoked and the TxFIFO is empty, SYN patterns continue to be transmitted until the TxFIFO is loaded. If data is present in the FIFO, the first character is loaded into the TxSR and serialization of the data begins. Note that the TxFIFO may be preloaded with data before the TSOM is issued.

The TSOMP command causes all characters in the TxFIFO (PAD characters) to be loaded into the TxSR and serialized if the Tx is enabled. Unlike the transmit SOM without PAD command, data (non-PAD characters) cannot be preloaded into the TxFIFO. While the PAD is transmitted, parity is disabled and character length is automatically set to 8 bits regardless of the value in TPR[1:0]. When the TxFIFO becomes empty after the PAD, the TxCRC/LRC generator is initialized, the SYN character(s) are transmitted with optional parity appended, and send SOM acknowledge asserted. Operation then proceeds in the same manner as the TSOM command; the user has the option to invoke the TSOM command to cause multiple SYNs to be transmitted.

After the TSOM/TSOMP command is executed, characters in the TxFIFO are loaded into the TxSR and shifted out with a parity bit, if specified, appended after the MSB. If, after the opening SYN(s) and at least one data has been transmitted, the TxFIFO is empty, a data underrun condition results and TRSR[7] is asserted. The transmitter's action on data underrun is determined by TPR[7:6] and the COP protocol. If TRP[7:6] = '10', the transmitter line fills with MARK characters until a character is loaded into the FIFO. I TRP[7:6] and the COP protocol. If TPR[7:6] = '11' is selected, the transmitter line fills with SYN, SYN1-SYN2, or DLE-SYN1 for monosync, dual sync, and BISYNC transparent modes, respectively. If TPR[7:6] = '00', the BCC characters are transmitted and frame complete (TRSR[6]) is set. TxD then assumes the programmed idle state (TPR[5]) of MARKs or SYN1/SYN1-SYN2.

Operation resumes with the transmission of a SYN sequence when a TSOM command is invoked. A TSOMP command is ignored unless the transmitter is disabled and then reenabled.

An appended TEOM command also terminates the frame as described above. It occurs after transmission of the character to which the TEOM is appended. The TEOM command can be explicitly asserted through the channel command register. If TPR[4] = '1', the TEOM is automatically appended to a character in DMA mode, if the DONEN input is asserted when that character is loaded into the TxFIFO, or if the counter/timer is counting transmitted characters when the character which causes the counter to reach zero count is loaded.

The TDLE command when appended to a character in the TxFIFO, causes the DLE character to be loaded into the the TxSR and serialized before the TxFIFO character is loaded into the TxSR and serialized. This feature is particularly useful for BISYNC operation. The DLE character will be excluded from the CRC accumulation in BISYNC transparent mode (see below), but will be included in all other COP modes.

In BISYNC mode, transmission of a DLE-STX character sequence (either via a send TDLE command appended to the STX character, or via DLE and STX loaded into the TxFIFO) puts the transmitter into the transparent test mode of operation. In this mode, normally restricted character sequences can be transmitted as 'normal' bit sequences. The switch occurs after transmission of the two characters, so that the DLE and STX are included in the BCC accumulation. If the DLE-STX is to be excluded from the CRC, the user should issue a 'reset CRC' command prior to loading the next character.

Another method of excluding the two characters from the CRC is to invoke the 'exclude from CRC' command prior to loading the character(s) into the FIFO. While in transparent mode, the transmitted line fills with DLE-SYN1 and automatically transmits an extra DLE if it finds a DLE in the TxFIFO ('DLE stuffing'). The transmitter reverts to non-transparent mode when the frame complete status is set in TRSR[5].

CRC/LRC accumulation can be specified in all COP modes; the type of CRC is specified via CMR2[2:0]. The TSOM/TSOMP commands set the CRC/LRC accumulator to its initial state and accumulation begins with the first non-SYN character after the initial SYN(s) are transmitted. PAD characters are not subject to CRC accumulation. In non-BISYNC or BISYNC normal modes, all transmitted characters except linefill characters (SYNs or MARKs) are subject to accumulation. In BISYNC transparent mode, odd (stuffed) DLEs and the DLE-SYN1 linefill are excluded from the accumulation. Characters can be selectively excluded from the accumulation by invoking the 'exclude form CRC' command prior to loading the character into the FIFO.

Accumulation stops when transmission of the first character of the BCC begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command. The CRC generator is also automatically initialized after the EOM is sent.

**Table 13. Abort Sequence — Protocol Mode**

| TPRA[7:6] | PROTOCOL | LAST CHARACTER |
|---|---|---|
| 00 | BOP | FLAG following either FCS (if selected) or last data character |
| | COP | Last byte of FCS before line begins SYN or MARKing |
| 10 | BOP | Abort sequence (11111111) prior to MARKing |
| | COP | Last byte of FCS before line begins SYN or MARKing |
| 11 | BOP | Abort sequence (11111111) prior to FLAG |
| | COP | First SYN of SYN sequence |

**Table 14. Special Bit Patterns**

| PROTOCOL | BIT PATTERN |
|---|---|
| ASYNC-BREAK | An all 0's character including parity bit (if specified) and stop bits. Used for send break command. |
| COP-SYN | Contained in S1R (single SYN mode) or in S1R/S2R (dual SYN modes). Used for TSOM and TSOMP commands and for non-transparent mode linefill and IDLE. |
| COP-DLE | Used for TDLE command and for BISYNC transparent mode linefill and to generate BISYNC control sequences. |
| COP-CRC | 16/8 bits from the CRC/LRC accumulator used for TEOM command or for auto-EOM modes. |
| BOP-FLAG | 01111110. Used for TSOM, TSOMP, and TEOM commands, for auto-EOM modes, and as an IDLE line fill. |
| BOP-ABORT | 11111111. Used for send ABORT command or during TxFIFO underrun. |
| BOP-CRC | 16 bits from the CRC accumulator used for TEOM command or for auto-EOM modes. |
| BOP/COP MARK | All 1's pattern on data line. |

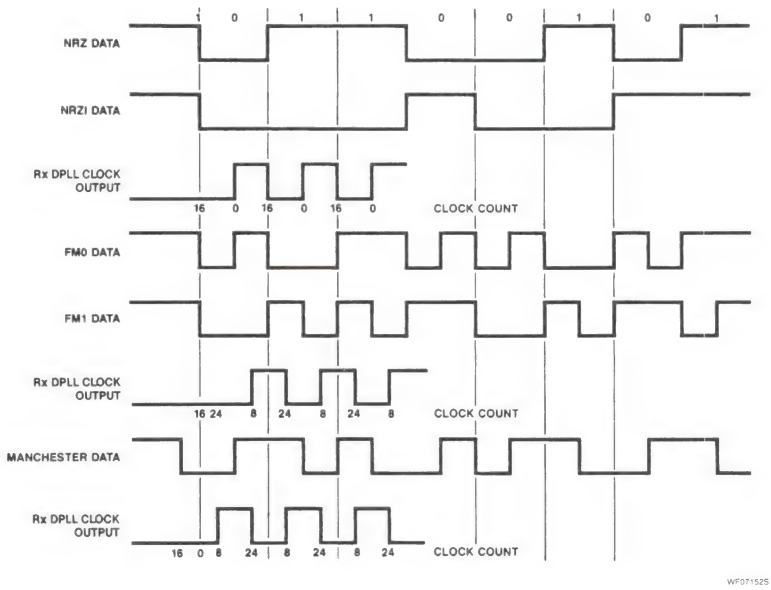



Figure 9. DPLL Waveforms

**TxBOP Modes**

Transmitter commands associated with BOP modes are TSOM, TSOMP, TEOM, and transmit ABORT (TABRK). The TSOM and TSOMP commands are identical to COP modes except that a FLAG character (01111110) is used as the start of message sequence instead of the SYNs, and FLAG(s) that continue to be sent until the TxFIFO is loaded. There is no zero insertion (see below) during transmission of the PAD characters, and they are not preceded by a FLAG or accumulated in the CRC. Character length is automatically set to 8 bits regardless of TPR[1:0].

The first characters loaded into the TxSR from the TxFIFO are the address and control fields, which have fixed character lengths of eight bits. The number of address field bytes is determined by CMR1[4:3]. If extended address field is specified, the field is terminated if the first address octet is H'00' or if the LSB of the octet is a 1. The number of control field bytes is selected by CMR1[5]. If any information field characters follow the control field (forming an I field), they are transmitted with the number of bits per character programmed in TPR[1:0]. The TEOM command can be appended to the last character whether explicitly or automatically as described for COP mode. When the character with the appended TEOM is loaded from the TxFIFO, it is transmitted with the character length specified by OMR[7:5]. In this way, a residual character of 1 - 8 bits is transmitted without requiring the CPU to change the Tx character length for this last character.

After opening the FLAG and first address octet have been transmitted, an underrun occurs (TRSR[7] = 1) if the TxFIFO is empty when the transmitter requires a new character. The underrun control bits (TPR[7:6]) determine whether the transmitter line fills with either ABORT-MARKs, ABORT-FLAGs (see below), or ends transmission with the 'normal' end of message sequence.

EOM on underrun is functionally similar to EOM due to an appended TEOM command. If the EOM is due to underrun, the normal character length applies to the last data character. After the last character is transmitted, the FCS (inverted CRC) and closing FLAG are sent, frame complete (TRSR[5]) is set, and the TxCRC is initialized. If the TxFIFO is empty after the closing FLAG has been sent, TXD will assume the programmed idle state of FLAGs or MARKs (TPR[5]) and wait for a character to be loaded into the FIFO or for a TSOM command to be issued. If the TXFIFO is not empty at that time, the TxFIFO data will be loaded into the TxSR and serialized. In that case, the closing FLAG is the opening FLAG of the next frame.

The user can control the number of FLAGs between frames by invoking the TSOM command after frame complete is asserted. The DUSCC then operates in the same manner as for transmission of multiple FLAGs at the beginning of a frame. When the command is no longer reinvoked, transmission of the TxFIFO data will begin. If the FIFO is empty, FLAGs continue to be transmitted.

The DUSCC provides automatic zero insertion in the data stream to prevent erroneous transmission of the FLAG sequence. All data characters loaded into the TxSR from the TxFIFO and characters transmitted from the CRC generator are subject to zero insertion. For this feature a zero is inserted in the serial data stream each time five consecutive ones (regardless of character boundaries) have been transmitted.

A send ABORT command clears the TxFIFO and inserts an ABORT character of eight ones (not subject to zero insertion) into the TxSR for transmission after the current character has been serialized. A send abort ack (TRSR[4]) facilitates reassertion of send abort by the user to guarantee transmission of multiple abort characters. This feature can be used to send the 15-ones idle sequence.

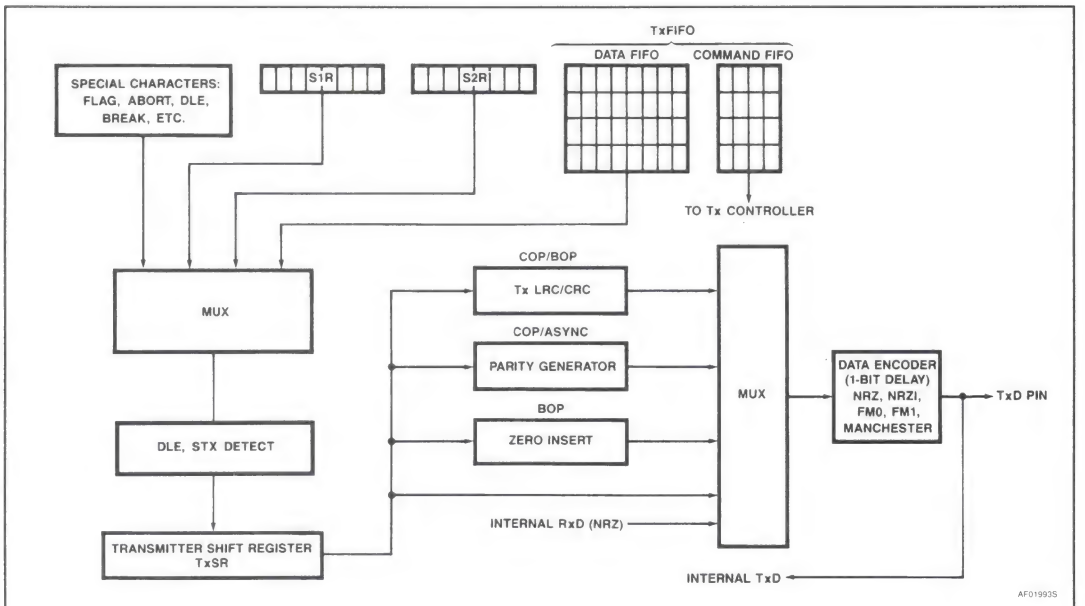



**Figure 10. Transmitter Data Path**

The transmitter sends either marks or FLAGs after the abort character(s) has been transmitted, depending on TPR[7:6]. Operation resumes with the transmission of a FLAG when a TSOM command is invoked. A TSOMP command is ignored unless the transmitter is disabled and then reenabled.

CRC accumulation can be specified in all BP modes. The type of CRC is specified via CMR2[2:0], and is normally selected as CRC-CCITT preset to ones, although any option is valid. Note that LRC8 option is not allowed in BOP modes.

The TSOM/TSOMP command sets the CRC accumulator to its initial state and accumulation begins with the first address octet after the initial FLAG(s). Accumulation stops when transmission of the first character of the FCS begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command and can exclude any character from the accumulation by use of the exclude from CRC command, but these features would not normally be used in BOP modes. The CRC generator is also automatically initialized after the EOM or an ABORT are sent.

**TxBOP Loop Mode**

The loop modes are used by secondary stations on the loop, while the primary station operates in the BOP primary mode. Both the transmitter and receiver must be enabled and should be programmed to use the same clock source. Loop operation is initiated by issuing the 'go on-loop' command. The receiver looks for the receipt of seven contiguous ones and then asserts the LCN output to cause external loop control hardware to put the DUSCC into the loop, with the TxD output echoing the RxD input with a 2-bit time delay. The echoing process continues until a Go Active on Poll (GAP) command is invoked. The DUSCC then looks for receipt of an EOP bit pattern (a zero followed by seven ones, 11111110) and changes the last one of the EOP into a zero making it an opening FLAG. Loop sending (TRSR[6]) is asserted at that same time. The action of the transmitter after sending the initial FLAG depends on the status of the transmit FIFO.

If the transmit FIFO is not empty, a normal frame transmission begins. The operation is then similar to normal BOP operation with the following differences:

1. An ABORT command, an underrun, or receipt of the turnaround sequence (H'00') or FLAG cause the transmitter to cease operation and to revert to echoing the RxD input with a 2-bit time delay. A new transmission cannot begin until the GAP command is reinvoked and a new EOP sequence is received.
2. Subsequent to sending the EOM sequence of FCS-FLAG, the DUSCC examines the internal GAP flip-flop. If it is not set (having been reset by the 'reset GAP' command, the DUSCC reverts to echoing the received data. If the internal GAP flip-flop is still set, transmission of a new frame begins, with the user having control of sending multiple FLAGs between frames by use of the 'send SOM' command. If the FIFO is empty at this time, the DUSCC continues to send FLAGs until the data is loaded into the FIFO or until GAP is reset. If the latter occurs, it reverts to echoing RxD.

   When the DUSCC reverts to echoing RxD in any of the above cases, the last transmitted zero and seven ones will form an EOP for the next station down the loop.

   If the TxFIFO is empty when the EOP is recognized, the transmitter continues to send FLAGs until there is data in the FIFO. If a turnaround sequence or the reset GAP command is received before the FIFO is loaded, the transmitter switches to echoing RxD without any data transmission. Otherwise a frame transmission begins as above when a character is loaded into the FIFO. The mechanism provides time for the CPU to examine the received frame (the frame preceding the EOP) to determine if it should respond or not, while holding its option to initiate a transmission.

Termination of operation in the loop mode should be accomplished by use of the 'go off-loop' command. When the command is invoked, the DUSCC looks for the receipt of eight contiguous ones. It then negates the LCN output to cause the external loop control hardware to remove the DUSCC from the loop without affecting operation of other units remaining on the loop.

## RECEIVER

The receiver data path includes two 9-bit holding registers, HSRH and HSRL, an 8-bit character comparison register, CCSR, two synchronizing flip-flops, a receiver shift register, RxST, the programmable SYN comparison registers, S1R and S2R, and BISYNC character comparison logic. The DUSCC configures the circuitry and utilizes it according to the operational mode selected for the channel through the two mode registers CMR1 and CMR2. For all data paths, character data is assembled according to the character bit count, in the RxSR, and is moved to the RxFIFO with any appended statuses when assembly is completed. Figure 1 depicts the four data paths created in the DUSCC for the previous protocols.

**Receiver RxFIFO, RxRDY**

The receiver converts received serial data on RxD (LSB first) into parallel data according to the transmission format programmed. Data is shifted through a synchronizing flip-flop and one or more shift registers, the last of which is the 8-bit receiver shift register (RxST). Bits are shifted into the RxSR on the rising edge of each 1X receive clock until the LSB is in RxSR[0]. Hence, the received character is right justified, with all unused bits in the RxSR cleared to zero. A receive character length counter generates a character boundary signal for synchronization of character assembly, character comparisons, break detection (ASYNC), and RxSR to RxFIFO transfers (except for BOP residual characters). During COP and BOP hunt phases, the SYN/GLAG comparison is made each receive bit time, as abort, and idle comparisons in BOP modes.

An internal clock from the BRG, the DPLL or the counter/timer, or an external 1X or 16X clock may be used as the receiver clock in ASYNC mode. The BRG or counter/timer cannot be used directly for the receiver clock in synchronous modes, since these modes require a 1X receive clock that is in phase with the received data. This clock may come externally from the RTxC or TRxC pins, or it may be derived internally from the DPLL. Received data is internally converted to NRZ format for the receiver circuits by using clock pulses generated by the DPLL.

When a complete character has been assembled in the RxSR, it is loaded into the receive FIFO with appended status bits. The most significant data bits of the character are set to zero if the character length is less than eight bits. In ASYNC and COP modes the user may select, via RPR[3], whether the data transferred to the FIFO includes the received parity bit or not. The receiver indicates to the CPU or DMA controller that it has data in the FIFO by asserting the channel's RxRDY status bit (GSR[4] or GSR[0] and, if in DMA mode, the corresponding receiver DMA request pin.

The RxFIFO consists of four 8-bit holding registers with appended status bits for character count complete indications (all modes), character compare indication (ASYNC), EOM indication (BISYNC/BOP), and parity, framing, and CRC errors. Data is loaded into the RxFIFO from the RxSR and extracted (read) by the CPU or DMA controller via the data bus. AN RxFIFO read create an empty RxFIFO position for new data from the RxSR.

RxRDY assertion depends on the state of OMR[3]:

1. If OMR[3] is 0 (FIFO not empty), RxRDY is asserted each time a character is transferred form the receive shift register to the receive FIFO. If it is not reset by the CPU, RxRDY remains asserted until the receive FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated, regardless of the current state of the receive FIFO, until a new character is transferred from the RxSR to the RxFIFO.
2. If OMR[3] is 1 (FIFO full), RxRDY is asserted:

a. When a character transfer from the receive shift register to the receive FIFO causes it to become full.

b. When a character with a tagged EOM status bit is loaded into the FIFO (BISYNC or BOP) regardless of RxFIFO full condition.

c. When the counter/timer is programmed to count received characters and the character which causes it to reach zero count is loaded into the FIFO (ICTSR[6]).

d. When the beginning of break is detected in ASYNC mode regardless of the RxFIFO full condition.

If it is not reset by the CPU, RxRDY remains asserted until the FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated regardless of the current state of the receive FIFO, until it is asserted again due to one of the above conditions.

The assertion of RxRDY causes an interrupt to be generated if IER[4] and the channel's master interrupt enable (ICR[0] or ICR[1]) are asserted.

When DMA operation is programmed, the RxRDY status bit is routed to the DMA control circuitry for use as the channel receiver DMA request. Assertion of RxRDY results in assertion of RTxDRQN output.

Several status bits are appended to each character in the RxFIFO. When the FIFO is read, causing it to be 'popped', the status bits associated with the new character at the top of the RxFIFO are logically ORed into the RSR. Therefore, the user should read RSR before reading the RxFIFO in response to RxRDY activation. If character-by character status is desired, the RSR should be read and cleared each time a new character is received. The user may elect to accumulate status over several characters or over a frame by clearing RSR at appropriate times. This mode would normally also be used when operating in DMA mode. If the RxFIFO is empty when a read is attempted, and wait mode as specified in CMR2[5:3], is not being used, a H'FF' is output on the data bus.

In all modes, the DUSCC protects the contents of the FIFO and the RxSR from overrun. If a character is received while in FIFO is full and a character is already in the RxSR waiting to be transferred into the FIFO, the overrunning character is discarded and the OVERRUN status bit (RSR[5]) is asserted. If the overruning character is an end-of-message character, the character is lost but the FIFOed EOM status bit will be asserted when the character in the RxSR is loaded into the FIFO.

Operation of the receiver is controlled by the enable receiver command. When this command is issued, the DUSCC goes into the search for start bit state (ASYNC), search for SYN state (COP modes), or search for FLAG state (BOP modes). When the disable receiver command is issued, the receiver ceases operation immediately. The RxFIFO is cleared on master reset, or by a rest receiver command. However, disabling the receiver does not affect the RxFIFO, RxRDY, or DMA request operation.

**Receiver DCD and RTS Controls**

If DCD enable Rx, RPR[2], is asserted, the DCD input must be asserted and the sampling circuit detects that the DCD input has been negated, the receiver ceases operation immediately. Operation resumes when the sampled DCD is asserted again. A change of state detector is provided on the DCD input of each channel. The required duration of the DCD level change is described in the discussion of ICTSR[5]. The user may program a change of state to cause an interrupt to be generated (master interrupt enable ICR[0] or [1] and IER[7] must be set) so that appropriate action can be taken.

In ASYNC mode, RPR[4] can be programmed to control the deactivation of the RTSN output by the receiver. RTSN can be manually asserted and negated by writing to OMR[0]. However, the assertion of RPR[4] causes RTS to be negated automatically upon receipt of a valid start bit if the channel's receive FIFO is already full. When this occurs, the RTSN negated status bit, RSR[6], is set. This may be used as a flow control feature to prevent overrun in the receiver by using the RTSN output signal to control the CTSN input of the remote transmitter. The new character will be assembled in the RxSR, but its transfer to the FIFO will be delayed until the CPU reads the FIFO, making the FIFO position available for the new character.

Once enabled, receiver operation depends on channel protocol mode. The following describes the receiver operation for the various protocols.

**RxASYNC Mode**

When first enabled, the receiver goes into the search for start bit state, looking for a High-to-Low (mark-to-space) transition of the start bit on the RxD input. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 71/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again.

If RxD is still Low, a valid start bit assumed and the receiver continues to sample the input at one bit time intervals (16 periods of the 16X Rx clock; one period of the 1X Rx clock) at the theoretical center of the bit, until the proper number of data bits and the parity bit (if specified) have been assembled, and the first stop bit has been detected.

The assembled character is then transferred to the RxFIFO with appended parity error (if parity is specified) and framing error status bits. The DUSCC can be programmed to compare this character to the contents of S1R. The appended character compare status bit, RSR[7], is set if the data matches and there is no parity error.

After the stop bit is sampled, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e., framing error) and RxD remains Low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

If a break condition is detected (RxD Low for entire character time including optional parity and first stop bit), only one character consisting of all zeros will be loaded into the RxFIFO and break start detect, RSR[2], will be set. The RxD input must return to a High condition for at least one half of a bit time (16X clock mode) or for one bit time (1X clock mode) before the break condition is terminated and the search for the next start bit begins. At that time, the break end detect condition, RSR[3], is set. Note that the maximum speed in the receiver when in asynchronous mode must not exceed 2Mbs.

**Rx COP Modes**

When the receiver is enabled in COP modes, it first goes into the SYN hunt phase, testing the received data each bit time for receipt of the appropriate SYN bit pattern, Plus parity if specified, to establish character boundaries. Receipt of the SYN bit pattern terminates hunt phase and places the receive in the data phase, in which all leading SYNs are stripped and the RxFIFO begins to load starting with the first non-SYN character. In COP single SYN protocol mode, S1R contains the SYN character required to establish character synchronization. In COP dual SYN and BISYNC protocol modes, S1R and S2R contain the first and second SYN characters, respectively, required to

establish character synchronization. The SYN character length is the same as the character length programmed in RPR[1:0], plus the parity bit if parity is specified. SYN characters received with a parity error, when parity is specified, are considered invalid and will not cause synchronization to be achieved.

In COP mode, resetting the receiver clears the receiver data path, while disabling the receiver does not. If not reset, partial sync patterns remaining in the receiver will be recognized when it is enabled.

If external synchronization is programmed (RPR[4] = 1), the internal SYN detection and special character recognition logic are disabled and receipt of SYN characters is not required. A pulse on the SYNI input pin will establish character synchronization and terminate hunt phase. The SYNI pin is ignored after the first input on the SYNIN pin is received. The receiver must be disabled and then reenabled to resynchronize or to return to normal mode. This must be programmed in conjunction with CMR1[2:0] = 110. Refer to the description of RPR[4] for further details

The SYN detect status bit RSR[2], is set whenever SYN1, SYN1-SYN2, or DLE-SYN1 is detected for single SYN, dual SYN/BISYNC normal, and BISYNC transparent modes, respectively, and the SYNOUT pin will go active for one receive clock period one bit time after SYN detection in HSRH/HSRL. After character sync has been attained, the receiver enters the data phase and assembles characters in the RxSR, beginning with the first non-SYN character, with the least significant bit received first. It computes the BCC if specified, checks parity if specified, and checks for overrun errors.

The operation of the BCC (CRC/LRC) logic depends on the particular COP mode in use. The BCC is initialized upon first entering the data phase. For non-BISYNC modes, all received characters after entering data phase are included in the BCC computation, except for leading SYNs and SYNs which are specified to be stripped by RPR[7]. As each received character is transferred from the RxSR to the FIFO, the current value of the BCC characters is checked and the CRC ERROR status bit (RSR[1]) is set if the value of the CRC remainder is not the expected value. RSR[1] gets set when the character reaches the top of the FIFO. The EOM status bit, RSR[7], is not set since there is no defined end-of-message character. The receiver computes the BCC for test messages automatically when operating in BISYNC protocol mode.

## BISYNC Features

The DUSCC provides support for both BISYNC normal and transparent operations. The following summarizes the features provided. Both EBCDIC and ASCII text messages can be handled by the DUSCC as selected by CMR1[5]. The receiver has the capability of recognizing special characters for the BISYNC protocol mode (see Table 15).

All sequences in Table 15, except SOH and STX, when detected explicitly cause a status to be affected. The following describes the conditions when this occurs.

The first character received when entering data phase for a header or text message should be an SOH, an STX, or a DLE-STX two-character sequence. Receipt of any of these initializes the CRC generator and starts the CRC accumulation. The SOH places the receiver in header mode, receipt of the STX places it in text mode, the receipt of the DLE-STX sequence (at any time) automatically places the receiver in transparent mode and sets the XPNT mode status bit, TRSR[0]. There is no explicit status associated with SOH and STX. If any characters are received when entering the data phase, the message is treated as a control message and will not be accumulated in CRC.

After the data phase is established, the receiver searches the data stream for an end of message control character(s):

Header field: ENQ, ETB, or ITB

Normal text field: ENQ, ETX, ETB, or ITB

Transparent text field: DLE-ENQ, DLE-ETX, DLE-ETB, or DLE-ITB

Control message field: EOT, NAK, ACK0, ACK1, WACK, RVI or TTD

Detection of any one of these sequences causes the EOM status bit, RSR[7], to be set. Also if RPR[5] is set and the receiver does not detect a closing PAD (four 1's) after the 'EOT' or 'NAK', the PAD error status bit, RSR[6], is set. When the abort sequence ENQ or DLE-ENQ is detected, the character is tagged with an EOM status and transferred to the FIFO, but the appended CRC error status bit should be ignored. For the other EOM control sequences, the receiver waits for the next two bytes (the CRC bytes) to be received, checks the value of the CRC generator, and tags the transferred character with a CRC error, RSR[1], if the CRC remainder is not correct. See Figure 11 for an example of BCC accumulation in various BISYNC messages.

The CRC bytes are normally not transferred to the FIFO, unless the transfer FCS to FIFO control bit, RPR[6], is asserted. In this case the EOM and CRC error status bits will be tagged onto the last byte of the last FCS byte instead of to the last character of the message. After detecting one of the End-Of-Message (EOM) character sequences and setting RSR[7], the receiver automatically goes into auto hunt mode for the SYNC characters and PAD check if RPR[5] is set.

## SYN Pattern Stripping

Leading SYNs (before a message) are always stripped and excluded from the FCS, but SYN patterns within a message are treated by the receiver according to the RPR[7] bit. SYN character patterns are defined for the various COP modes as follows:

COP single SYN mode — SYN1

COP dual SYN mode — SYN1, and SYN2 when immediately preceded by SYN1.

BISYNC normal mode — SYN1, and SYN2 when immediately preceded by SYN1. SYN1 is always stripped, even if it is not followed by SYN2 when stripping is selected.

BISYNC transparent mode — DLE-SYN1, where the DLE is the last of an odd number of consecutive DLEs.

0 Strip only RPR[7] leading the SYN and do not accumulate in FCS.

1 Strip all SYNs. Additionally, strip odd DLEs when operating in BISYNC transparent mode. Do not accumulate stripped characters in FCS.

Processing of the SYN patterns is determined by the RPR[7] bit, the COP mode, and the position of the pattern in the frame. This is summarized in Table 16.

The value of the RPR[7] field does not affect the setting of the SYN DETECT status bit, RSR[2], and the generation of a SYNOUT pulse when a SYN pattern is received.

## RxBOP Mode

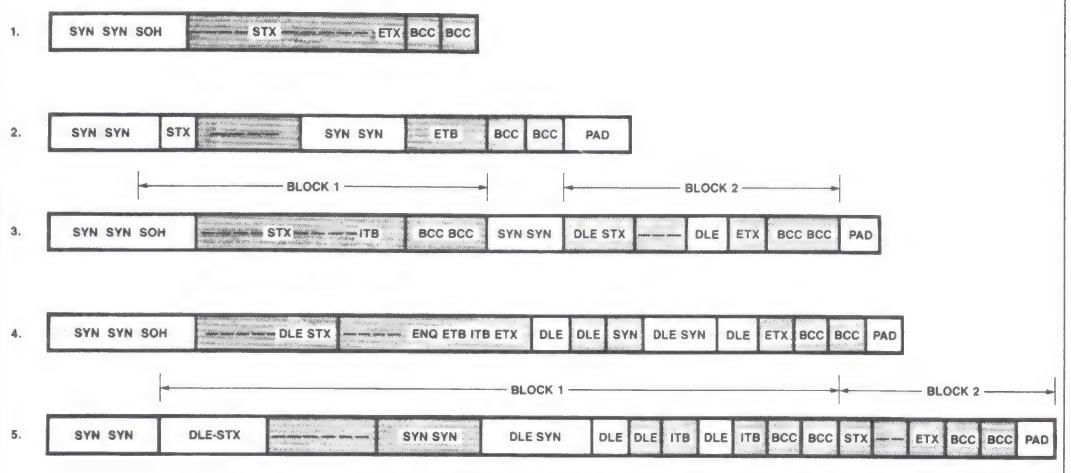
In BOP protocol mode, the receiver may be in any one of four phases: hunt phase, address field (A) phase, control field (C) phase, or information field (I) phase. The character length for the A and C phases is always 8 bits. The I field character length is specified in RPR[1:0].

Note that if the residual character length is not zero, the unused most significant bits in the receiver FIFO are not necessarily zero. the unused bits should be ignored, this will not cause a CRC error.

After an enable receiver command is executed, the receiver enters hunt phase, in which a comparison for the string (01111110) is done every Rx bit time. The FLAG delineates the beginning (and end) of a received frame and establishes the character boundary. Each FLAG match in CCSR causes the FLAG detect status bit (RSR[2]) to be set and SYNOUTN pin to be activated one bit time later for one receive clock period. FLAGs with an overlapping zero will be detected. All FLAGs are deleted from the data stream.

## Table 15. BISYNC Features

| BISYNC — Single-Character Sequences | | | |
|---|---|---|---|
| **Sequences** | **ASCII** | **EBCDIC** | **Description** |
| SOH | H'01' | H'01' | Start of header |
| STX | H'02' | H'02' | Start of text |
| ETX | H'83' | H'03' | End of text |
| EOT | H'04' | H'37' | End of transmission |
| ENQ | H'85' | H'2D' | Enquiry |
| DLE | H'10' | H'10' | Data link escape |
| NAK | H'15' | H'3D' | Negative ack |
| ETB | H'97' | H'26' | End of transmission block |
| ITB | H'1F' | H'1F' | End of intermediate transmission block |
| **BISYNC — Two-Character Sequences** | | | |
| **Sequence** | **ASCII** | **EBCDIC** | **Description** |
| ACK0 | H'10,B0' | H'10,70' | Acknowledge 0 |
| ACK1 | H'10,31' | H'10,61' | Acknowledge 1 |
| WACK | H'10,3B' | H'10,6B' | Wait before transmit positive ack |
| RVI | H'10,BC' | H'10,7C' | Reverse interrupt |
| TTD | H'02,85' | H'02,2D' | Temporary text delay |
| **BISYNC — (Transparent Text Mode) — Two-Character Sequences** | | | |
| **Sequence** | **ASCII** | **EBCDIC** | **Description** |
| DLE-ENQ | H'10,85' | H'10,2D' | Enquiry |
| DLE-ITB | H'10,1F' | H'10,1F' | End of intermediate transmission block |
| DLE-ETB | H'10,97' | H'10,26' | End of transmission block |
| DLE-ETX | H'10,83' | H'10,03' | End of text |
| DLE-STX | H'10,02' | H'10,02' | Start of transparent text mode |




**NOTES:**
The BCC accumulator is stopped after the end of message character sequence is accumulated. All shaded areas are accumulated.
ENQ (DLE - ENQ) in a text message should be treated as an abort.
Opening SYNs will be stripped by the receiver.

**Figure 11. Example of BCC Accumulation in Various BISYNC Messages**

**Table 16. SYN Pattern Processing**

| MODE | RPR [7] | LEADING SYNs | WITHIN A MESSAGE |
|---|---|---|---|
| BISYNC | 0 | no FCS<br>no FIFO | no FCS<br>Pattern into FIFO |
| | 1 | no FCS<br>no FIFO | no FCS<br>no FIFO |
| COP | 0 | no FCS<br>no FIFO | Accumulate in FCS<br>Pattern into FIFO |
| | 1 | no FCS<br>no FIFO | no FCS<br>no FIFO |

Once a FLAG has been detected, the receiver will exit hunt phase and enter address phase. The handling of the address field is determined by the values programmed in CMR1[2:0], which selects one of the BOP modes. The BOP secondary address modes are selected by CMR1[4:3] and function as in the description that follows.

**Single-Octet Address**

For receive, the address comparison for a secondary station is made on the first octet following the opening FLAG. A match occurs if the first octet after the FLAG matches occurs if the first octet after the FLAG matches the contents of S1R, or if all parties address (RPR[3]) is asserted and the first octet is equal to H'FF'.

**Dual Octet Address**

For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG.

A match occurs if the first two octets after the FLAG match the contents of S1R and S2R respectively, or if all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF, FF'.

**Dual Address with Group Mode**

For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG. A match occurs for one of three possible conditions. If the first two octets after the FLAG match the contents of S1R and S2R, respectively, or if the first octet is H'FF' and the second matches the contents of S2R (group mode), or when all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF,FF'. The second condition (group mode) allows a selected group of stations to receive a message.

**Extended Address Mode**

Extend address field to the next octet if the LSB of the current address octet is zero. Address field is terminated if the LSB of the address is a one. The address field will be terminated after the first octet if the null address H'00' is received/transmitted as the first address octet. For this mode the receiver does not perform an address comparison (all received characters after the opening FLAG are transferred to the FIFO) but does determine when the address field is terminated.

The length of the A field may be a single octet, a dual octet, or more octets, as described above. A primary station or an extended address secondary station does not perform an address comparison, and all characters in the A, C, and I fields after the flag are transferred to the FIFO. Although address field comparisons are not performed, the length of the address field is still determined by CMR1[4:3]. For the other secondary address modes, if there is a match, or the received character(s) match either of the other enabling conditions (group or all-parties address), all characters in the A, C, and I field are transferred to the FIFO. If there is no match, the receiver returns to the FLAG hunt phase.

C phase begins after A phase is terminated. The receiver receives one or two control characters, CMR1[5]. After this phase is terminated, the character length is switched automatically from 8 bits to the number of bits specified in RPR[1:0] and the information field phase is entered.

The frame is terminated when a closing FLAG is detected. The same FLAG can also serve as the opening FLAG of the next frame. The 16 bits received prior to the closing FLAG form the frame check sequence (if an FCS is specified in CMR2[2:0]). All non-FLAG characters of the frame are accumulated in the CRC checker and the result is compared to the expected remainder. Failure to match will cause a CRC error. EOM detect RSR[7], RCL not zero RSR[0], and CRC error RSR[1] are normally FIFOed with the last character of the I field. RCL not zero RSR[0] is set if the length of the last character of the I field does not have the length programmed in RPR[1:0]. The residual character length in TRSR[2:0] is also valid at that time. The CRC characters themselves are normally not passed to the RxFIFO. However, if the transfer FCS to FIFO control bit RPR[6] is asserted, the FCS bytes will be transferred to the FIFO. In this case the EOM, CRC error, and RCL not zero status bits will be tagged onto the last byte of the CRC sequence instead of to the last character of the message.

If the closing FLAG is received prior to receipt of the appropriate number of A field, C field as programmed in CMR1[5:3], and FCS field octets, a short frame will be detected and RSR[4] will be set. The I field need not be present in a valid frame. An abort (11111110) comparison is done after an opening FLAG has been received and up to receipt of the closing FLAG. A match causes the abort detect status bit (RSR[6]) to be set. The receiver then enters FLAG search mode. The abort is stripped from the received data stream.

If a zero followed by 15 contiguous ones is detected, the idle detect status bit RSR[3] is set. This comparison is done whenever the receiver is enabled. Therefore, it can occur before or after a received frame.

Zero deletion is performed during BOP receive. A zero after 5 contiguous ones is deleted from the data stream regardless of character boundaries. Deleted zeros are not subject to CRC accumulation. FLAG, ABORT, and IDLE comparisons are done prior to zero deletion.

If external synchronization is programmed (RPR[4] - 1), the internal FLAG detection and address comparison logic is disabled and receipt of FLAGs is not required. In this arrangement, a pulse on the SYNI-N input pin will establish synchronization and terminate hunt phase. The receiver will then go immediately into the I-field mode with zero deletion disabled, assembling and transferring characters into the FIFO with the character length specified in RPR[1:)]. The SYNI-N pin is ignored after the first input on the SYNI-N pin is received. The receiver must be disabled and then reenabled to resynchronize or to return to normal operating mode.

This mode must be programmed in conjunction with CMR1[2:0] = 110. Refer to the description of RPR[4] for further details.

**BOP Loop Mode**

Operation of the receiver in BOP loop protocol mode is similar to operation in other BOP modes, except that only certain frame formats are supported. Several character detection functions that interact with the operation of the transmitter commands are added:

1. When the 'go on-loop' command is invoked, the receiver looks for the receipt of a zero followed by seven ones and then asserts the LCN output.
2. When the 'go off-loop' command is invoked, the receiver looks for the receipt of eight contiguous ones and then negates the LCN output.
3. The TxD output normally echoes the receive input with a two bit time delay. When the 'go active on poll' command is asserted, the receiver looks for an EOP (a zero followed by seven ones) and then switches the TxD output line to the normal transmitter output. Receipt of an EOP or an ABORT sets RSR[6].
4. Receipt of a turnaround sequence (eight contiguous zeros) terminates the transmitter operation, if any, and returns the TxD output to echoing the RxD input. RSR[3] is set if a turnaround is received.

See transmitter operation for additional details.

## SUMMARY OF COP FEATURES

| | |
|---|---|
| **COP Dual SYN Mode** | |
| SYN detect | SYN1-SYN2 |
| Linefill | SYN1-SYN2 |
| SYN stripping | SYN1-SYN2 used to establish character sync, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1-SYN2 if stripping is specified by RPR[7]. |
| Excluded form FCS** | SYN1 and SYN1-SYN2 before beginning of message, i.e., leading SYNs and, if SYN stripping is specified by RPR[7] anywhere else in the message for the Rx; linefill SYN1-SYN2 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.) |
| **BISYNC normal mode** | |
| SYN detect | SYN1-SYN2 |
| Linefill | FYN1-SYN2 |
| SYN stripping | SYN1-SYN2 used to establish character sync, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1-SYN2 if stripping is specified by RPR[7]. |
| Excluded from FCS | All SYNs either before or within a message, regardless of RPR[7], plus additional characters as required by the protocol. |
| **BISYNC transparent mode** | |
| SYN detect | *DLE-SYN1 |
| Linefill | *DLE-SYN1 |
| SYN/DLE stripping | *DLE-SYN1 and odd DLEs if stripping is specified by RPR[7]. |
| Excluded from FCS | *DLE-SYN1 and odd DLEs, regardless of RPR[7] plus additional characters as required by the protocol. |
| **COP single SYN mode** | |
| SYN detect | SYN1 |
| Linefill | SYN1 |
| SYN stripping | SYN1 used to establish character sync, i.e., leading SYNs. Subsequent to this, SYN1 if stripping is specified by RPR[7]. |
| Excluded from FCS** | SYN1 before beginning of message, i.e., leading SYNs, and if SYN stripping is specified by RPR[7], anywhere else in the message for the Rx; linefill SYN1 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.) |

**NOTES:**

* DLE indicates last DLE of an odd number of consecutive DLEs.

** In non-BISYNC COP modes (single or dual SYN case), if SYN stripping is off, i.e., RPR[7] = 0, then SYNs within a message will be included in FCS by receiver. Therefore, the remote DUSCC transmitter should be careful not to let the TxFIFO underrun since the linefill SYN characters are not accumulated in FCS by the transmitter regardless of RPR[7]. Letting the TxFIFO underrun will result in a CRC error in the receiver.

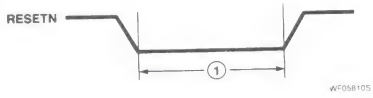



**Figure 12. Reset Timing**

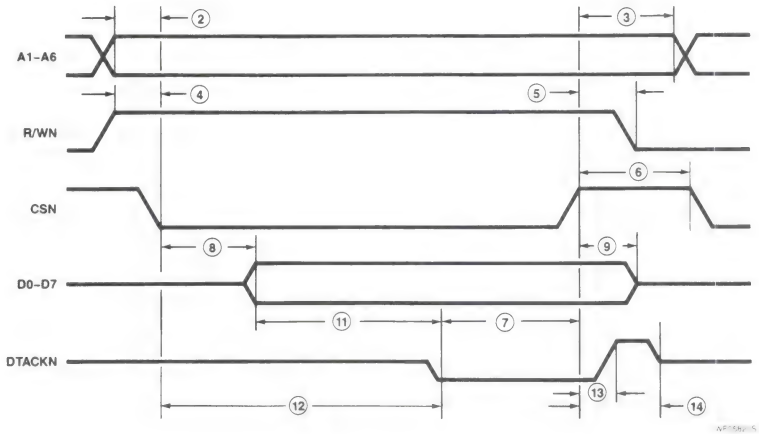



Figure 13. Bus Timing (Read Cycle)

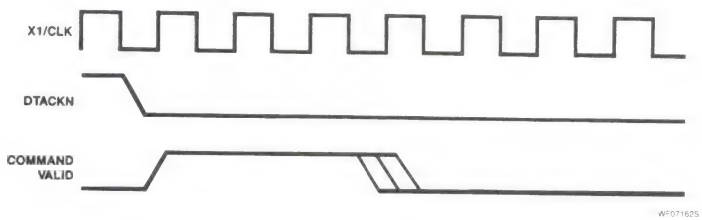



Figure 14. Command Timing

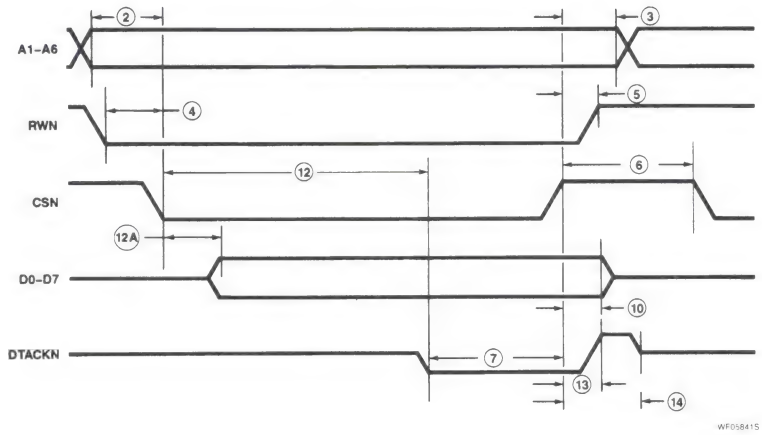



Figure 15. Bus Timing (Write Cycle)

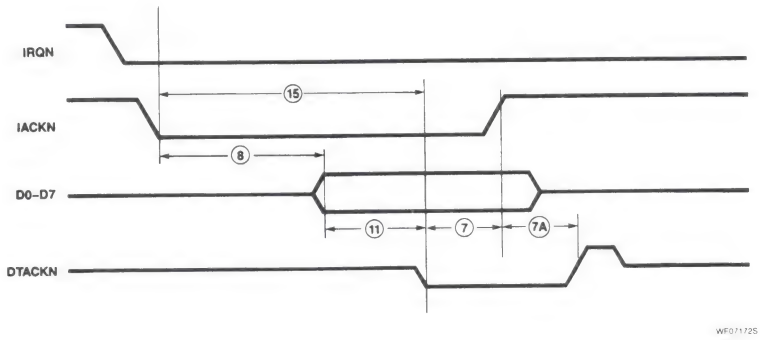



Figure 16. Interrupt Cycle Timing

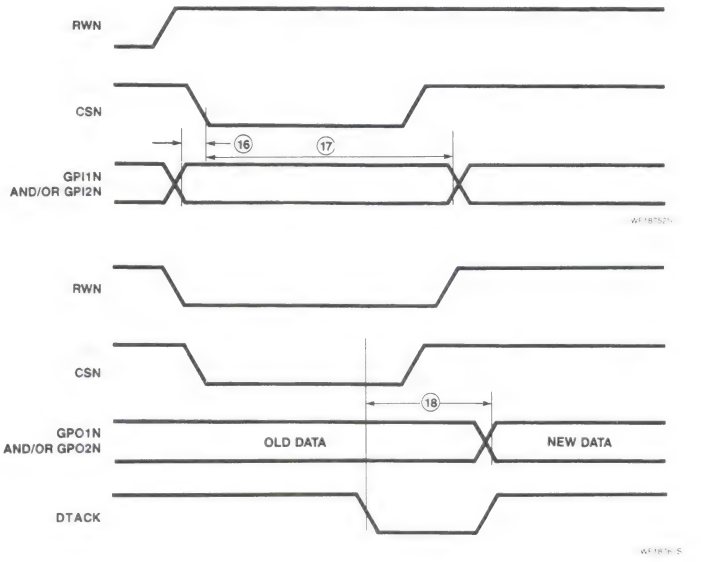



Figure 17. Port Timing

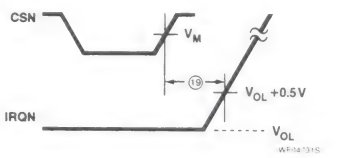



Figure 18. Interrupt Timing

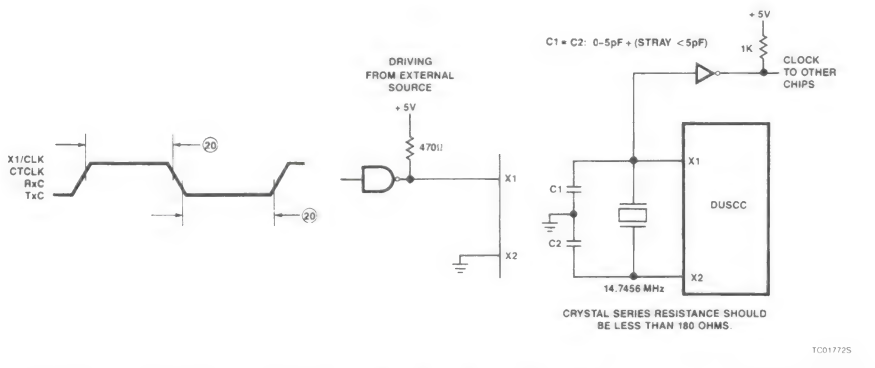



Figure 19. Clock Timing

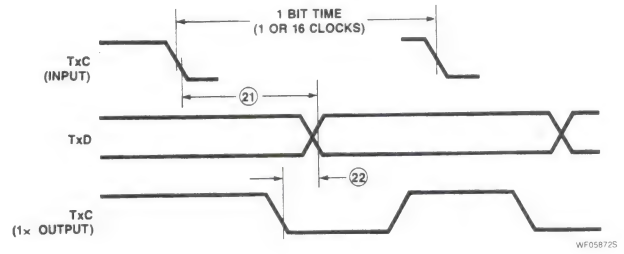



Figure 20. Transmit Timing

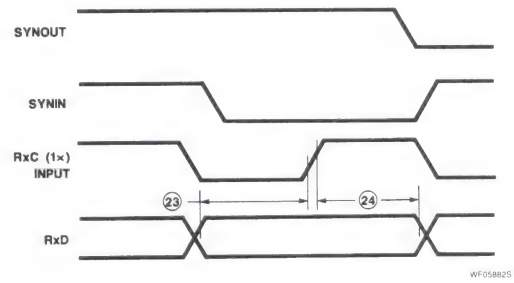



Figure 21. Receive Timing

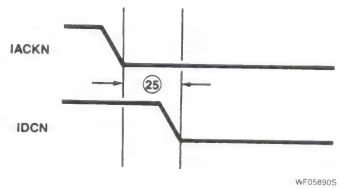



Figure 22. Interrupt Daisy Chain Timing

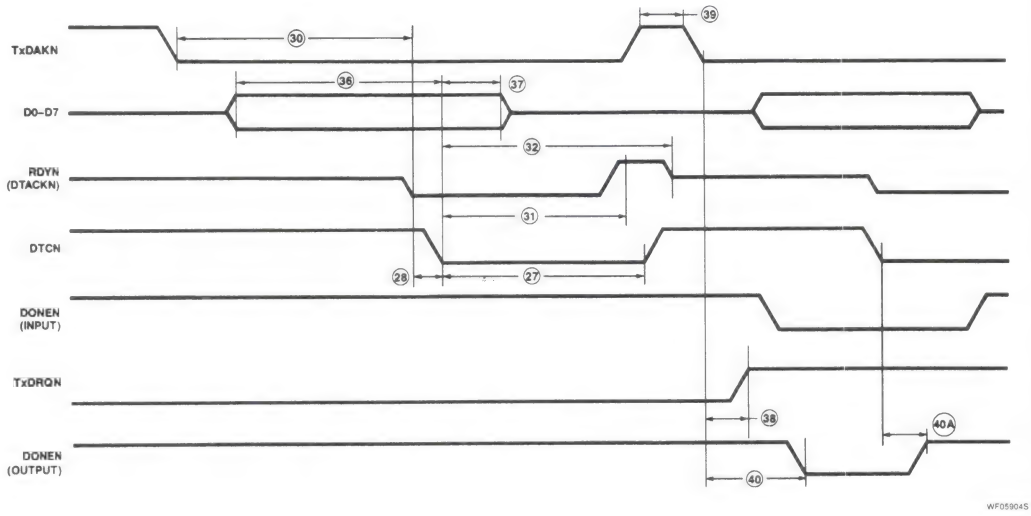



Figure 23. DMA Transmit Write Timing — Single Adress DMA Mode

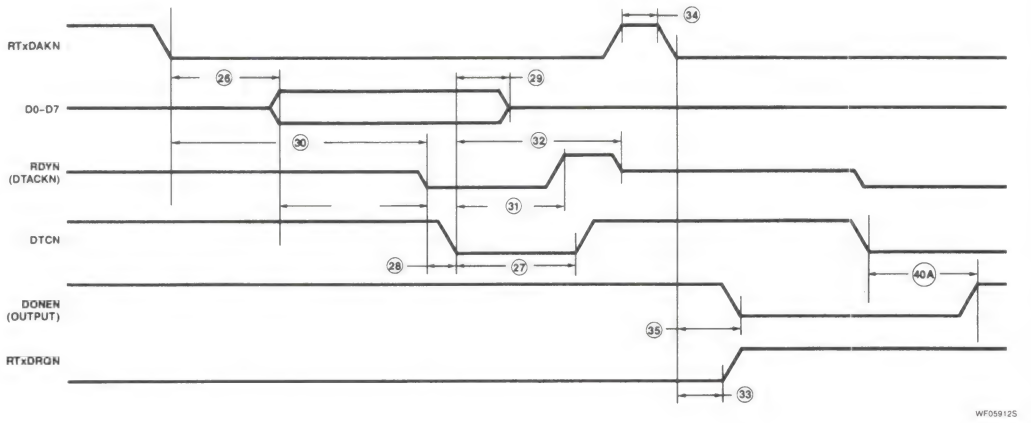



Figure 24. DMA Receiver Read Timing — Single Address DMA Mode

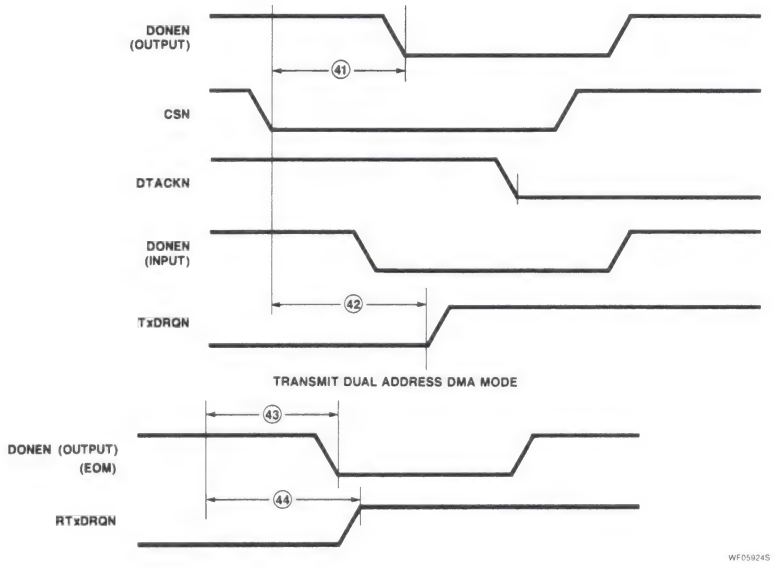



Figure 25. Dual Address DMA Mode Timing

Signetics

Military Microprocessor Products

# 68661/2661
## Enhanced Programmable Communications Interface (EPCI)

*Product Specification*

### DESCRIPTION

The Signetics 68661 EPCI is a universal synchronous/asynchronous data communications controller chip that is an enhanced version of the 68661. It interfaces easily to all 8-bit and 16-bit microprocessors and may be used in a polled or interrupt driven system environment. The 68661 accepts programmed instruction from the microprocessor while supporting many serial data communications disciplines —synchronous and asynchronous — in the full — or half-duplex mode. Special support for BISYNC is provided.

The EPCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The 68661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (A, B, C) has a different set of baud rates.

### FEATURES

- Synchronous operation
  - 5- to 8-bit characters plus parity
  - Single or double SYN operation
  - Internal or external character synchronization
  - Transparent or non-transparent mode
  - Transparent mode DLE stuffing (Tx) and detection (Rx)
  - Automatic SYN or DLE and DLE-SYN stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters plus parity
  - 1, 1-1/2 or 2 stop bits transmitted
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode (echoplex)
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
    DC to 62.5kbps (16X clock)
    DC to 15.625kbps (64X clock)

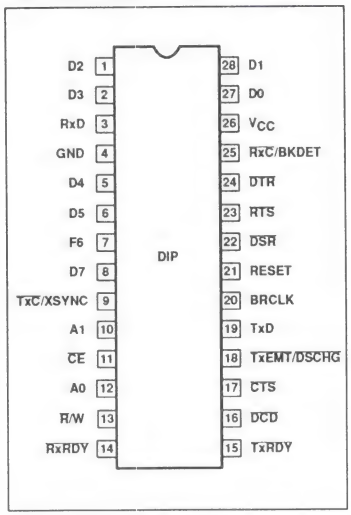
### OTHER FEATURES

- Internal or external baud rate clock
- 3 baud rate sets
- 16 internal rates for each set
- Double-buffered transmitter and receiver
- Full- or half-duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short-circuit protected
- Single +5V power supply
- No system clock required

### APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer-to-computer links
- Serial peripherals
- BISYNC adaptors

### PIN CONFIGURATION




### ORDERING INFORMATION

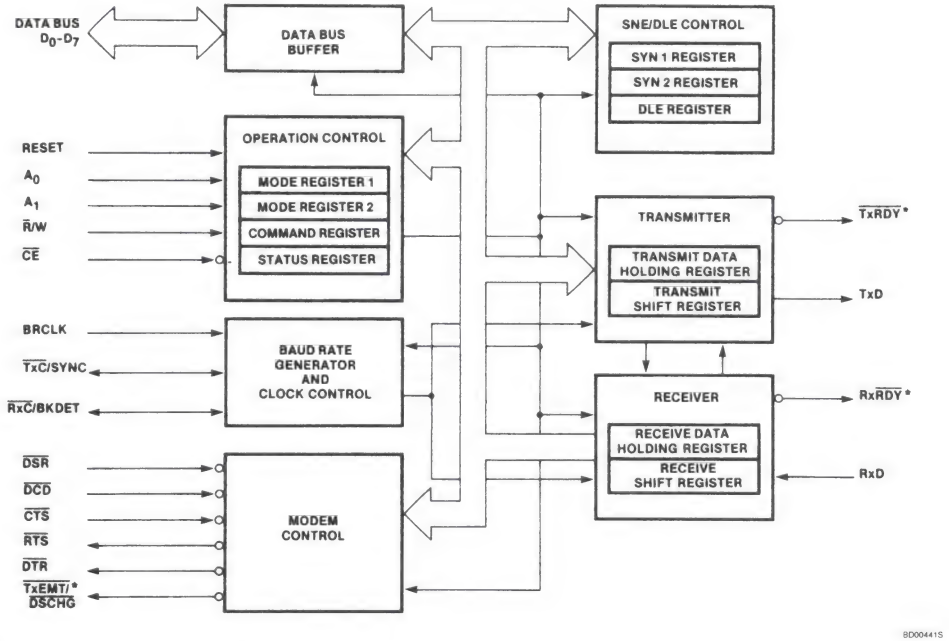
| PACKAGES | ORDER CODE* |
|---|---|
| 28–Pin Ceramic DIP | 68661A/BXA<br>68661B/BXA<br>68661C/BXA |

NOTES:
* See Table 1 for Baud Rate Definition for A, B, or C.
The 68661 is identical to the 2661. Order using part numbers above.

# Enhanced Programmable Communications Interface (EPCI)

# 68661/2661

## BLOCK DIAGRAM




NOTES:
* Open-drain output pin.

# Enhanced Programmable Communications Interface (EPCI) 68661/2661

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_{MAX}$ | All voltages with respect to ground[3] | –0.5 to +6.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High level input voltage | 2.0 | | | V |
| $V_{IL}$ | Low level input voltage | | | 0.8 | V |
| $I_{OL}$ | Low level output current | | | 2.2 | mA |
| $I_{OH}$ | High level output current | | | –400 | µA |
| $T_A$ | Operating free–air temperature range[2] | –55 to +125 | | | °C |

## DC ELECTRICAL CHARACTERISTICS[4, 5, 6]

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Output voltage** | | | | | | |
| $V_{OL}$<br>$V_{OH}$[7] | Low<br>High | $V_{CC}$ = MIN, $I_{OL}$ = MAX<br>$V_{CC}$ = MIN, $I_{OH}$ = MAX | <br>2.4 | | 0.4 | V<br>V |
| $I_{IL}$ | Input Low level current | $V_{CC}$ = MAX, $V_I$ = 0V | | | –10 | µA |
| $I_{IH}$ | Input High level current | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 10 | µA |
| **3–State output leakage current** | | | | | | |
| $I_{OZH}$<br>$I_{OZL}$ | Data bus High<br>Data bus Low | $V_{CC}$ = MAX, $V_O$ = 4.0V<br>$V_{CC}$ = MAX, $V_O$ = 0.45V | | | 10<br>–10 | µA<br>µA |
| $I_{CC}$ | Power supply current | $V_{CC}$ = MAX | | | 150 | mA |

## CAPACITANCE $T_A$ = 25°C, $V_{CC}$ = 0V

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Capacitance** | | | | | | |
| $C_I$[11]<br>$C_O$[11]<br>$C_{I/O}$[11] | Input<br>Output<br>Input/Output | <br>$f_C$ = 1MHz<br>Unmeasured pins tied to ground | | | 20<br>20<br>20 | pF<br>pF<br>pF |

## AC ELECTRICAL CHARACTERISTICS[4, 5, 6, 12]

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Pulse width** | | | | | | |
| $t_{RES}$ | Reset | | 1000 | | | ns |
| $t_{CE}$ | Chip enable | | 250 | | | ns |
| **Setup and hold time** | | | | | | |
| $t_{AS}$ | Address setup | | 10 | | | ns |
| $t_{AH}$ | Address hold | | 10 | | | ns |
| $t_{CS}$ | R/$\overline{W}$ control setup | | 10 | | | ns |
| $t_{CH}$ | R/$\overline{W}$ control hold | | 10 | | | ns |
| $t_{DS}$ | Data setup for write | | 150 | | | ns |
| $t_{DH}$ | Data hold for write | | 10 | | | ns |
| $t_{RXS}$ | RX data setup | | 300 | | | ns |
| $t_{RXH}$ | RX data hold | | 350 | | | ns |
| $t_{DD}$ | Data delay time for read | $C_L$ = 150pF | | | 200 | ns |
| $t_{DF}$[11] | Data bus floating time for read | $C_L$ = 150pF | | | 100 | ns |
| $t_{CED}$ | CE to CE delay | | 600 | | | ns |
| **Input clock frequency** | | | | | | |
| $f_{BRG}$ | Baud rate generator (2661A, B) | | 1.0 | 4.9152 | 4.9202 | MHz |
| $f_{BRG}$ | Baud rate generator (2661C) | | 1.0 | 5.0688 | 5.0738 | MHz |
| $f_{R/T}$[10] | $\overline{TxC}$ or $\overline{RxC}$ | | dc | | 1.0 | MHz |
| **Clock width** | | | | | | |
| $t_{BRH}$[9] | Baud rate High (2661A, B) | | 75 | | | ns |
| $t_{BRH}$[9] | Baud rate High (2661C) | | 70 | | | ns |
| $t_{BRL}$[9] | Baud rate Low (2661A, B) | | 75 | | | ns |
| $t_{BRL}$[9] | Baud rate Low (2661C) | | 70 | | | ns |
| $t_{R/TH}$ | $\overline{TxC}$ or $\overline{RxC}$ High | | 480 | | | ns |
| $t_{R/TL}$[10] | $\overline{TxC}$ or $\overline{RxC}$ Low | | 480 | | | ns |
| $t_{TXD}$ | TxD delay from falling edge of $\overline{TxC}$ | $C_L$ = 150pF | | | 650 | ns |
| $t_{TCS}$ | Skew between TxD changing and falling edge of $\overline{TxC}$ output[8] | $C_L$ = 150pF | | 0 | | ns |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum function temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Over recommended free–air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
5. All voltages measurements are referenced to ground. All time measurements are at the 50% level for inputs (except $t_{BRH}$ and $t_{BRL}$) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of ≤ 20ns maximum.
6. Typical values are at +25°C, typical supply voltages and typical processing parameters.
7. $\overline{INTR}$, $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT/DSCHG}$ outputs are open–drain.
8. Parameter applies when internal transmitter clock is used.
9. Under test conditions of 5.0688MHz $f_{BRG}$ (68661) and 4.9152MHz $f_{BRG}$ (68661A, B), $t_{BRH}$ and $t_{BRL}$ measured at $V_{IH}$ and $V_{IL}$, respectively.
10. In asynchronous local loopback mode, using 1X clock, the following parameters apply: $f_{R/T}$ = 0.83MHz max and $t_{R/TL}$ = 700ns min.
11. See AC load conditions.

# Enhanced Programmable Communications Interface (EPCI)

# 68661/2661

## BLOCK DIAGRAM

The EPCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modern control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control but. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

## Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the EPCI programming section of this data sheet.

## Timing

The EPCI contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full–duplex operation. See Table 1.

## Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

## Transmitter

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

## Modem Control

The modern control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modern.

## SYN/DLE Control

This section contains control circuitry and three 8–bit registers storing the SYNB1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

### Table 1. Baud Rate Generator Characteristics

**68661A (BRCLK = 4.9152MHz)**

| MR23–20 | BAUD RATE | ACTUAL FREQUENCY 16X CLOCK | PERCENT ERROR | DIVISOR |
|---|---|---|---|---|
| 0000 | 50 | 0.8kHz | — | 6144 |
| 0001 | 75 | 1.2 | — | 4096 |
| 0010 | 110 | 1.7598 | –0.01 | 2793 |
| 0011 | 134.5 | 2.152 | — | 2284 |
| 0100 | 150 | 2.4 | — | 2048 |
| 0101 | 200 | 3.2 | — | 1536 |
| 0110 | 300 | 4.8 | — | 1024 |
| 0111 | 600 | 9.6 | — | 512 |
| 1000 | 1050 | 16.8329 | 0.196 | 292 |
| 1001 | 1200 | 19.2 | — | 256 |
| 1010 | 1800 | 28.7438 | –0.19 | 171 |
| 1011 | 2000 | 31.9168 | –0.26 | 154 |
| 1100 | 2400 | 38.4 | — | 128 |
| 1101 | 4800 | 76.8 | — | 64 |
| 1110 | 9600 | 153.6 | — | 32 |
| 1111 | 19200 | 307.2 | — | 16 |

**68661B (BRCLK = 4.9152MHz)**

| MR23–20 | BAUD RATE | ACTUAL FREQUENCY 16X CLOCK | PERCENT ERROR | DIVISOR |
|---|---|---|---|---|
| 0000 | 45.5 | 0.7279kHz | 0.005 | 6752 |
| 0001 | 50 | 0.8 | — | 6144 |
| 0010 | 75 | 1.2 | — | 4096 |
| 0011 | 110 | 1.7598 | –0.01 | 2793 |
| 0100 | 134.5 | 2.152 | — | 2284 |
| 0101 | 150 | 2.4 | — | 2048 |
| 0110 | 300 | 4.8 | — | 1024 |
| 0111 | 600 | 9.6 | — | 512 |
| 1000 | 1200 | 19.2 | — | 256 |
| 1001 | 1800 | 28.7438 | –0.19 | 171 |
| 1010 | 2000 | 31.9168 | –0.26 | 154 |
| 1011 | 2400 | 38.4 | — | 128 |
| 1100 | 4800 | 76.8 | — | 64 |
| 1101 | 9600 | 153.6 | — | 32 |
| 1110 | 19200 | 307.2 | — | 16 |
| 1111 | 38400 | 614.4 | — | 8 |

**68661C (BRCLK = 5.0688MHz)**

| MR23–20 | BAUD RATE | ACTUAL FREQUENCY 16X CLOCK | PERCENT ERROR | DIVISOR |
|---|---|---|---|---|
| 0000 | 50 | 0.8kHz | — | 6336 |
| 0001 | 75 | 1.2 | — | 4224 |
| 0010 | 110 | 1.76 | — | 2880 |
| 0011 | 134.5 | 2.1523 | 0.016 | 2355 |
| 0100 | 150 | 2.4 | — | 2112 |
| 0101 | 300 | 4.8 | — | 1056 |
| 0110 | 600 | 9.6 | — | 528 |
| 0111 | 1200 | 19.2 | — | 264 |
| 1000 | 1800 | 28.8 | — | 176 |
| 1001 | 2000 | 32.081 | 0.253 | 158 |
| 1010 | 2400 | 38.4 | — | 132 |
| 1011 | 3600 | 57.6 | — | 88 |
| 1100 | 4800 | 76.8 | — | 66 |
| 1101 | 7200 | 115.2 | — | 44 |
| 1110 | 9600 | 153.6 | — | 33 |
| 1111 | 19200 | 316.8 | 3.125 | 16 |

**NOTE:**
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

## OPERATION

The functional operation of the 68661 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the EPCI programming section of the data sheet.

After programming, the EPCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

### Receiver

The 68661 is conditioned to receiver data when the $\overline{DCD}$ input is Low and the RxEN bit in the commands register is true. In the asynchronous mode, the receiver looks for High–to–Low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one–half of a bit–time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data are then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the High order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit timer interval. If a break condition is detected (RxD is Low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit SR5 set) will be transferred to the holding register. The RxD input must return to a High condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27–MR24. If so, a detected break will cause that pin to go High. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the Break Detection Timing Diagram.

When the EPCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data are shifted register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the EPCI returns to the hunt mode. (Note that the sequence SYN1–SYN1–SYN2 will not achieve synchronization.) When synchronization has been achieved, the EPCI continues to assemble characters and transfer then to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27–MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1–SYN2, and DLE–SYN1 detection is disable. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxD. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

# Enhanced Programmable Communications Interface (EPCI) 68661/2661

**Table 2. CPU–Related Signals**

| PIN NAME | PIN NO. | INPUT/ OUTPUT | FUNCTION |
|---|---|---|---|
| RESET | 21 | I | A High on this input performs a master reset on the 68661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words. |
| A0, A1 | 12,10 | I | Address lines used to select internal EPCI registers. |
| R/W | 13 | I | Read command when Low, write command when High. |
| $\overline{CE}$ | 11 | I | Chip enable command. When Low, indicates that control and data lines to the EPCI are valid and that the operation specified by the R/W, A1 and A0 inputs should be performed. When High, places the D0–D7 lines in the 3–State condition. |
| D0–D7 | 27,28,1,2,5–8 | I/O | 8–bit, 3–State data bus used to transfer commands, data and status between EPCI and the CPU. D0 is the least significant bit, D7 the most significant bit. |
| $\overline{TxRDY}$ | 15 | O | This output is the complement of status register bit SR0. When Low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes High when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open–drain output which can be used as an interrupt to the CPU. |
| $\overline{RxRDY}$ | 14 | O | This output is the complement of status register bit SR1. When Low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes High when the RHR is ready the CPU, and also when the receiver is disabled. It is an open–drain output which can be used as an interrupt to the CPU. |
| $\overline{TxEMT}$/ $\overline{DSCHG}$ | 18 | O | This output is the complement of status register bit SR2. When Low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCDE}$ inputs has occurred. This output goes High when the status register is ready by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open–drain output which can be used as an interrupt to the CPU. See Status Register (SR2) for details. |

**Table 3. Device–Related Signals**

| PIN NAME | PIN NO. | INPUT/ OUTPUT | FUNCTION |
|---|---|---|---|
| BRCLK | 20 | I | Clock input to the internal baud rate generator (see Table 1). Not required if external receiver and transmitter clocks are used. |
| $\overline{RxC}$/BKDET | 25 | I/O | Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin. |
| $\overline{TxC}$/XSYNC | 9 | I/O | Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input. |
| RxD | 3 | I | Serial data input to the receiver. "Mark" is High, "space" is Low. |
| TxD | 19 | O | Serial data output from the transmitter. "Mark" is High, "Space" is Low. Held in mark condition when the transmitter is disabled. |
| $\overline{DSR}$ | 22 | I | General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a Low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0 = 1. |
| $\overline{DCD}$ | 16 | I | Data carrier detect input. Must be Low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a Low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0 = 1. If $\overline{DCD}$ goes High while receiving, the RxC is internally inhibited. |
| $\overline{CTS}$ | 17 | I | Clear to send input. Must be Low in order for the transmitter to operate. If it goes High during transmission, the character in the transmit shift register will be transmitted before termination. |
| $\overline{DTR}$ | 24 | O | General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready. |
| $\overline{RTS}$ | 23 | O | General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. See Command Register (CR5) for details. |

### Transmitter

The EPCI is conditioned to transmit data when the $\overline{CTS}$ input is Low and the TxEN command register bit is set. The 68661 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data re transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (High) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous Low (BREAK) condition by setting the send break command bit (CR3) High.

In the synchronous mode, when the 68661 is initially conditioned to transmit, the TxD output remains High and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the EPCI unless the CPU fails to send a new character to the EPCI by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the EPCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1–SYN2 doublets, or DLE–SYN1 doubles, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the send DLE bit in the commands register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.

## EPCI PROGRAMMING

Prior to initiating data communications, the 68661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The EPCI can be reconfigured at any time during program execution. A flowchart of the initialization process appears in Figure 1.

The internal registers of the EPCI are accessed by applying specific signals to the $\overline{CE}$, R/$\overline{W}$, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1 = 0, A0 = 1, and R/$\overline{W}$ = 1. The first operation loads the SYN1 register. The next loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a read command register operation, but are unaffected by any other read or write operation.

The 68661 register formats are summarized in Tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the EPCI, while the command register controls the operation within this basic framework. The EPCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

### Mode Register 1 (MR1)

Table 5 illustrates mode register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7 or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14. In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 2X baud rate is programmed, 1.5 stop bits defaults to 1 stop bits on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1–SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE–SYN1 is used for character fill and SYN detect, but he normal synchronization sequence is sued to establish character sync. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also, DLE stripping and DLE detect (with MR14 = 0) are enabled.

The bits in the mode register affecting character assembly and disassembly (MR12–MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half–duplex mode (RxEN = 1 or TxEN = 1, but not both simultaneously = 1). IN asynchronous mode, character changes should be made when RxEN and TxEN = 0 or when TxEN = 1 and the transmitter is marking in half–duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12 – 15 must be changed within n bit times of the active going state of $\overline{RxRDY/TxRDY}$. Transparent and non–transparent mode changes (MR16) must occur within n–1 bit times of the character to be affected when the receiver or transmitter is active. (n – smaller of the new and old character lengths.)

**Table 4. 68661 Register Addressing**

| $\overline{CE}$ | $A_1$ | $A_0$ | R/W | FUNCTION |
|---|---|---|---|---|
| 1 | X | X | X | 3–State data bus |
| 0 | 0 | 0 | 0 | Read receive holding register |
| 0 | 0 | 0 | 1 | Write transmit holding register |
| 0 | 0 | 1 | 0 | Read status register |
| 0 | 0 | 1 | 1 | Write SYN1/SYN2/DLE registers |
| 0 | 1 | 0 | 0 | Read mode register 1/2 |
| 0 | 1 | 0 | 1 | Write mode register 1/2 |
| 0 | 1 | 1 | 0 | Read command register |
| 0 | 1 | 1 | 1 | Write command register |

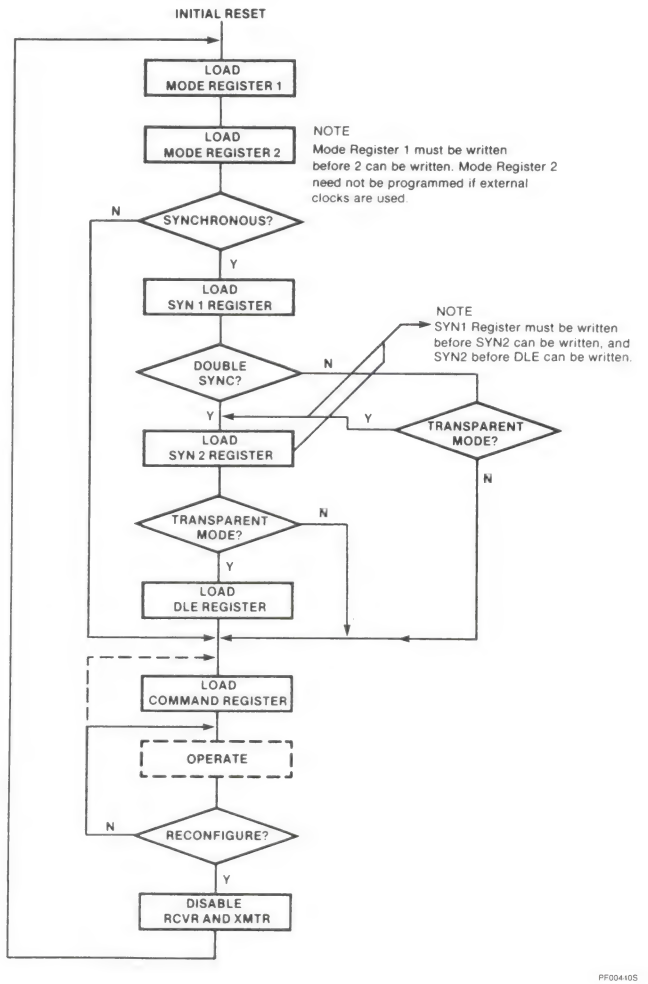



**Figure 1. 68661 Initialization Flowchart**

# Enhanced Programmable Communications Interface (EPCI) — 68661/2661

## Table 5. Mode Register 1 (MR1)

| MR17 | MR16 | MR15 | MR14 | MR13 | MR12 | MR11 | MR10 |
|---|---|---|---|---|---|---|---|
| Sync/Async | | Parity Type | Parity Control | Character Length | | Mode and Baud Rate Factor | |
| Async: Stop bit length<br>00 = invalid<br>01 = 1 stop bit<br>10 = 1 1/2 stop bits<br>11 = 2 stop bits | | 0 = Odd<br>1 = Even | 0 = Disabled<br>1 = Enabled | 00 = 5 bits<br>01 = 6 bits<br>10 = 7 bits<br>11 = 8 bits | | 00 = Synchronous 1X rate<br>01 = Asynchronous 1X rate<br>10 = Asynchronous 16X rate<br>11 = Asynchronous 64X rate | |
| Sync: Number of SYN char<br>0 = Double SYN<br>1 = Single SYN | Sync: Transparency control<br>0 = Normal<br>1 = Transparent | | | | | | |

NOTE: Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

## Table 6. Mode Register 2 (MR2)

| MR27 – MR24 | | | | | | | | | | | MR23 – MR20 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | TxC | RxC | Pin 9 | Pin 25 | | TxC | RxC | Pin 9 | Pin 25 | Mode | Baud Rate Selection |
| 0000 | E | E | TxC | RxC | 1000 | E | E | XSYNC* | RXC/TxC | sync | |
| 0001 | E | I | TxC | 1X | 1001 | E | I | TxC | BKDET | async | |
| 0010 | I | E | 1X | RxC | 1010 | I | E | XSYNC* | RxC | sync | |
| 0011 | I | I | 1X | 1X | 1011 | I | I | 1X | BKDET | async | See baud rates in Table 1. |
| 0100 | E | E | TxC | RxC | 1100 | E | E | XSYNC* | RxC/TxC | sync | |
| 0101 | E | I | TxC | 16X | 1101 | E | I | TXC | BKDET | async | |
| 0110 | I | E | 16X | RxC | 1110 | I | E | XSYNC* | RxC | sync | |
| 0111 | I | I | 16X | 16X | 1111 | I | I | 16X | BKDET | async | |

NOTES:
* When pin 9 is programmed as XSYNC input, SYN1, SYN1–SYN2, and DLE–SYN1 detection is disabled.
E = External clock
I = Internal clock (BRG)
1X and 16X are clock outputs.

## Table 7. Command Register (CR)

| CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |
|---|---|---|---|---|---|---|---|
| Operating Mode | | Request to Send | Reset Error | Sync/Async | Receive Control (RxEN) | Data Terminal Ready | Transmit Control (TxEN) |
| 00 = Normal operation<br>01 = Async:<br>Automatic Echo mode<br>Sync: SYN and/or DLE stripping mode<br>10 = Local loopback<br>11 = Remote loopback | | 0 = Force $\overline{RTS}$ Output High one clock time after TxSR serialization<br>1 = Force $\overline{RTS}$ output Low | 0 = Normal<br>1 = Reset error flags in status reg. (FE,OE,PE/ DLE detect.) | **Async:**<br>Force Break<br>0 = Normal<br>1 = Force break<br><br>**Sync**<br>**Send DLE**<br>0 = Normal<br>1 = Send DLE | 0 = Disable<br>1 = Enable<br><br>Not applicable in | 0 = Force $\overline{DTR}$ output High<br>1 = Force $\overline{DTR}$ output Low | 0 = Disable<br>1 = Enable |

**Table 8. Status Register (SR)**

| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |
|---|---|---|---|---|---|---|---|
| **Data Set Ready** | **Data Carrier Detect** | **FE/SYN Detect** | **Overrun** | **PE/DLE Detect** | **TxEMT DSCHG** | **RxRDY** | **TxRDY** |
| 0 = $\overline{DSR}$ input is High<br>1 = $\overline{DSR}$ input is Low | 0 = $\overline{DCD}$ input is High<br>1 = $\overline{DCD}$ input is Low | **Async:**<br>0 = Normal<br>1 = Framing error<br>**Sync:**<br>0 = Normal<br>1 = SYN detected | 0 = Normal<br>1 = Overrun error | **Async:**<br>0 = Normal<br>1 = Parity error<br>**Sync:**<br>0 = Normal<br>1 = Parity error or DLE received | 0 = Normal<br>1 = Change in $\overline{DSR}$ or $\overline{DCD}$, or transmit shift register is empty | 0 = Receive holding register empty<br>1 = Receive holding register has data | 0 = Transmit holding register busy<br>1 = Transmit holding register empty |

## Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each EPCI version (–1,–2,–3). Versions 1 and 2 specify a 4.9152MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688MHz input which is identical to the Signetics 2651. MR23 – 20 are don't cares if external clocks are selected (MR25 – MR24 = 0). The individual rates are given in Table 1.

MR24 – MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to Table 6.

## Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0–to–1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go High (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (High) while $\overline{TxRDY}$ and $\overline{TxEMT}$ will go High (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. A 0–to–1 transition of CR2 will initiate start bit search (async) or hunt mode (sync).

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output Low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go High for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register ;contents prior to sending the character in the transmit data holding register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE–non–DLE character sequences.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared,. this is a one time command. There is not internal latch for this bit.

When CR5 (RTS) is set, the $\overline{RTS}$ pin is forced Low. A 1–to–0 transition of CR5 will cause $\overline{RTS}$ to go High (inactive) one TxC time after the last serial bit has been transmitted. If a 1–to–0 transition of CR5 occurs while data is being transmitted, $\overline{RTS}$ will remain Low (active) until both the THR and the transmit shift register are empty and then go High (inactive) one TxC time later.

The EPCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational sub–mode is determined by CR7 and CR6. CR7 – CR6 = 00 is the normal mode, with the transmitter and receive operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7 – CR6 = 01 places the EPCI in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed.

The TxD output will go High until the next valid start is detected. The following conditions are true while in automatics echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ output = 1.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7 – CR6 = 01 places the EPCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non–transparent, single SYN mode (MR17 – MR16 = 10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding register (RHR).
2. In the non–transparent, double SYN mode (MR17 – MR16 = 00), character in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred the RHR.
3. In transparent mode (MR16 = 1), character in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE–DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic sub–modes can also be configured. In local loopback mode (CR7 – CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held High.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 (DTR) and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the EPCI.

The second diagnostic mode is the remote loopback mode (CR7 – CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receiver clock.
3. No data are sent to the local CPU, but he error status conditions (PE, FE) are set.
4. The $\overline{\text{RxRDY}}$, $\overline{\text{TxRDY}}$, and $\overline{\text{TxEMT}}$/$\overline{\text{DSCHG}}$ outputs are held High.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

## Status Register

The data contained in the status register (as shown in Table 8) indicates receive rand transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0–, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit register. If set equal to 1, it indicates that the holding register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is Low. In the automatic echo and remote loopback modes, the output is held High.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is Low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs (when CR2 or CR0 = 1) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG conditions is enabled when TxEN = 1 or RxEN = 1. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 – 1 while SR6 and SR7 remain unchanged, the a TxEMT condition exists. When SR2 is set, the $\overline{\text{TxEMT}}$/$\overline{\text{DSCHG}}$ output is Low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching DLE register was received and the present character is neither SYN2 or DLE. This bit is cleared when the next character following the above sequence is loaded into RHR, when the receiver is disabled, or by a reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not ready the CPU at the time of new received character was transferred into it. This bit is cleared when the receiver is disabled or by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit; i.e., only the first stop bit is checked. If RHR = 0 when SR5 = 1, a break condition is present. In synchronous non–transparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1 – SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN or SYN1 – SYN2) and, after synchronization has been achieved, when a DLE–SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, or when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs, respectively. A Low input sets its corresponding status bit, and a High input clears it.

**Table 9. 68661 EPCI vs 2651 PCI**

| FEATURE | EPCI | PCI |
|---|---|---|
| 1. MR2 BIT 6, 7 | Control pins 9, 25 | Not used |
| 2. DLE detect – SR3 | SR3 = 0 for DLE–DLE, DLE – SYN1 | SR3 = 1 for DLE–DLE, DLE – SYN1 |
| 3. Reset of SR3, DLE detect | Second character after DLE, or receiver disable, or CR4 = 1 | Receiver disable, or CR4 = 1 |
| 4. Send DLE – CR3 | One time command | Reset via CR3 on next $\overline{\text{TxRDY}}$ |
| 5. DLE stuffing in transparent mode | Automatic DLE stuffing when DLE is loaded except if CR3 = 1 | None |
| 6. SYN1 stripping in double sync non–transparent mode | All SYN1 | First SYN1 of pair |
| 7. Baud rate versions | Three | One |
| 8. Terminate ASYNC transmission (drop RTS) | Reset CR5 in response to $\overline{\text{TxEMT}}$ changing from 1 to 0 | Reset CR0 when $\overline{\text{TxEMT}}$ goes from 1 to 0. Then reset CR5 when $\overline{\text{TxEMT}}$ goes from 1 to 0 |
| 9. Break detect | Pin 25* | FE and null character |
| 10. Stop bit searched | One | Two |
| 11. External jam sync | Pin 9** | No |
| 12. Data bus timing | Improved over 2651 | — |
| 13. Data bus drivers | Sink 2.2mA<br>Source 400µA | Sink 1.6mA<br>Source 100µA |

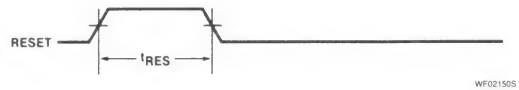
NOTES:
* Internal BRG used for RxC.
** Internal BRG used for TxC.

## AC LOAD CONDITIONS

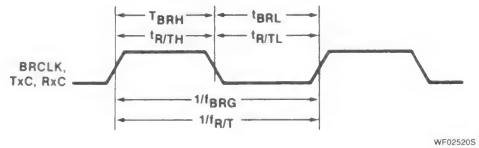
NOTES:
Open–drain outputs.
$C_L$ = Load capacitance includes JIG and probe capacitance.

## TIMING DIAGRAMS

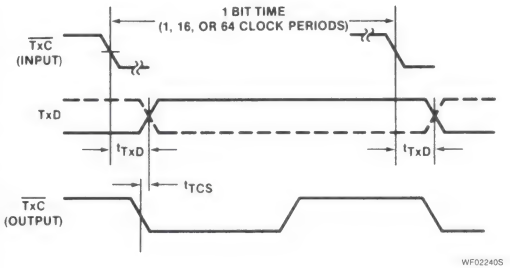
### RESET



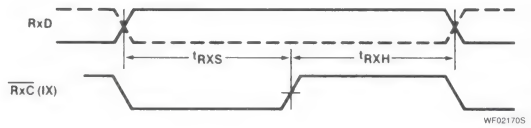

### CLOCK



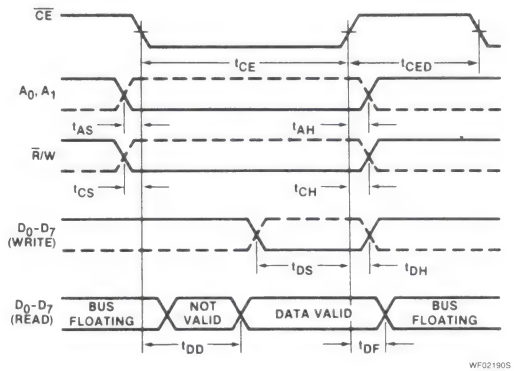

### TRANSMIT




### RECEIVE

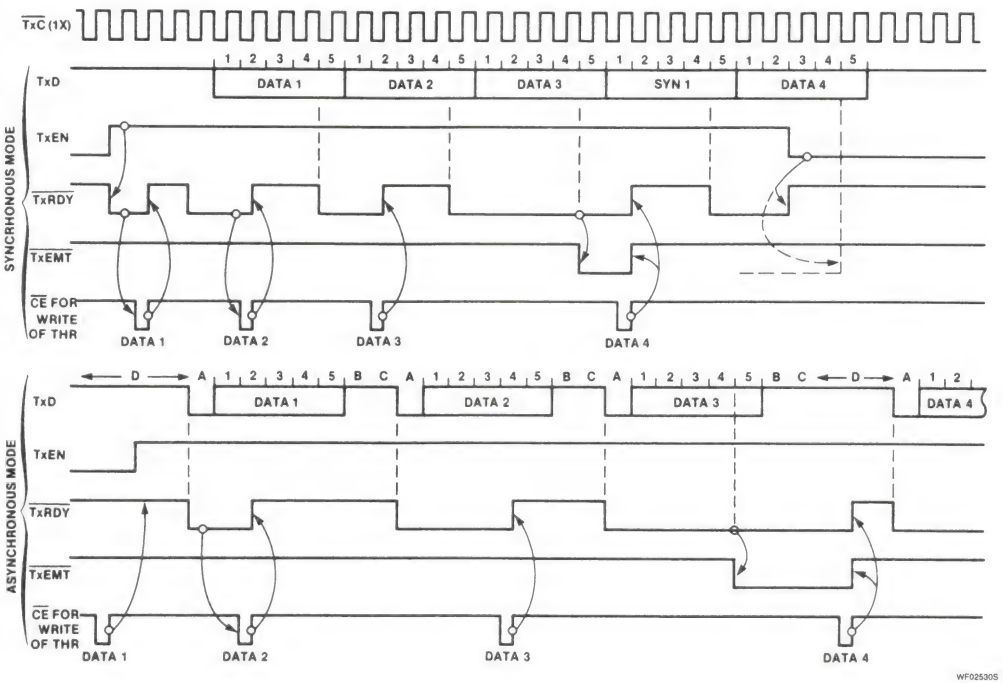



### READ AND WRITE



## TIMING DIAGRAMS (Continued)

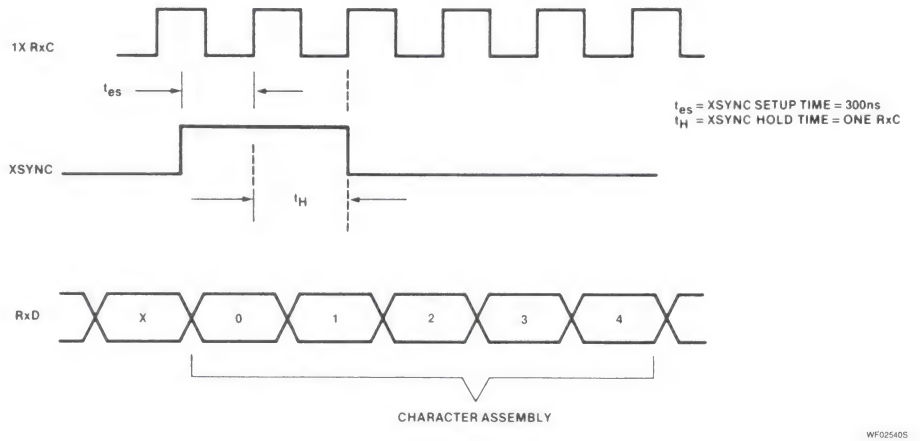
**TxRDY, TxEMT** (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



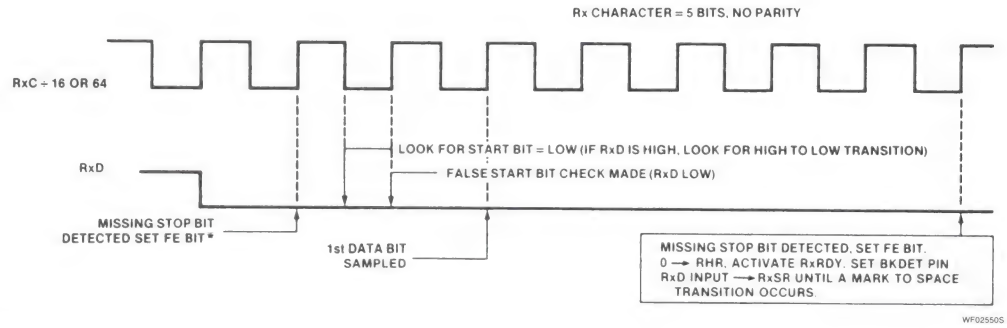

**NOTES:**
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

## TIMING DIAGRAMS (Continued)

### EXTERNAL SYNCHRONIZATION WITH XSYNC



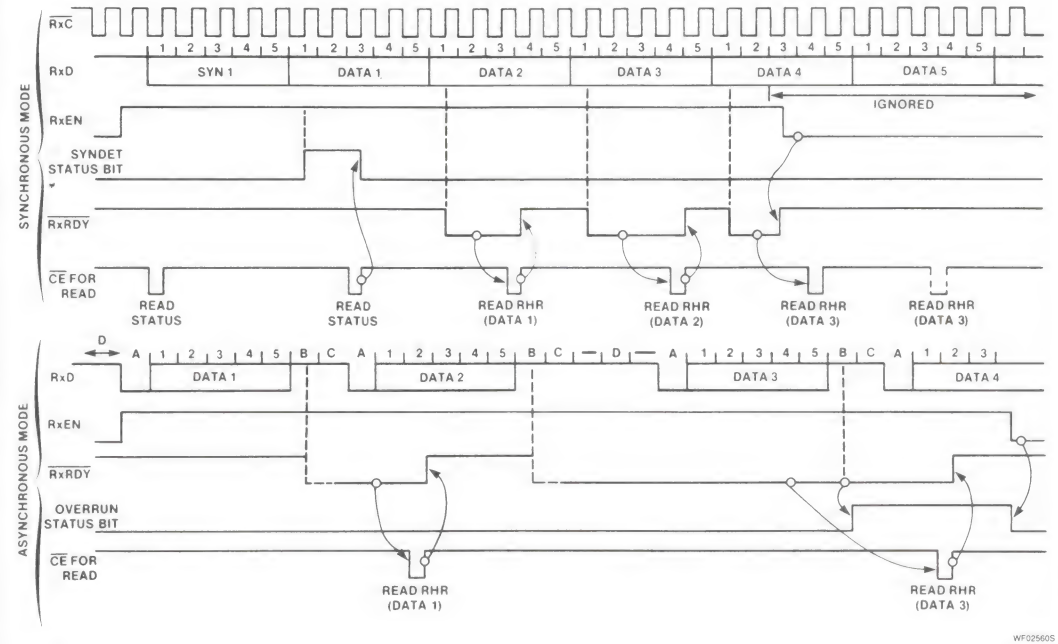

### BREAK DETECTION TIMING


Rx CHARACTER = 5 BITS, NO PARITY
RxC ÷ 16 OR 64
RxD
LOOK FOR START BIT = LOW (IF RxD IS HIGH, LOOK FOR HIGH TO LOW TRANSITION)
FALSE START BIT CHECK MADE (RxD LOW)
MISSING STOP BIT DETECTED SET FE BIT*
1st DATA BIT SAMPLED
MISSING STOP BIT DETECTED, SET FE BIT.
0 → RHR, ACTIVATE RxRDY, SET BKDET PIN
RxD INPUT → RxSR UNTIL A MARK TO SPACE TRANSITION OCCURS.
WF02550S

**NOTE:**
* If the stop bit is present, the start bit search will commence immediately.

## TIMING DIAGRAMS (Continued)

**RxRDY** (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



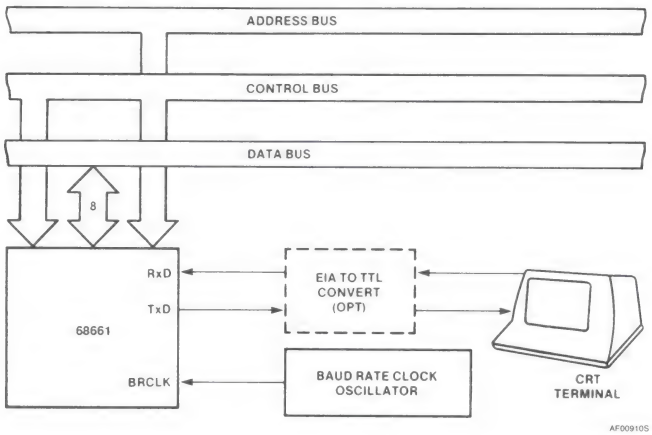

**NOTES:**
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
Only one stop bit is detected.

# Enhanced Programmable Communications Interface (EPCI)

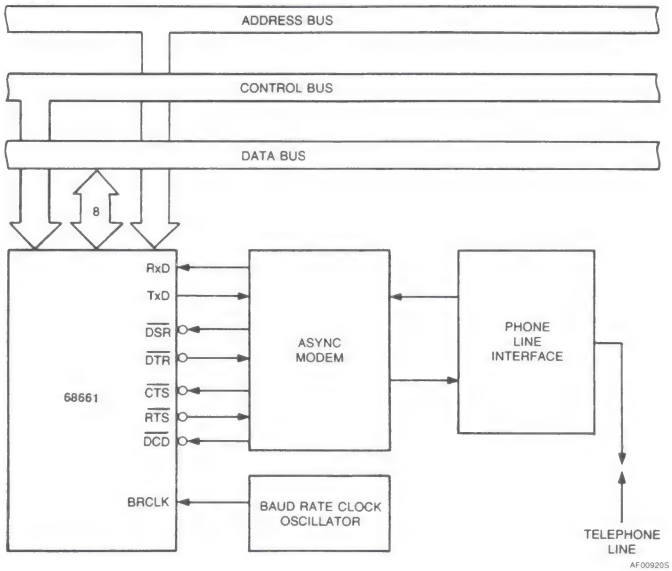


## TYPICAL APPLICATIONS

### ASYNCHRONOUS INTERFACE TO CRT TERMINAL

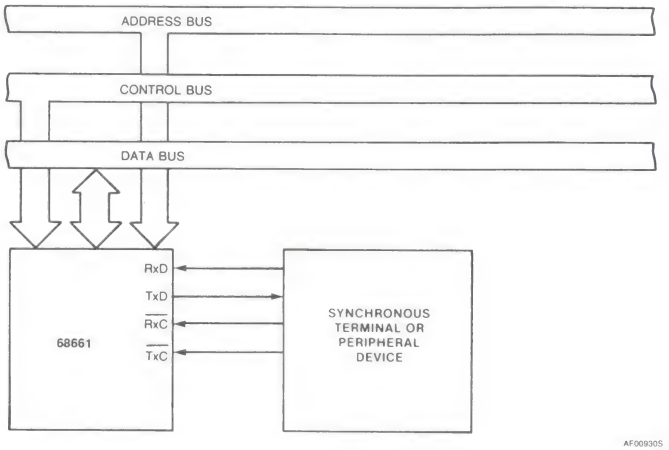



### ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

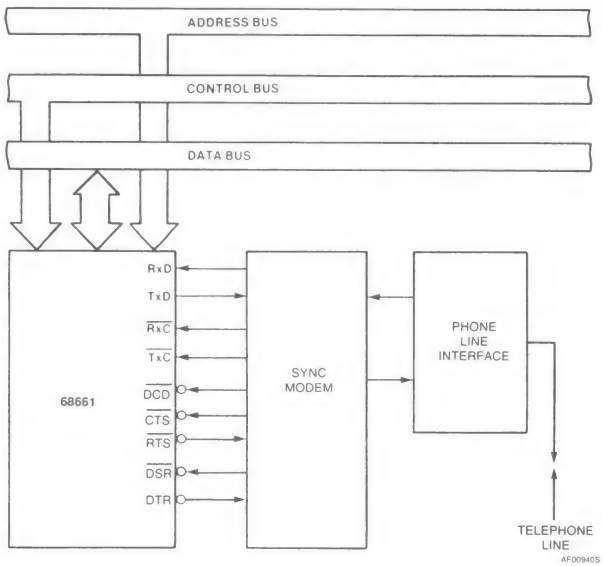


## TYPICAL APPLICATIONS (Continued)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE




SYNCHRONOUS INTERFACE TO TELEPHONE LINES



Signetics

# 68681
## Dual Asynchronous Receiver/Transmitter (DUART)

*Product Specification*

**Military Microprocessor Products**

### DESCRIPTION

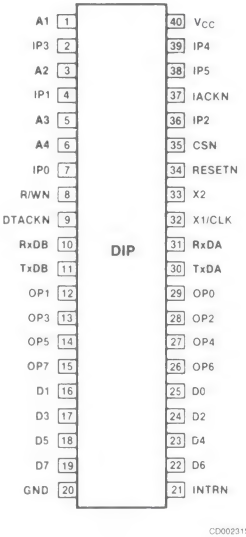
The Signetics 68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other 68000 family devices, and can also interface easily with other microprocessors. The DUART can be used in polled or interrupt driven systems.

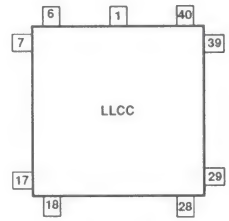
The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

### FEATURES

- 68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multifunction programmable 16-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multifunction 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X - 1MB/sec, 16X - 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply

### PIN CONFIGURATIONS




**PIN/FUNCTION**

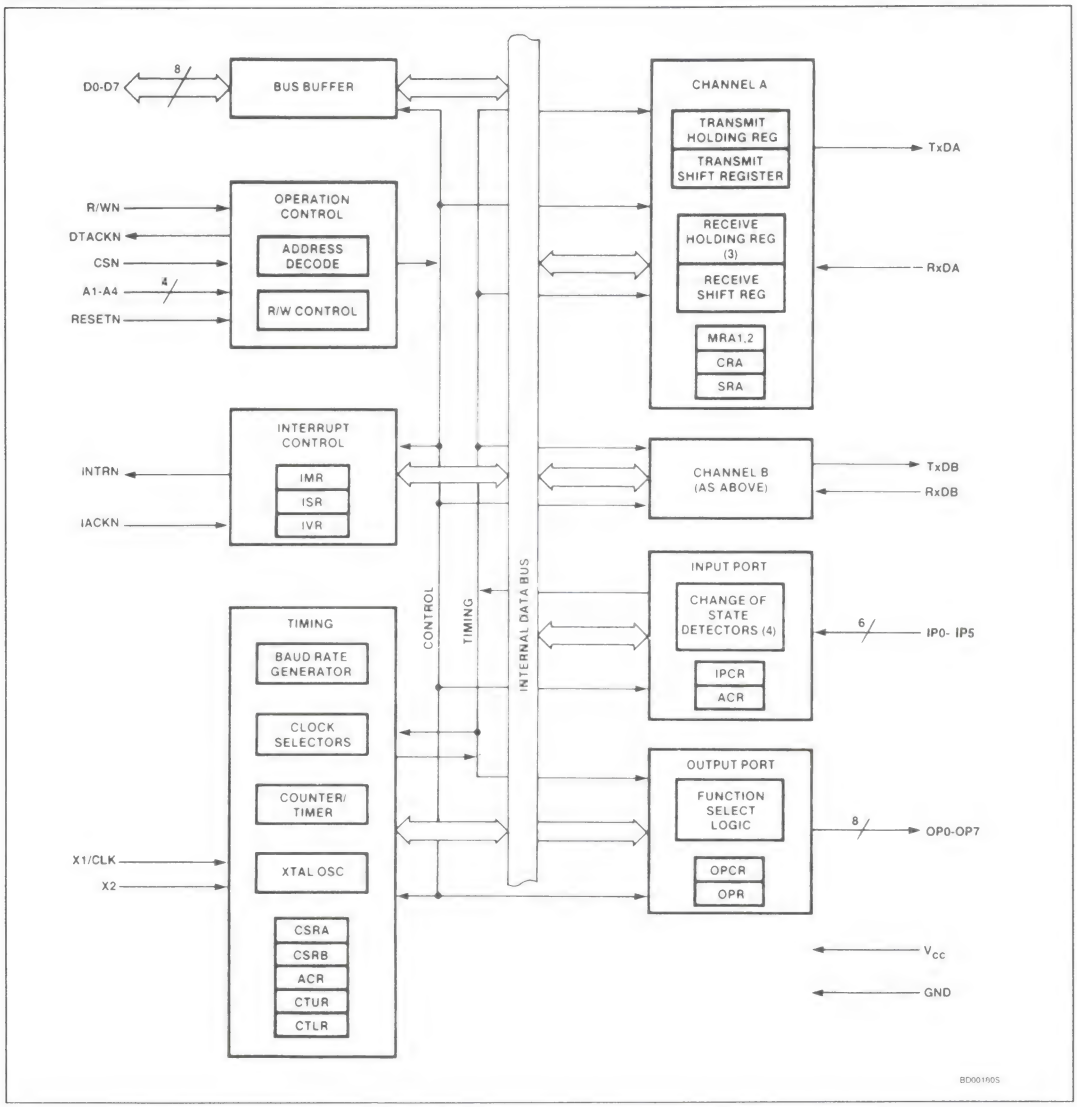
| | | | | | |
|---|---|---|---|---|---|
| 1 | NC | 16 | OP5 | 31 | OP2 |
| 2 | A1 | 17 | OP7 | 32 | OP0 |
| 3 | IP3 | 18 | D1 | 33 | TxDA |
| 4 | A2 | 19 | D3 | 34 | NC |
| 5 | IP1 | 20 | D5 | 35 | RxDA |
| 6 | A3 | 21 | D7 | 36 | X1/CLK |
| 7 | A4 | 22 | GND | 37 | X2 |
| 8 | IP0 | 23 | NC | 38 | RESETN |
| 9 | R/WN | 24 | INTRN | 39 | CSN |
| 10 | DTACKN | 25 | D6 | 40 | IP2 |
| 11 | RxDB | 26 | D4 | 41 | IACKN |
| 12 | NC | 27 | D2 | 42 | IP5 |
| 13 | TxDB | 28 | D0 | 43 | IP4 |
| 14 | OP1 | 29 | OP6 | 44 | $V_{CC}$ |
| 15 | OP3 | 30 | OP4 | | |

# Dual Asynchronous Receiver/Transmitter (DUART) 68681

## ORDERING INFORMATION

| PACKAGE | ORDER CODE |
|---|---|
| 40–Pin Ceramic DIP | 68681/BQA |
| 44–Pin LLCC | 68681/BUA |

## BLOCK DIAGRAM



# Dual Asynchronous Receiver/Transmitter (DUART) 68681

## PIN DESCRIPTION

| SYMBOL | TYPE | NAME AND FUNCTION |
|---|---|---|
| D0-D7 | I/O | **Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit. |
| CSN | I | **Chip Select:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the R/WN, RDN and A1-A4 inputs. When High, places the D0-D7 lines in the 3-State condition. |
| R/WN | I | **Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input. |
| A1-A4 | I | **Address Inputs:** Select the DUART internal registers and ports for read/write operations. |
| RESETN | I | **Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0-OP7 in the High state, stops the coutner/timer, and puts Channel A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. |
| DTACKN | O | **Data Transfer Acknowledge:** Three-state active Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART. |
| INTRN | O | **Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true. |
| IACKN | I | **Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending. |
| X1/CLK | I | **Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. If a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). |
| X2 | I | **Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If an external clock is used, this pin should be grounded. |
| RxDA | I | **Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low. |
| RxDB | I | **Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low. |
| TxDA | O | **Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low. |
| TxDB | O | **Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low. |
| OP0 | O | **Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit. |
| OP1 | O | **Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit. |
| OP2 | O | **Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output. |
| OP3 | O | **Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output. |
| OP4 | O | **Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output. |
| OP5 | O | **Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output. |
| OP6 | O | **Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output. |
| OP7 | O | **Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYB output. |
| IP0 | I | **Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN). |
| IP1 | I | **Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN). |
| IP2 | I | **Input 2:** General purpose input, or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. |
| IP3 | I | **Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. |
| IP4 | I | **Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. |
| IP5 | I | **Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. |
| $V_{CC}$ | I | **Power Supply:** +5V supply input. |
| GND | I | **Ground:** |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |
| $V_{MAX}$ | All voltages with respect to ground[3] | -0.5 to +6.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$<br>$V_{IH}$ (X/CLK) | High level input voltage<br>High level input voltage | 2.0<br>4.0 | | | V<br>V |
| $V_{IL}$ | Low level input voltage | | | 0.8 | V |
| $I_{OL}$ | Low level output current | | | 2.4 | mA |
| $I_{OH}$ | High level output current | | | -400 | µA |
| $T_A$ | Operating free-air temperature range[2] | -55 to +125 | | | °C |

## DC ELECTRICAL CHARACTERISTICS $T_A$ = -55°C to +125°C[2], $V_{CC}$ = 5.0V ± 10%[4,5,6]

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[6] | Max | |
| $V_{OL}$<br>$V_{OH}$ | Output Low voltage<br>Output High voltage (except OD outputs) | $I_{OL}$ = 2.4mA<br>$I_{OH}$ = -400µA | <br>2.4 | | 0.4 | V<br>V |
| $I_{IL}$<br>$I_{OZL}$,<br>$I_{OZH}$ | Input leakage current<br>Data bus 3-State leakage current | $V_I$ = 0 to $V_{CC}$<br>$V_O$ = 0.4 to $V_{CC}$ | -10<br>-10 | | 10<br>10 | µA<br>µA |
| $I_{IL}$(X1) | X1/CLK Low input current | $V_I$ = 0, X2 GND<br>$V_I$ = 0, X2 floated | -4.0<br>-3.0 | -2.0<br>-1.5 | 0.0<br>0.0 | mA<br>mA |
| $I_{IH}$(X1) | X1/CLK High input current | $V_I$ = $V_{CC}$, X2 GND<br>$V_I$ = $V_{CC}$, X2 floated | -1.0<br>0.0 | 0.2<br>3.5 | 1.0<br>10.0 | mA<br>mA |
| $I_{IL}$(X2)<br>$I_{IH}$(X2) | X2 Low input current<br>X2 High input current | $V_I$ = 0, X1/CLK floated<br>$V_I$ = $V_{CC}$, X1/CLK floated | -100<br>0.0 | -30<br>+30 | 0.0<br>100 | µA<br>µA |
| $I_{OH}$ | Open-drain output leakage current | $V_O$ = 0.4 to $V_{CC}$ | -10 | | 10 | µA |
| $I_{CC}$ | Power supply current | $V_{CC}$ = 5.5V, $T_A$ = 25°C, +125°C | | | 150 | mA |
| $I_{CC}$ | Power supply current | $V_{CC}$ = 5.5V, $T_A$ = -55°C | | | 175 | µA |
| $C_{IN}$[10] | Input | | | | 20 | pF |
| $C_{OUT}$[10] | Output | | | | 20 | pF |

## AC CHARACTERISTICS $T_A$ = -55°C to +125°C, $V_{CC}$ = 5.0V ± 10%[4, 5, 6, 7]

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ[6] | Max | |
| **Reset Timing (See Figure 1)** | | | | | |
| $t_{RES}$ | RESETN pulse width | 1.0 | | | µs |
| **Bus Timing (See Figures 2, 3 4)** | | | | | |
| $t_{AS}$ | A1-A4 setup time to CSN Low | 10 | | | ns |
| $t_{AH}$ | A1-A4 hold time from CSN High | 0 | | | ns |
| $t_{RWS}$ | RWN setup time to CSN High | 0 | | | ns |
| $t_{RWH}$ | RWN holdup time to CSN High | 0 | | | ns |
| $t_{CSW}$ | CSN High pulse width | 90 | | | ns |
| $t_{CSD}$[8] | CSN or IACKN High from DTACKN Low | 20 | | | ns |
| $t_{DD}$ | Data valid from CSN or IACKN Low | | | 175 | ns |
| $t_{DF}$ | Data bus floating from CSN or IACKN High[10] | | | 100 | ns |
| $t_{DS}$ | Data setup time to CLK High | 100 | | | ns |
| $t_{DH}$ | Data hold time from CSN High | 0 | | | ns |
| $t_{DAL}$ | DTACKN Low from read data valid | 0 | | | ns |
| $t_{DCR}$ | DTACKN Low (read cycle) from CLK High | | | 125 | ns |
| $t_{DCW}$ | DTACKN Low (write cycle) from CLK High | | | 125 | ns |
| $t_{DAH}$ | DTACKN High from CSN or IACKN High | | | 100 | ns |
| $t_{DAT}$ | DTACKN High imepdance from CSN or IACKN High | | | 125 | ns |
| $t_{CSC}$[9] | CSN or IACKN setup time to clock High | 90 | | | ns |
| **Port Timing (See Figure 5)** | | | | | |
| $t_{PS}$ | Port input setup time to CSN Low | 0 | | | ns |
| $t_{PH}$ | Port input hold time from CSN High | 0 | | | ns |
| $t_{PD}$ | Port output valid from CSN High | | | 400 | ns |
| **Interrupt Reset Timing (See Figure 6)** | | | | | |
| | INTRN or OP3-OP7 when used as interrupts negated from: | | | | |
| | Read RHR (RxRDY/FFULL interrupt) | | | 300 | ns |
| | Write THR (TxRDY interrupt) | | | 300 | ns |
| $t_{IR}$ | Reset command (delta break interrupt) | | | 300 | ns |
| | Stop C/T command (counter interrupt) | | | 300 | ns |
| | Read IPCR (input port change interrupt) | | | 300 | ns |
| | Write IMR (clear of interrupt mask bit) | | | 300 | ns |
| **Clock Timing (See Figure 7)** | | | | | |
| $t_{CLK}$ | X1/CLK High or Low time | 100 | | | ns |
| $f_{CLK}$ | X1/CLK frequency | 2.0 | 3.6864 | 4.0 | MHz |
| $t_{CTC}$ | CTCLK High or Low time | 100 | | | ns |
| $f_{CTC}$ | CTCLK frequency | 0 | | 4.0 | MHz |
| $t_{RX}$ | RxC High or Low time | 220 | | | ns |
| $f_{RX}$ | RxC frequency (16X) | 0 | | 2.0 | MHz |
| | (1X) | 0 | | 1.0 | MHz |
| $t_{TX}$ | TxC High or Low time | 220 | | | ns |
| $f_{TX}$ | TxC frequency (16X) | 0 | | 2.0 | MHz |
| | (1X) | 0 | | 1.0 | MHz |
| **Transmitter Timing (See Figure 8)** | | | | | |
| $t_{TXD}$ | TxD output delay from TxC Low | | | 350 | ns |
| $t_{TCS}$ | Output delay from TxC Low to TxD data output | | | 150 | ns |
| **Receiver Timing (See Figure 9)** | | | | | |
| $t_{RXS}$ | RxD data setup time to RxC High | 240 | | | ns |
| $t_{RXH}$ | RxD data hold time from RxC High | 200 | | | ns |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of $\leq$ 20ns. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. Test conditions for outputs: $C_L$ = 150pF, except interrupt outputs. Test condition for interrupt outputs: $C_L$ = 50pF, $R_L$ = 2.7kΩ to $V_{CC}$.
8. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
9. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.
10. This parameter is guaranteed but not tested.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Also provided on the 68681 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

## BLOCK DIAGRAM

The 68681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

### Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

### Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

### Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auditary Control Register(ACR) and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR regsiter on the data bus and asserting DTACKN.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

### Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART. If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4k baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

### Communications Channels A and B

Each communications channel of the 68681 comprises a full-duplex asynchronous receiver/transmitter (DUART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (assuming that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee a true change in level has occurred, requires that two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. The 50µs time refers to the situation in which the change of state is just missed and the first change of state is not detected until 25µs later.

### Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address D16. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1 and D6 will reflect the level of IACKN. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

### Output Port

The 8-bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR[n] = 1 results in OP[n] = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

## OPERATION

### Transmitter

The 68681 is conditioned to transmit data when the transmitter is enabled through the command register. The 68681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters can-

not be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

## Receiver

The 68681 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

## Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

## PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'OA' should never be read during normal operation since they are reserved for internal diagnostics.

**Table 1. 68681 Register Addressing**

| A4 | A3 | A2 | A1 | READ (R/WN = 1) | WRITE (R/WN = 0) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Mode Register A (MR1A, MR2A) | Mode Register A (MR1A, MR2A) |
| 0 | 0 | 0 | 1 | Status Register A (SRA) | Clock Select Register A (CSRA) |
| 0 | 0 | 1 | 0 | *Reserved* | Command Register A (CRA) |
| 0 | 0 | 1 | 1 | Rx Holding Register A (RHRA) | Tx Holding Register A (THRA) |
| 0 | 1 | 0 | 0 | Input Port Change Register (IPCR) | Aux. Control Register (ACR) |
| 0 | 1 | 0 | 1 | Interrupt Status Register (ISR) | Interrupt Mask Register (IMR) |
| 0 | 1 | 1 | 0 | Counter/Timer Upper (CTU) | C/T Upper Register (CRUR) |
| 0 | 1 | 1 | 1 | Counter/Timer Lower (CTL) | C/T Lower Register (CTLR) |
| 1 | 0 | 0 | 0 | Mode Register B (MR1B, MR2B) | Mode Register B (MR1B, MR2B) |
| 1 | 0 | 0 | 1 | Status Register B (SRB) | Clock Select Register B (CSRB) |
| 1 | 0 | 1 | 0 | *Reserved* | Command Register B (CRB) |
| 1 | 0 | 1 | 1 | Rx Holding Register B (RHRB) | Tx Holding Register B (THRB) |
| 1 | 1 | 0 | 0 | Interrupt Vector Register (IVR) | Interrupt Vector Register (IVR) |
| 1 | 1 | 0 | 1 | Input Port | Output Port Conf. Register (OPCR) |
| 1 | 1 | 1 | 0 | Start Counter Command | Set Output Port Bits Command |
| 1 | 1 | 1 | 1 | Stop Counter Command | Reset Output Port Bits Command |

## MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

**MR1A[7] – Channel A Receiver Request-to-Send Control**

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

**MR1A[6] – Channel A Receiver Interrupt Select**

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

**MR1A[5] – Channel A Error Mode Select**

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

**MR1A[4:3] – Channel A Parity Mode Select**

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

**MR1A[2] – Channel A Parity Type Select**

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

**MR1A[1:0] – Channel A Bits Per Character Select**

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

## MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

**MR2A[7:6] – Channel A Mode Select**

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.

4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

**MR2A[5] – Channel A Transmitter Request-to-Send Control**

This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Verify the message is sent by waiting until the transmit ready status (TxRDY) is asserted. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

**MR2A[4] – Channel A Clear-to-Send Control**

If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IP0) each time it is ready to send a character. If IP0 is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

**MR2A[3:0] – Channel A Stop Bit Length Select**

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled), in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

## MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

**Table 2. Register Bit Formats**

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 BIT 3 | BIT 2 | BIT 1 BIT 0 |
|---|---|---|---|---|---|---|
| | RxRTS CONTROL | RxINT SELECT | ERROR MODE | PARITY MODE | PARITY TYPE | BITS PER CHARACTER |
| MR1A MR1B | 0 = No<br>1 = Yes | 0 = RxRDY<br>1 = FFULL | 0 = Char<br>1 = Block | 00 = With Parity<br>01 = Force Parity<br>10 = No Parity<br>11 = Multidrop Mode | 0 = Even<br>1 = Odd | 00 = 5<br>01 = 6<br>10 = 7<br>11 = 8 |

| | BIT 7 BIT 6 | BIT 5 | BIT 4 | BIT 3 BIT 2 BIT 1 BIT 0 | | | |
|---|---|---|---|---|---|---|---|
| | CHANNEL MODE | TxRTS CONTROL | CTS ENABLE Tx | STOP BIT LENGTH* | | | |
| MR2A MR2B | 00 = Normal<br>01 = Auto-Echo<br>10 = Local loop<br>11 = Remote loop | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = 0.563<br>1 = 0.625<br>2 = 0.688<br>3 = 0.750 | 4 = 0.813<br>5 = 0.875<br>6 = 0.938<br>7 = 1.000 | 8 = 1.563<br>9 = 1.625<br>A = 1.688<br>B = 1.750 | C = 1.813<br>D = 1.875<br>E = 1.938<br>F = 2.000 |

NOTE:
*Add 0.5 to values shown for 0 - 7 if channel is programmed for 5 bits/char.

| | BIT 7 BIT 6 BIT 5 BIT 4 | BIT 3 BIT 2 BIT 1 BIT 0 |
|---|---|---|
| | RECEIVER CLOCK SELECT | TRANSMITTER CLOCK SELECT |
| CSRA CSRB | See Text | See Text |

| | BIT 7 BIT 6 BIT 5 BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|
| | MISCELLANEOUS COMMANDS | DISABLE Tx | ENABLE Tx | DISABLE Rx | ENABLE Rx |
| CRA CRB | See Text | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | RECEIVED BREAK* | FRAMING ERROR* | PARITY ERROR* | OVERRUN ERROR | TxEMT | TxRDY | FFULL | RxRDY |
| SRA SRB | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 BIT 2 | BIT 1 BIT 0 |
|---|---|---|---|---|---|---|
| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 |
| OPCR | 0 = OPR[7]<br>1 = TxRDYB | 0 = OPR[6]<br>1 = TxRDYA | 0 = OPR[5]<br>1 = RxRDY/ FFULLB | 0 = OPR[4]<br>1 = RxRDY/ FFULLA | 00 = OPR[3]<br>01 = C/T OUTPUT<br>10 = TxCB(1x)<br>11 = RxCB(1x) | 11 = OPR[2]<br>01 = TxCA(16x)<br>10 = TxCA(1x)<br>11 = RxCA(1x) |

**Table 2. Register Bit Formats** (Continued)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | BRG SET SELECT | COUNTER/TIMER MODE AND SOURCE | | | DELTA IP3 INT | DELTA IP2 INT | DELTA IP1 INT | DELTA IP0 INT |
| ACR | 0 = set 1<br>1 = set 2 | See Table 4 | | | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | DELTA IP3 | DELTA IP2 | DELTA IP1 | DELTA IP0 | IP3 | IP2 | IP1 | IP0 |
| IPCR | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High | 0 = Low<br>1 = High |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | INPUT PORT CHANGE | DELTA BREAK B | RxRDY/ FFULLB | TxRDYB | COUNTER READY | DELTA BREAK A | RxRDY/ FFULLA | TxRDYA |
| ISR | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes | 0 = No<br>1 = Yes |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | IN. PORT CHANGE INT | DELTA BREAK B INT | RxRDY/ FFULLB INT | TxRDYB INT | COUNTER READY INT | DELTA BREAK A INT | RxRDY/ FFULLA INT | TxRDYA INT |
| IMR | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On | 0 = Off<br>1 = On |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | C/T[15] | C/T[14] | C/T[13] | C/T[12] | C/T[11] | C/T[10] | C/T[9] | C/T[8] |
| CTUR | | | | | | | | |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | C/T[7] | C/T[6] | C/T[5] | C/T[4] | C/T[3] | C/T[2] | C/T[1] | C/T[0] |
| CTLR | | | | | | | | |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | IVR[7] | IVR[6] | IVR[5] | IVR[4] | IVR[3] | IVR[2] | IVR[1] | IVR[0] |
| IVR | | | | | | | | |

## CSRA – Channel A Clock Select Register

**CSRA[7:4] – Channel A Receiver Clock Select**
This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

**CSRA[3:0] – Channel A Transmitter Clock Select**
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

| CSRA[3:0] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 1110 | IP3-16X | IP3-16X |
| 1111 | IP3-1X | IP3-1X |

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

**Table 3. Baud Rate Clock = 3.6864 MHz**

| CSRA[7:4] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 0000 | 50 | 75 |
| 0001 | 110 | 110 |
| 0010 | 134.5 | 134.5 |
| 0011 | 200 | 150 |
| 0100 | 300 | 300 |
| 0101 | 600 | 600 |
| 0110 | 1,200 | 1,200 |
| 0111 | 1,050 | 2,000 |
| 1000 | 2,400 | 2,400 |
| 1001 | 4,800 | 4,800 |
| 1010 | 7,200 | 1,800 |
| 1011 | 9,600 | 9,600 |
| 1100 | 38.4k | 19.2k |
| 1101 | Timer | Timer |
| 1110 | IP4-16X | IP4-16X |
| 1111 | IP4-1X | IP4-1X |

**NOTE:** The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

## CSRB – Channel B Clock Select Register

**CSRB[7:4] – Channel B Receiver Clock Select**
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

| CSRB[7:4] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 1110 | IP2-16X | IP2-16X |
| 1111 | IP2-1X | IP2-1X |

The transmitter clock is always a 16X clock except for CSRB[7:4] = 1111.

**CSRB[3:0] – Channel B Transmitter Clock Select**
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

| CSRB[3:0] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 1110 | IP5-16X | IP5-16X |
| 1111 | IP5-1X | IP5-1X |

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

## CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

**CRA[6:4] – Miscellaneous Commands**
The encoded value of this field may be used to specify a single command as follows:

| CRA[6:4] | COMMAND |
|---|---|
| 000 | No command. |
| 001 | Reset MR pointer. Causes the Channel A MR pointer to point to MR1. |
| 010 | Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed. |
| 011 | Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied. |
| 100 | Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received. |
| 101 | Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero. |
| 110 | Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted. |
| 111 | Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted. |

**CRA[3] – Disable Channel A Transmitter**
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

**CRA[2] – Enable Channel A Transmitter**
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

**CRA[1] – Disable Channel A Receiver**
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

**CRA[0] – Enable Channel A Receiver**
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

## CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.,

## SRA – Channel A Status Register

**SRA[7] – Channel A Received Break**
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

**SRA[6] – Channel A Framing Error**
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

**SRA[5] – Channel A Parity Error**
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

**SRA[4] – Channel A Overrun Error**
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

**SRA[3] – Channel A Transmitter Empty (TxEMTA)**
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

**SRA[2] – Channel A Transmitter Ready (TxRDYA)**
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

**SRA[1] – Channel A FIFO Full (FFULLA)**
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

**SRA[0] – Channel A Receiver Ready (RxRDYA)**
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

## SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## OPCR – Output Port Configuration Register

**OPCR[7] – OP7 Output Select**
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[6] – OP6 Output Select**
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[5] – OP5 Output Select**
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[4] – OP4 Output Select**
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[3:2] – OP3 Output Select**
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

**OPCR[1:0] – OP2 Output Select**
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

## ACR – Auxiliary Control Register

**ACR[7] – Baud Rate Generator Set Select**
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

**Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz**

| NORMAL RATE (BAUD) | ACTUAL 16x CLOCK (kHz) | ERROR (%) |
|---|---|---|
| 50 | 0.8 | 0 |
| 75 | 1.2 | 0 |
| 110 | 1.759 | -0.069 |
| 134.5 | 2.153 | 0.059 |
| 150 | 2.4 | 0 |
| 200 | 3.2 | 0 |
| 300 | 4.8 | 0 |
| 600 | 9.6 | 0 |
| 1050 | 16.756 | -0.260 |
| 1200 | 19.2 | 0 |
| 1800 | 28.8 | 0 |
| 2000 | 32.056 | 0.175 |
| 2400 | 38.4 | 0 |
| 4800 | 76.8 | 0 |
| 7200 | 115.2 | 0 |
| 9600 | 153.6 | 0 |
| 19.2k | 307.2 | 0 |
| 38.4k | 614.4 | 0 |

**NOTE:**
Duty cycle of 16x clock is 50% ± 1%.

**ACR[6:4] – Counter/Timer Mode And Clock Source Select**
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

**Table 5. ACR 6:4 Field Definition**

| ACR [6:4] | MODE | CLOCK SOURCE |
|---|---|---|
| 000 | Counter | External (IP2)* |
| 001 | Counter | TxCA – 1x clock of Channel A transmitter |
| 010 | Counter | TxCB – 1x clock of Channel B transmitter |
| 011 | Counter | Crystal or external clock (x1/CLK) divided by 16 |
| 100 | Timer | External (IP2)* |
| 101 | Timer | External (IP2) divided by 16* |
| 110 | Timer | Crystal or external clock (X1/CLK) |
| 111 | Timer | Crystal or external clock (X1/CLK) divided by 16 |

**NOTE:**
* In these modes, the Channel B receiver clock should normally be generated from the baud rate generator.

**ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable**
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

## IPCR – Input Port Change Register

**IPCR[7] – IP3, IP2, IP1, IP0 Change-of-State**
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

**IPCR[3:0] – IP3, IP2, IP1, IP0 Current State**
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

## ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to $00_{16}$ when the DUART is reset.

**ISR[7] – Input Port Change Status**
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

**ISR[6] – Channel B Change In Break**
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

**ISR[5] – Channel B Receiver Ready or FIFO Full**
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

**ISR[4] – Channel B Transmitter Ready**
This bit is a duplicate of TxRDYB (SRB[2]).

**ISR[3] – Counter Ready.**
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

**ISR[2] – Channel A Change In Break**
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

**ISR[1] – Channel A Receiver Ready Or FIFO Full**
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

**ISR[0] – Channel A Transmitter Ready**
This bit is a duplicate of TxRDYA (SRA[2]).

## IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

### CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is $0002_{16}$. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A4-A1 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR. The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A4-A1 = 1111). The command, however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

On power-up and after reset, the counter/timer runs in timer mode and can only be restarted. Because it cannot be shut off or stopped, and runs continuously in timer mode, it is recommended that at initialization, the output port, OP3, should be masked off through the OPCR[3:2] = 00 until the C/T is programmed to the desired operational state.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count $0000_{16}$, the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

### IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

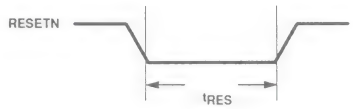



Figure 1. Reset Timing

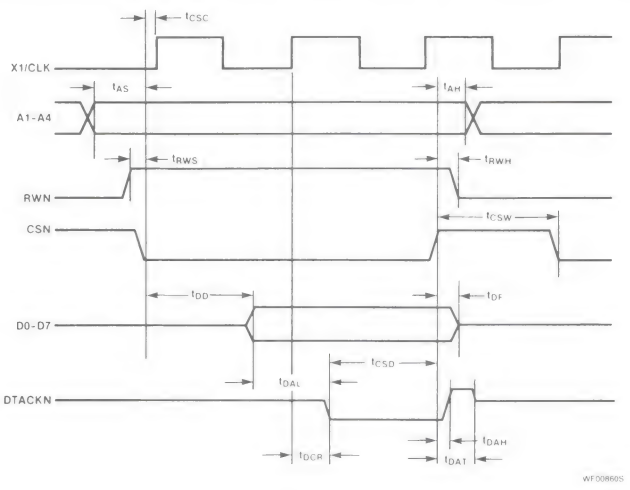



Figure 2. Bus Timing (Read Cycle)

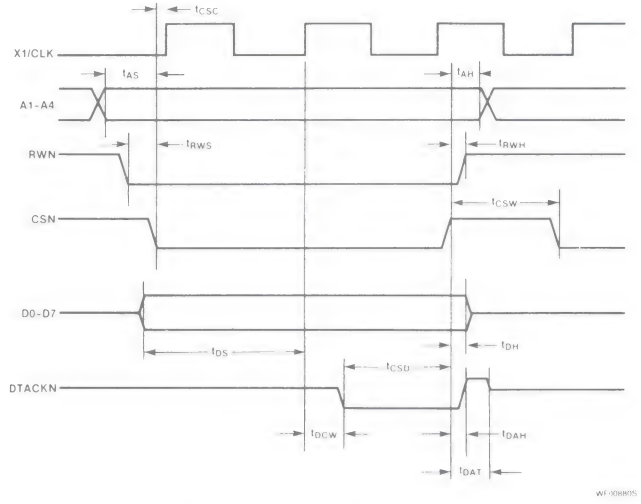



Figure 3. Bus Timing (Write Cycle)

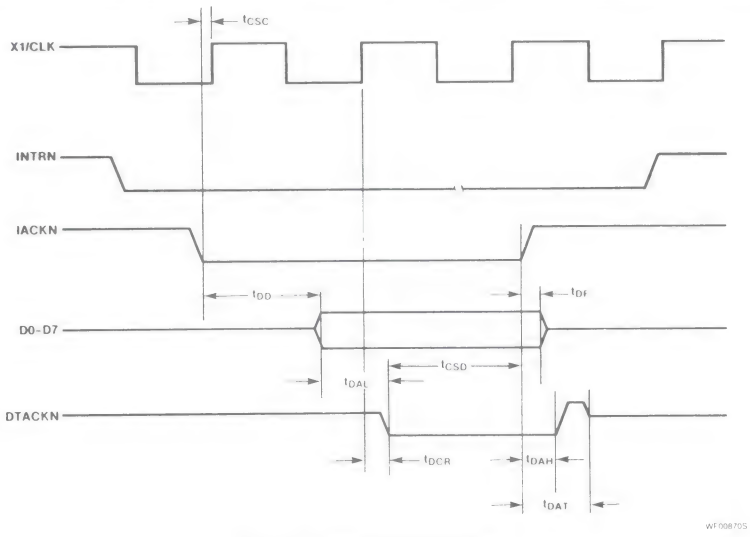



Figure 4. Interrupt Cycle Timing

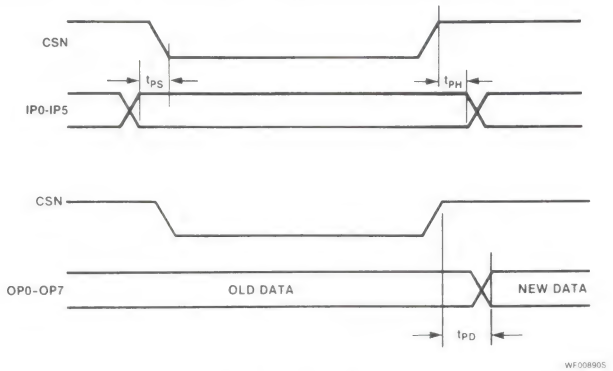
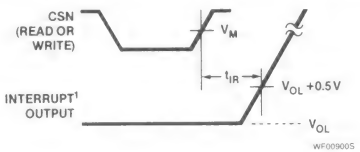



Figure 5. Port Timing




NOTES:
1. INTRN or OP3 - OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, $V_M$, to a point 0.5 volts above $V_{OL}$. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 6. Interrupt Timing

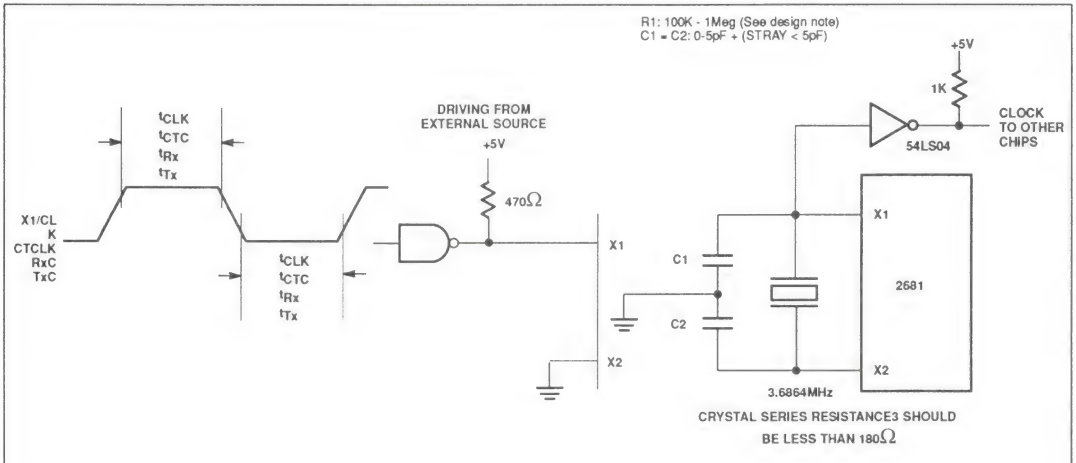



Figure 7. Clock Timing

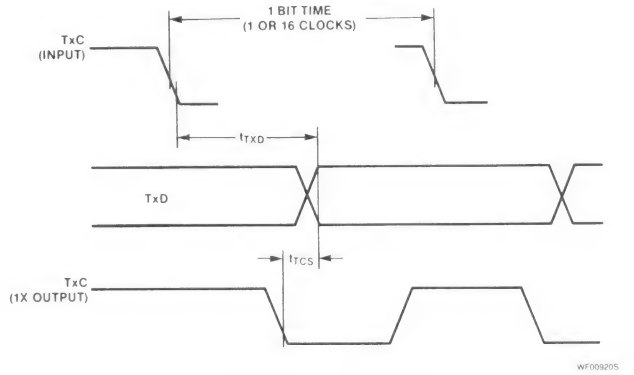



Figure 8. Transmit Timing

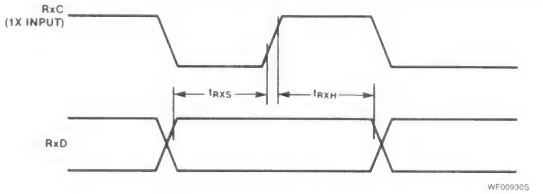
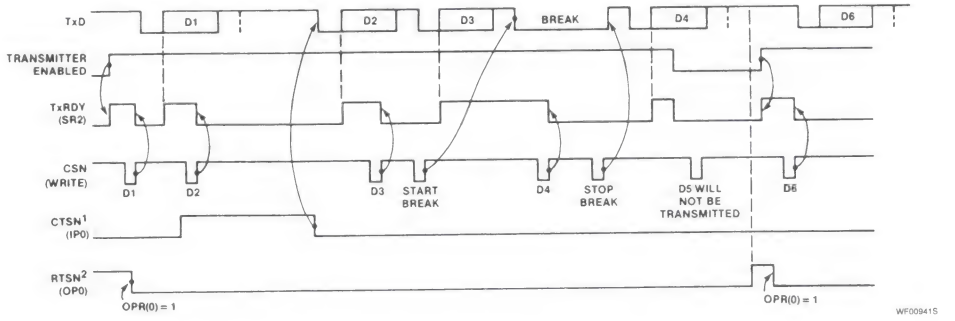
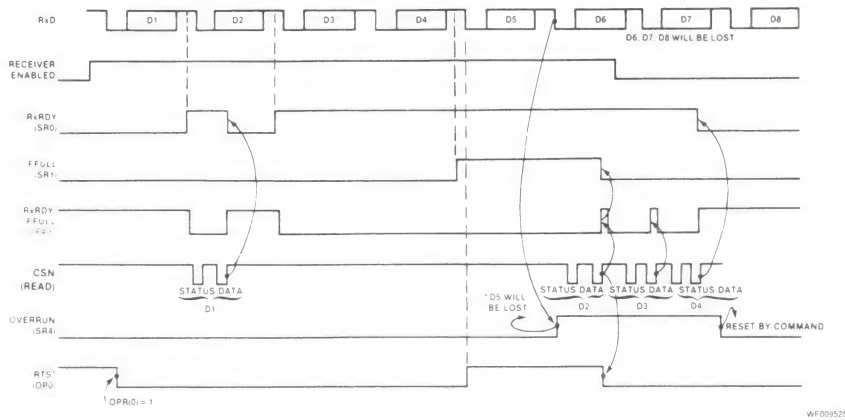



Figure 9. Receive Timing




NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 10. Transmitter Timing




NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

Figure 11. Receiver Timing

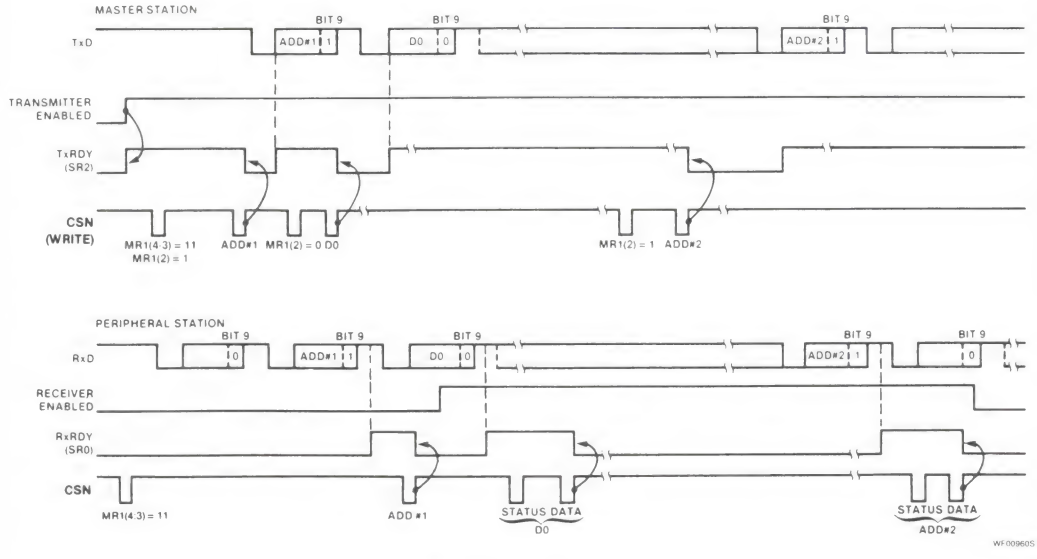



Figure 12. Wake-Up Mode

Signetics

# 68692
## Dual Asynchronous Receiver/Transmitter (DUART)

*Objective Specification*

**Military Microprocessor Products**

### DESCRIPTION

The Signetics 68692 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other 68000 family devices and can also interface easily with other microprocessors. The DUART can be used in a polled or interrupt driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

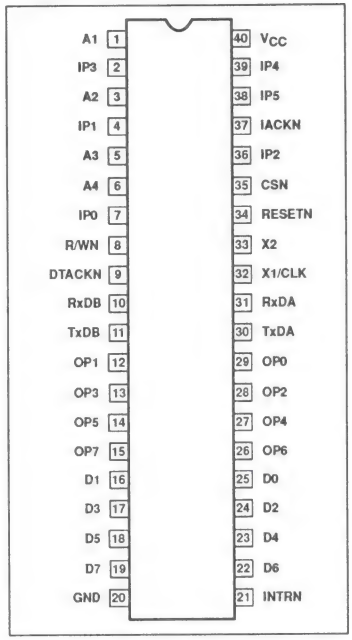
Also provided on the 68692 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

Order codes for this device are listed in the Ordering Information table.

### FEATURES

- 68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multifunction 6-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multifunction 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge

### PIN CONFIGURATION



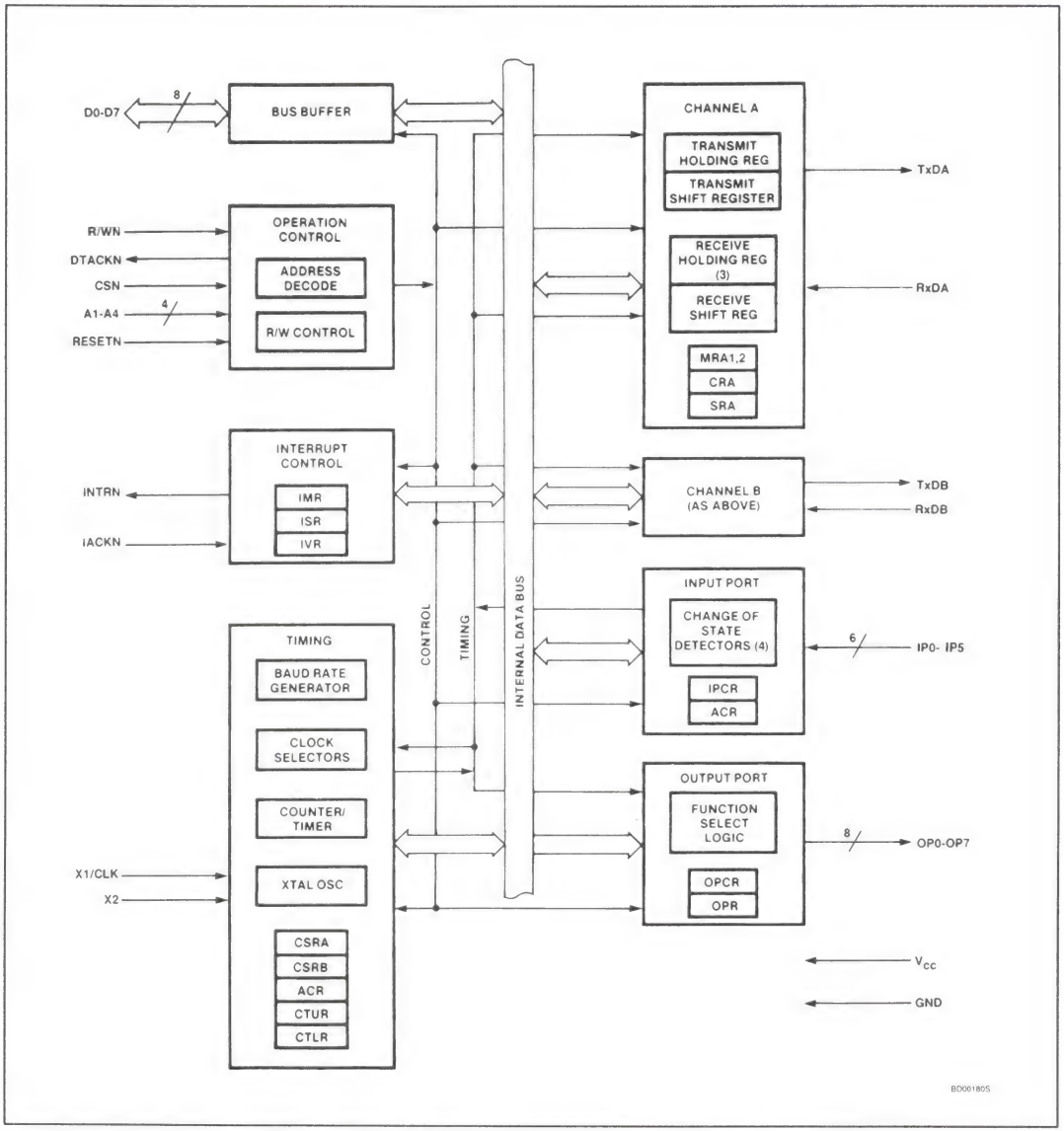

  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- TTL compatible
- Single +5V power supply

# Dual Asynchronous Receiver/Transmitter (DUART) 68692

## ORDERING INFORMATION

| PACKAGE | ORDER CODE |
|---|---|
| 40–Pin Ceramic DIP | 68692/BQA |

## BLOCK DIAGRAM



# Dual Asynchronous Receiver/Transmitter (DUART) 68692

## PIN DESCRIPTION

| SYMBOL | PIN NO. | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| D0–D7 | 25,16,24,17 23,18,22,19 | I/O | **Data Bus:** Bidirectional 3–State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit. |
| CSN | 35 | I | **Chip Enable:** Active–Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A1–A4 inputs. When CEN is High, the DUART places the D0–D7 lines in the 3–State condition. |
| R/WN | 8 | I | **Read/Write:** A High input indicates a read cycle and a low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input. |
| A1–A4 | 1,2,5,6 | I | **Address Inputs:** Select the DUART internal registers and ports for read/write operations. |
| RESETN | 34 | I | **Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. |
| $\overline{\text{DTACKN}}$ | 9 | O | **Data Transfer Acknowledge:** 3–State active–Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART. |
| INTRN | 21 | O | **Interrupt Request:** Active–Low, open–drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true. |
| IACKN | 37 | I | **Interrupt Acknowledge:** Active–Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending. |
| X1/CLK | 32 | I | **Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). |
| X2 | 33 | I | **Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin can be left open. |
| RxDA | 31 | I | **Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low. |
| RxDB | 10 | I | **Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low. |
| TxDA | 30 | O | **Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low. |
| TxDB | 11 | O | **Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low. |
| OP0 | 29 | O | **Output 0:** General purpose output or Channel A request to send (RTSAN, active–Low). Can be deactivated automatically on receive or transmit. |
| OP1 | 12 | O | **Output 1:** General purpose output or Channel B request to send (RTSBN, active–Low). Can be deactivated automatically on receive or transmit. |
| OP2 | 28 | O | **Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output. |
| OP3 | 13 | O | **Output 3:** General purpose output or open–drain, active–Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output. |
| OP4 | 27 | O | **Output 4:** General purpose output or Channel A open–drain, active–Low, RxRDYAN/FFULLAN output. |
| OP5 | 14 | O | **Output 5:** General purpose output or Channel B open–drain, active–Low, RxRDYBN/FFULLBN output. |
| OP6 | 26 | O | **Output 6:** General purpose output or Channel A open–drain, active–Low, TxRDYAN output. |
| OP7 | 15 | O | **Output 7:** General purpose output or Channel B open–drain, active–Low, TxRDYBN output. |
| IP0 | 7 | I | **Input 0:** General purpose input or Channel A clear to send active–Low input (CTSAN). |
| IP1 | 4 | I | **Input 1:** General purpose input or Channel B clear to send active–Low input (CTSBN). |
| IP2 | 36 | I | **Input 2:** General purpose input or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When external clock is used by the receiver, the received data is sampled on the rising edge of the clock. |
| IP3 | 2 | I | **Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. |
| IP4 | 39 | I | **Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. |
| IP5 | 38 | I | **Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. |
| $V_{CC}$ | 40 | I | **Power Supply:** +5V supply input. |
| GND | 20 | I | **Ground** |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Operating ambient temperature range | –55 to +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_{CC}$ | Voltage from $V_{CC}$ to GND[2] | –0.5 to +7.0 | V |
| $V_S$ | Voltage from any pin to GND[2] | –0.5 to $V_{CC}$ +0.5 | V |
| $P_D$ | Power dissipation | 750 | mW |

## DC ELECTRICAL CHARACTERISTICS[3, 4, 6] $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[5] | Max | |
| $V_{IL}$<br>$V_{IH}$<br>$V_{IH}$ | Input Low voltage<br>Input High voltage (except X1/CLK)<br>Input High voltage (X1/CLK) | | <br>2.0<br>0.8 $V_{CC}$ | | 0.8 | V<br>V<br>v |
| $V_{OL}$<br>$V_{OH}$ | Output Low voltage<br>Output High voltage (except OD outputs)[6] | $I_{OL}$ = 2.4mA<br>$I_{OH}$ = –400µA | <br>$V_{CC}$ –0.5 | | 0.4 | V<br>V |
| $I_{IX1PD}$<br>$I_{ILX1}$<br>$I_{IHX1}$ | X1/CLK input current – power down<br>X1/CLK input Low current – operating<br>X1/CLK input High current – operating | $V_{IN}$ = 0 to $V_{CC}$<br>$V_{IN}$ = 0<br>$V_{IN}$ = $V_{CC}$ | –10<br>–75<br>0 | | +10<br>0<br>75 | µA<br>µA<br>µA |
| $I_{OHX2}$<br>$I_{OHX2S}$<br>$I_{OLX2}$<br>$I_{OLX2S}$ | X2 output High current – operating<br>X2 output High short circuit current – operating<br>X2 output Low current – operating<br>X2 output Low short circuit current – operating and power down | $V_{OUT}$ = $V_{CC}$, X1 = 0<br>$V_{OUT}$ = 0, X1 = 0<br>$V_{OUT}$ = 0, X1 = $V_{CC}$<br>$V_{OUT}$ = $V_{CC}$, X1 = $V_{CC}$ | 0<br>–10<br>–75<br>1 | | +75<br>–1<br>0<br>10 | µA<br>mA<br>µA<br>mA |
| $I_I$ | Input leakage current:<br>All except input port pins<br>Input port pins | <br>$V_{IN}$ = 0 to $V_{CC}$<br>$V_{IN}$ = 0 to $V_{CC}$ | <br>–10<br>–20 | | <br>+10<br>+10 | <br>µA<br>µA |
| $I_{OZH}$<br>$I_{OZL}$ | Output Off current High, 3–State data bus<br>Output Off current Low, 3–State data bus | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = 0V | <br>–10 | | 10 | µA<br>µA |
| $I_{ODL}$<br>$I_{ODH}$ | Open–drain output Low current in Off–State<br>Open–drain output High current in Off–State | $V_{IN}$ = 0<br>$V_{IN}$ = $V_{CC}$ | –10 | | <br>10 | µA<br>µA |
| $I_{CC}$ | Power supply current[7]<br>Operating mode<br><br>Power down mode | <br>TTL input levels<br>CMOS input levels<br>TTL input levels<br>CMOS input levels | | <br>10<br>10<br>3.0<br>2.0 | | <br>mA<br>mA<br>mA<br>mA |

## AC CHARACTERISTICS[3, 4, 6]

| SYMBOL | FIGURE | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[5] | Max | |
| **Reset Timing** | | | | | | |
| $t_{RES}$ | 1 | RESET pulse width | 1.0 | | | µs |
| **Bus Timing[8]** | | | | | | |
| $t_{AS}$ | 2,3,4 | A1–A4 setup time to CSN Low | 10 | | | ns |
| $t_{AH}$ | 2,3,4 | A1–A4 hold time from CSN Low | 100 | | | ns |
| $t_{RWS}$ | 2,3,4 | RWN setup time to CSN High | 0 | | | ns |
| $t_{RWH}$ | 2,3,4 | RWN holdup time to CSN High | 0 | | | ns |
| $t_{CSW}$[8] | 2,3,4 | CSN High pulse width | 160 | | | ns |
| $t_{CSD}$[9] | 2,3,4 | CSN or IACKN High from DTACKN Low | 20 | | | ns |
| $t_{DD}$ | 2,3,4 | Data valid from CSN or IACKN Low | | | 175 | ns |
| $t_{DA}$ | 2 | RDN Low to data bus active[11] | 15 | | | ns |
| $t_{DF}$ | 2,3,4 | Data bus floating from CSN or IACKN High[11] | | | 125 | ns |
| $t_{DI}$ | 2 | RDN High to data bus invalid[11] | 20 | | | ns |
| $t_{DS}$ | 2,3,4 | Data setup time to CLK High | 100 | | | ns |
| $t_{DH}$ | 2,3,4 | Data hold time from CSN High | 0 | | | ns |
| $t_{DAL}$ | 2,3,4 | DTACKN Low from read data valid | 0 | | | ns |
| $t_{DCR}$ | 2,3,4 | DTACKN Low (read cycle) from CLK High | | | 125 | ns |
| $t_{DCW}$ | 2,3,4 | DTACKN Low (write cycle) form CLK High | | | 125 | ns |
| $t_{DAH}$ | 2,3,4 | DTACKN High from CSN or IACKN High | | | 100 | ns |
| $I_{DAT}$ | 2,3,4 | DTACKN High impedance from CSN or IACKN High | | | 125 | ns |
| $t_{CSC}$[10] | 2,3,4 | CSN or IACKN setup time to clock High | 90 | | | ns |
| **Port Timing[8]** | | | | | | |
| $t_{PS}$ | 5 | Port input setup time to CSN Low | 0 | | | ns |
| $t_{PH}$ | 5 | Port input hold time from CSN High | 0 | | | ns |
| $t_{PD}$ | 5 | Port output valid from CSN High | | | 400 | ns |
| **Interrupt Timing** | | | | | | |
| $t_{IR}$ | 6 | INTRN (or OP3–OP7 when used as interrupts) negated from: | | | | |
| | | Read RHR (RxRDY/FFULL interrupt) | | | 300 | ns |
| | | Write THR (TxRDY interrupt) | | | 300 | ns |
| | | Reset command (break interrupt) | | | 300 | ns |
| | | Stop C/T command (counter interrupt) | | | 300 | ns |
| | | Read IPCR (input port change interrupt) | | | 300 | ns |
| | | Write IMR (clear of interrupt mask bit) | | | 300 | ns |
| **Clock Timing** | | | | | | |
| $t_{CLK}$ | 7 | X1/CLK High or Low time | 100 | | | ns |
| $f_{CLK}$ | 7 | X1/CLK frequency | 2 | 3.6864 | 4 | MHz |
| $t_{CTC}$ | 7 | CTCLK (IP2) High or Low time | 100 | | | ns |
| $f_{CTC}$ | 7 | CTCLK (IP2) frequency[12] | 100 | | 4 | MHz |
| $t_{RX}$ | 7 | RxC High or Low time | 220 | | | ns |
| $f_{RX}$ | 7 | RxC frequency (16X)[12] | 100 | | 2 | MHz |
| | | (1X)[12] | 100 | | 1 | MHz |
| $t_{TX}$ | 7 | TxC High or Low time | 220 | | | ns |
| $f_{TX}$ | 7 | TxC frequency (16X)[12] | 0 | | 2 | MHz |
| | | (1X)[12] | 0 | | 1 | MHz |
| **Transmitter Timing** | | | | | | |
| $t_{TXD}$ | 8 | TxD output delay from TxC Low | | | 350 | ns |
| $t_{TCS}$ | 8 | Output delay from TxC Low to TxD data output | | | 150 | ns |
| **Receiver Timing** | | | | | | |
| $t_{RXS}$ | 9 | RxD data setup time to RxC High | 240 | | | ns |
| $t_{RXH}$ | 9 | RxD data hold time from RxC High | 200 | | | ns |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
3. Parameters are valid over specified temperature range.
4. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
5. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
6. Test conditions for outputs: $C_L$ = 150pF, except interrupt outputs. Test condition for interrupt outputs: $C_L$ = 50pF, $R_L$ = 2.7kΩ to $V_{CC}$.
7. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of $V_{CC}$ –0.2V and $V_{SS}$ + 0.2V.
8. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
9. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
10. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.
11. Guaranteed by characterization of sample units.
12. Minimum frequencies are not tested but are guaranteed by design.

# Dual Asynchronous Receiver/Transmitter (DUART) 68692

## BLOCK DIAGRAM

The 68692 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

### Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

### Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

### Interrupt Control

A single active–Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auxiliary Control Register (ACR), and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR register on the data bus and asserting DTACKN.

Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

### Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16–bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

### Communications Channels A and B

Each communications channel of the 68692 comprises a full–duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

### Input Port

The inputs to this unlatched 6–bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always be read as a logic 1 and D6 will reflect the level of IACKN. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change–of–state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High–to–Low or Low–to–High transition of these inputs, lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change–of–state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change–of–state is "just missed" and the first change–of–state is not detected until 25µs later.

### Output Port

The 8–bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also be individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

## OPERATION

### Transmitter

The 68692 is conditioned to transmit data when the transmitter is enabled through the command register. The 68692 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are ne-

gated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

## Receiver

The 68692 is conditioned to receive data when enabled through the command register. The receiver looks for a High–to–Low (mark–to–space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7–1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non–zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one–half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one–half bit time before a search for the next start bit begins.

The RHR consists of a First–In–First–Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character–by–character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical–OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set–upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re–asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

## Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR,

the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

### Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

## PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

**Table 1. Register Addressing**

| A3 | A2 | A1 | A0 | READ (RDN = 0) | WRITE (WRN = 0) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Mode Register A (MR1A, MR2A) | Mode Register A (MR1A, MR2A) |
| 0 | 0 | 0 | 1 | Status Register A (SRA) | Clock Select Register A (CSRA) |
| 0 | 0 | 1 | 0 | Reserved | Command Register A (CRA) |
| 0 | 0 | 1 | 1 | Rx Holding Register A (RHRA) | Tx Holding Register A (THRA) |
| 0 | 1 | 0 | 0 | Input Port Change Register (IPCR) | Aux. Control Register (ACR) |
| 0 | 1 | 0 | 1 | Interrupt Status Register (ISR) | Interrupt Mask Register (IMR) |
| 0 | 1 | 1 | 0 | Counter/Timer Upper (CTU) | C/T Upper Register (CRUR) |
| 0 | 1 | 1 | 1 | Counter/Timer Lower (CTL) | C/T Lower Register (CTLR) |
| 1 | 0 | 0 | 0 | Mode Register B (MR1B, MR2B) | Mode Register B (MR1B, MR2B) |
| 1 | 0 | 0 | 1 | Status Register B (SRB) | Clock Select Register B (CSRB) |
| 1 | 0 | 1 | 0 | Reserved | Command Register B (CRB) |
| 1 | 0 | 1 | 1 | Rx Holding Register B (RHRB) | Tx Holding Register B (THRB) |
| 1 | 1 | 0 | 0 | Reserved | Interrupt Vector Register (IVR) |
| 1 | 1 | 0 | 1 | Input Port | Output Port Conf. Register (OPCR) |
| 1 | 1 | 1 | 0 | Start Counter Command | Set Output Port Bits Command |
| 1 | 1 | 1 | 1 | Stop Counter Command | Reset Output Port Bits Command |

## MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

**MR1A[7] – Channel A Receiver Request–to–Send Control**

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

**MR1A[6] – Channel A Receiver Interrupt Select**

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

**MR1A[5] – Channel A Error Mode Select**

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character–by–character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical–OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

**MR1A[4:3] – Channel A Parity Mode Select**

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

**MR1A[2] – Channel A Parity Type Select**

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

**MR1A[1:0] – Channel A Bits Per Character Select**

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

## MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

**MR2A[7:6] – Channel A Mode Select**

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de–selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

**MR2A[5] – Channel A Transmitter Request–to–Send Control**

This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto–reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

## Table 2. Register Bit Formats

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 BIT 3 | BIT 2 | BIT 1 BIT 0 |
|---|---|---|---|---|---|---|
| | RxRTS CONTROL | RxINT SELECT | ERROR MODE | PARITY MODE | PARITY TYPE | BITS PER CHARACTER |
| MR1A MR1B | 0 = No 1 = Yes | 0 = RxRDY 1 = FFULL | 0 = Char 1 = Block | 00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode | 0 = Even 1 = Odd | 00 = 5 01 = 6 10 = 7 11 = 8 |

| | BIT 7 BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| | CHANNEL MODE | TxRTS CONTROL | CTS ENABLE Tx | STOP BIT LENGTH* | | | |
| MR2A MR2B | 00 = Normal 01 = Auto–Echo 10 = Local loop 11 = Remote loop | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750 | 4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000 | 8 = 1.563 9 = 1.625 A = 1.688 B = 1.750 | C = 1.813 D = 1.875 E = 1.938 F = 2.000 |

**NOTE:**
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

| | BIT 7 BIT 6 BIT 5 BIT 4 | BIT 3 BIT 2 BIT 1 BIT 0 |
|---|---|---|
| | RECEIVER CLOCK SELECT | TRANSMITTER CLOCK SELECT |
| CSRA CSRB | See Text | See Text |

| | BIT 7 BIT 6 BIT 5 BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|
| | MISCELLANEOUS COMMANDS | DISABLE Tx | ENABLE Tx | DISABLE Rx | ENABLE Rx |
| CRA CRB | See Text | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | RECEIVED BREAK* | FRAMING ERROR* | PARITY ERROR* | OVERRUN ERROR | TxEMT | TxRDY | FFULL | RxRDY |
| SRA SRB | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes |

**NOTE:**
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 BIT 2 | BIT 1 BIT 0 |
|---|---|---|---|---|---|---|
| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 |
| OPCR | 0 = OPR[7] 1 = TxRDYB | 0 = OPR[6] 1 = TxRDYA | 0 = OPR[5] 1 = RxRDY/ FFULLB | 0 = OPR[4] 1 = RxRDY/ FFULLA | 00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x) | 11 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x) |

| | BIT 7 | BIT 6 BIT 5 BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|
| | BRG SET SELECT | COUNTER/TIMER MODE AND SOURCE | DELTA IP3 INT | DELTA IP2 INT | DELTA IP1 INT | DELTA IP0 INT |
| ACR | 0 = set 1 1 = set 2 | See Table 4 | 0 = Off 1 = On | 0 = Off 1 = On | 0 = Off 1 = On | 0 = Off 1 = On |

**Table 2. Register Bit Formats** (Continued)

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | DELTA IP3 | DELTA IP2 | DELTA IP1 | DELTA IP0 | IP3 | IP2 | IP1 | IP0 |
| IPCR | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = Low 1 = High | 0 = Low 1 = High | 0 = Low 1 = High | 0 = Low 1 = High |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | INPORT CHANGE | DELTA BREAK B | RxRDY/ FFULLB | TxRDYB | COUNTER READY | DELTA BREAK A | RxRDY/ FFULLA | TxRDYA |
| ISR | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes | 0 = No 1 = Yes |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | INPORT CHANGE INT | DELTA BREAK B INT | RxRDY/ FFULLB INT | TxRDYB INT | COUNTER READY INT | DELTA BREAK A INT | RxRDY/ FFULLA INT | TxRDYA INT |
| IMR | 0 = Off 1 = On | 0 = Off 1 = On | 0 = Off 1 = On | 0 = Off 1 = On | 0 = Off 1 = On | 0 = Off 1 = On | 0 = Off 1 = On | 0 = Off 1 = On |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | C/T[15] | C/T[14] | C/T[13] | C/T[12] | C/T[11] | C/T[10] | C/T[9] | C/T[8] |
| CTUR | | | | | | | | |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | C/T[7] | C/T[6] | C/T[5] | C/T[4] | C/T[3] | C/T[2] | C/T[1] | C/T[0] |
| CTLR | | | | | | | | |

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| | IVR[7] | IVR[6] | IVR[5] | IVR[4] | IVR[3] | IVR[2] | IVR[1] | IVR[0] |
| IVR | | | | | | | | |

**MR2A[4] – Channel A Clear–to–Send Control**

If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

**MR2A[3:0] – Channel A Stop Bit Length Select**

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

## MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## CSRA – Channel A Clock Select Register

**CSRA[7:4] – Channel A Receiver Clock Select**
This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

**CSRA[3:0] – Channel A Transmitter Clock Select**
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

| CSRA[3:0] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 1110 | IP3–16X | IP3–16X |
| 1111 | IP3–1X | IP3–1X |

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

### Table 3. Baud Rate

| CSRA[7:4] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 0000 | 50 | 75 |
| 0001 | 110 | 110 |
| 0010 | 134.5 | 134.5 |
| 0011 | 200 | 150 |
| 0100 | 300 | 300 |
| 0101 | 600 | 600 |
| 0110 | 1,200 | 1,200 |
| 0111 | 1,050 | 2,000 |
| 1000 | 2,400 | 2,400 |
| 1001 | 4,800 | 4,800 |
| 1010 | 7,200 | 1,800 |
| 1011 | 9,600 | 9,600 |
| 1100 | 38.4k | 19.2k |
| 1101 | Timer | Timer |
| 1110 | IP4–16X | IP4–16X |
| 1111 | IP4–1X | IP4–1X |

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

## CSRB – Channel B Clock Select Register

**CSRB[7:4] – Channel B Receiver Clock Select**
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

| CSRB[7:4] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 1110 | IP6–16X | IP6–16X |
| 1111 | IP6–1X | IP6–1X |

The transmitter clock is always a 16X clock except for CSRB[7:4] = 1111.

**CSRB[3:0] – Channel B Transmitter Clock Select**
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

| CSRB[3:4] | ACR[7] = 0 | Baud Rate ACR[7] = 1 |
|---|---|---|
| 1110 | IP5–16X | IP5–16X |
| 1111 | IP5–1X | IP5–1X |

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

## CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non–conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

**CRA[7:4] – Miscellaneous Commands**
The encoded value of this field may be used to specify a single command as follows:

0000 No command.
0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.
1000 Assert RTSN. Causes the RTSN output to be asserted (Low).
1001 Negate RTSN. Causes the RTSN output to be negated (High).
1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.
1011 Not used.
1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued
1101 Not used.
1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only. Design Note: The part will not output DTACKN while in power down mode. Use automatic DTACKN generation.
1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

**CRA[3] – Disable Channel A Transmitter**
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

**CRA[2] – Enable Channel A Transmitter**
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

**CRA[1] – Disable Channel A Receiver**
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

**CRA[0] – Enable Channel A Receiver**
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start–bit state.

## CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non–conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

## SRA – Channel A Status Register

**SRA[7] – Channel A Received Break**
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one–half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

**SRA[6] – Channel A Framing Error**
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

**SRA[5] – Channel A Parity Error**
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In the special multidrop mode, the parity error bit stores the received A/D bit.

**SRA[4] – Channel A Overrun Error**
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a 'reset error status' command.

**SRA[3] – Channel A Transmitter Empty (TxEMTA)**
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

**SRA[2] – Channel A Transmitter Ready (TxRDYA)**
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

**SRA[1] – Channel A FIFO Full (FFULLA)**
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

**SRA[0] – Channel A Receiver Ready (RxRDYA)**
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

## SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

## OPCR – Output Port Configuration Register

**OPCR[7] – OP7 Output Select**
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open–drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[6] – OP6 Output Select**
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open–drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[5] – OP5 Output Select**
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open–drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[4] – OP4 Output Select**
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open–drain output. Note that this output is not masked by the contents of the IMR.

**OPCR[3:2] – OP3 Output Select**
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an open–drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the re-

ceived data. If data is not being received, a free running 1X clock is output.

**OPCR[1:0] – OP2 Output Select**
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

## ACR – Auxiliary Control Register

**ACR[7] – Baud Rate Generator Set Select**
This bit selects one of two sets of baud rates to be generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

**Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz**

| NORMAL BAUD RATE | ACTUAL 16x CLOCK (kHz) | ERROR (%) |
|---|---|---|
| 50 | 0.8 | 0 |
| 75 | 1.2 | 0 |
| 110 | 1.759 | –0.069 |
| 134.5 | 2.153 | 0.059 |
| 150 | 2.4 | 0 |
| 200 | 3.2 | 0 |
| 300 | 4.8 | 0 |
| 600 | 9.6 | 0 |
| 1050 | 16.756 | –0.260 |
| 1200 | 19.2 | 0 |
| 1800 | 28.8 | 0 |
| 2000 | 32.056 | 0.175 |
| 2400 | 38.4 | 0 |
| 4800 | 76.8 | 0 |
| 7200 | 115.2 | 0 |
| 9600 | 153.6 | 0 |
| 19.2k | 307.2 | 0 |
| 38.4k | 614.4 | 0 |

**NOTE:**
Duty cycle of 16x clock is 50% ± 1%.

**ACR[6:4] – Counter/Timer Mode And Clock Source Select**
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

**Table 5. ACR [6:4] Field Definition**

| [6:4] | MODE | CLOCK SOURCE |
|---|---|---|
| 000 | Counter | External (IP2) |
| 001 | Counter | TxCA – 1x clock of Channel A transmitter |
| 010 | Counter | TxCB – 1x clock of Channel B transmitter |
| 011 | Counter | Crystal or external clock (x1/CLK) divided by 16 |
| 100 | Timer | External (IP2) |
| 101 | Timer | External (IP2) divided by 16 |
| 110 | Timer | Crystal or external clock (X1/CLK) |
| 111 | Timer | Crystal or external clock (X1/CLK) divided by 16 |

**ACR[3:0] – IP3, IP2, IP1, IP0 Change–of–State Interrupt Enable**
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

## IPCR – Input Port Change Register

**IPCR[7:4] – IP3, IP2, IP1, IP0 Change–of–State**
These bits are set when a change–of–state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

**IPCR[3:0] – IP3, IP2, IP1, IP0 Change–of–State**
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

## ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to $00_{16}$ when the DUART is reset.

**ISR[7] – Input Port Change Status**
This bit is a '1' when a change–of–state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

**ISR[6] – Channel B Change In Break**
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

**ISR[5] – Channel B Receiver Ready or FIFO Full**
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

**ISR[4] – Channel B Transmitter Ready**
This bit is a duplicate of TxRDYB (SRB[2]).

**ISR[3] – Counter Ready.**
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

**ISR[2] – Channel A Change in Break**
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

**ISR[1] – Channel A Receiver Ready Or FIFO Full**
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

**ISR[0] – Channel A Transmitter Ready**
This bit is a duplicate of TxRDYA (SRA[2]).

## IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

## CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write–only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half–period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

## IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

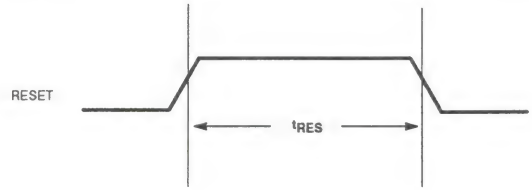



**Figure 1. Reset Timing**

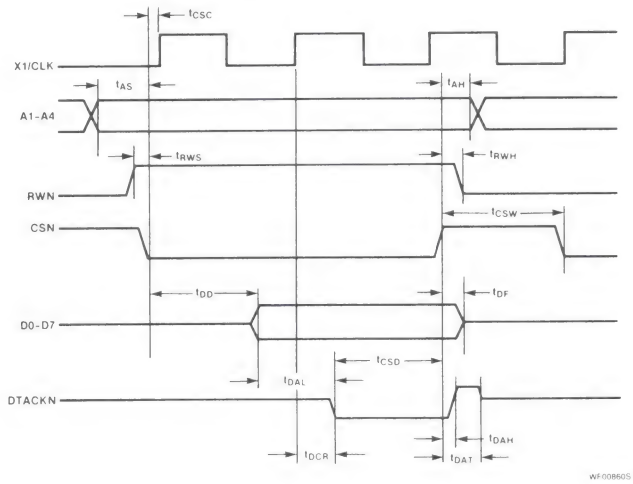



**Figure 2. Bus Timing (Read Cycle)**

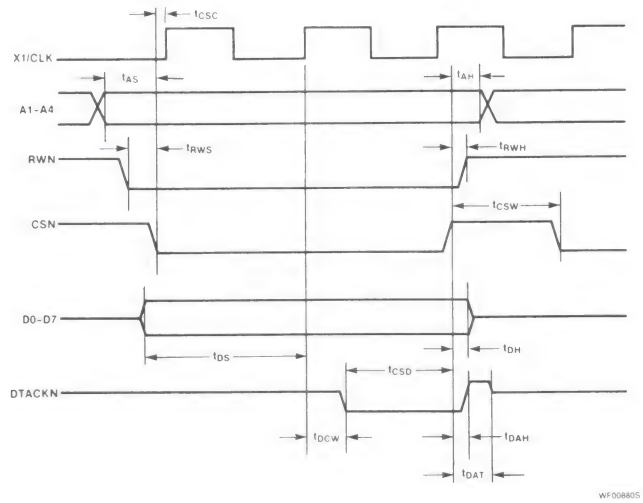



Figure 3. Bus Timing (Write Cycle)

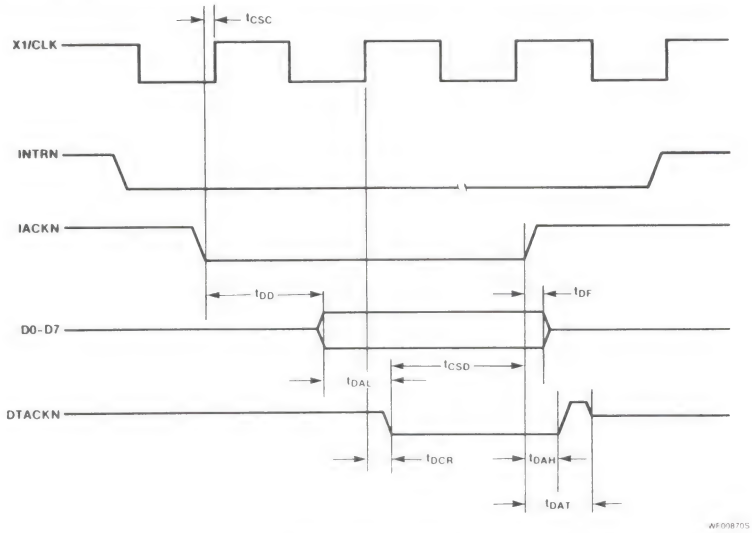



Figure 4. Interrupt Cycle Timing

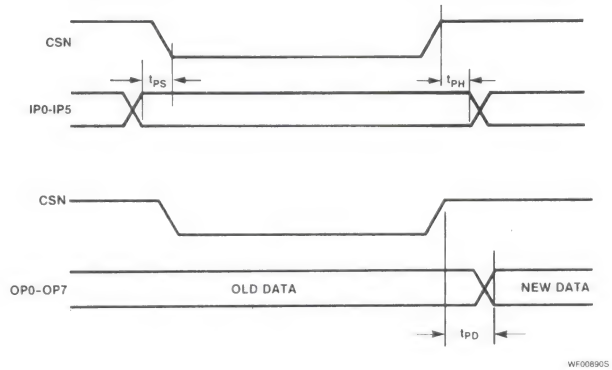
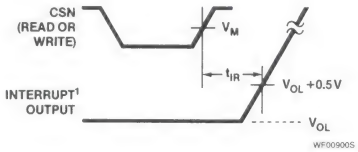



**Figure 5. Port Timing**




**NOTES:**
1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, $V_M$, to a point 0.5 volts above $V_{OL}$. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

**Figure 6. Interrupt Timing**

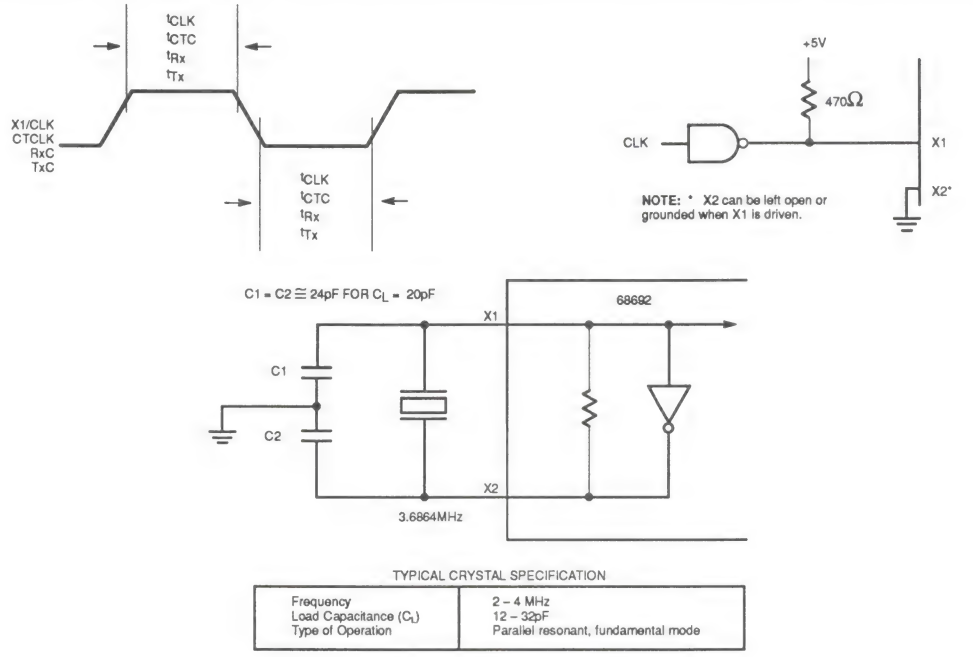



**Figure 7. Clock Timing**

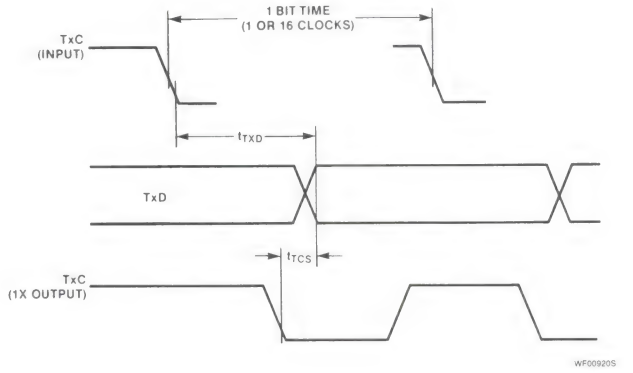



**Figure 8. Transmit Timing**

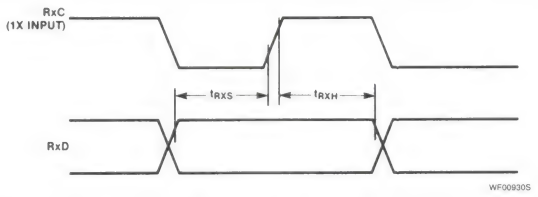
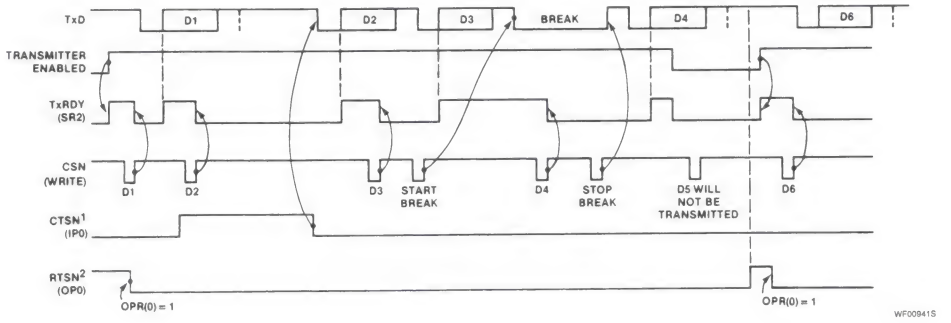
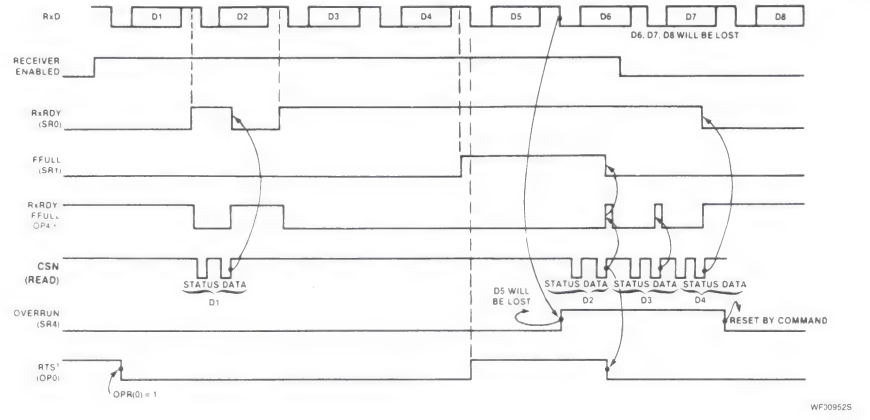



**Figure 9. Receive Timing**




NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

**Figure 10. Transmitter Timing**




NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

**Figure 11. Receiver Timing**

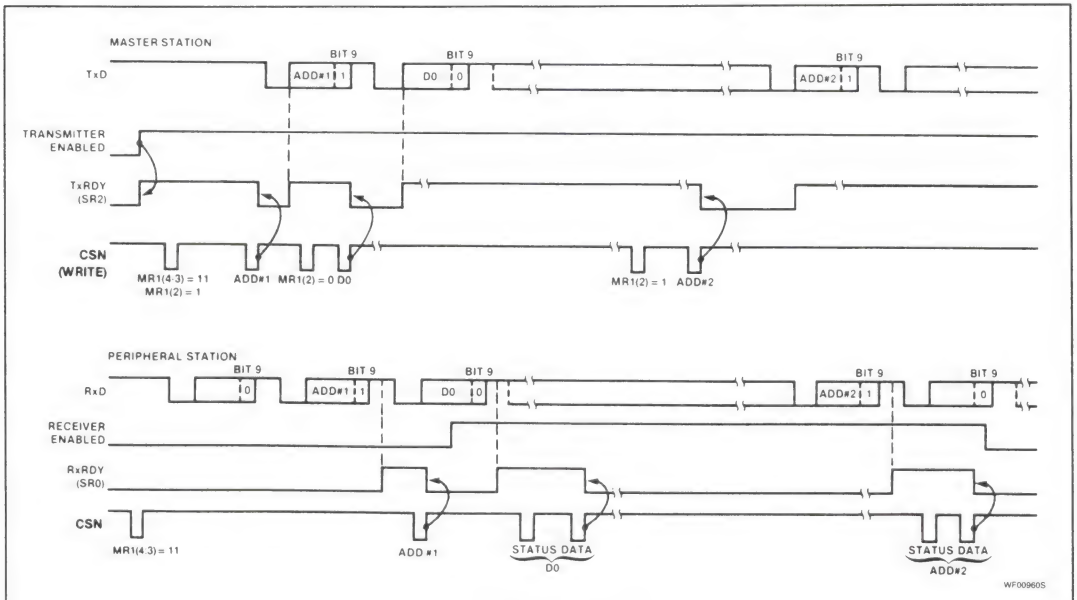



**Figure 12. Wake-Up Mode**

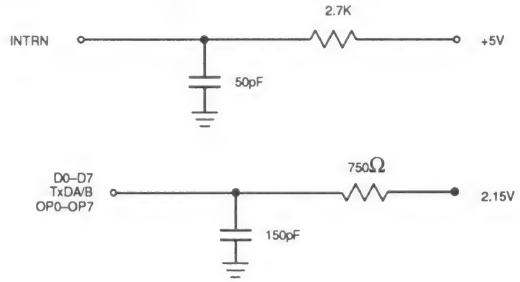



**Figure 13. Test Conditions on Outputs**

Signetics

# Section 4
# Microcontroller/ Microprocessor

Military Products

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Signetics

# 68000

## 16-/32-Bit Microprocessor

*Product Specification*

**Military**
**Customer Specific Products**

### DESCRIPTION

The 68000 is the first implementation of the 68000 16/32 bit microprocessor architecture. The 68000 has a 16-bit data bus and 24-bit address bus, while the full architecture provides for 32-bit address and data buses. It is completely code-compatible with the 68008 8-bit data bus implementation of the 68000 and is downward code-compatible with the 68010 virtual extension and the 68020 32-bit implementation of the architecture. Any user-mode programs written using the 68000 instruction set will run unchanged on the 68008, 68010, and 68020. This is possible because the user programming model is identical for all four processors and the instruction sets are proper sub-sets of the complete architecture.

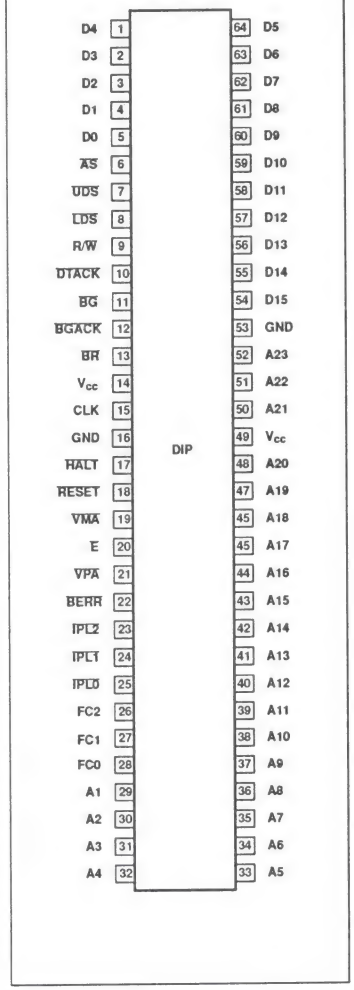
The 68000 possesses an asynchronous bus structure with a 24-bit address bus and a 16-bit data bus.

The resources available to the 68000 user consist of the following:

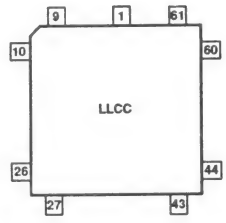
- **17 32-bit data and address registers**
- **16MB direct adressing registers**
- **56 powerful instruction types**
- **Operations on five main data types**
- **Memory-mapped I/O**
- **14 addressing modes**

As shown in the programming model (Figure 1), the 68000 offers sixteen 32-bit registers and a 32-bit program counter. The first eight registers (D0 - D7) are used as data registers for byte (8-bit), word (16-bit), and long-word (32-bit) operations. The second set of seven registers (A0 - A6) and the user stack pointer (USP) may be used as software stack pointers and base address registers. In addition, the registers may be used for word and long-word operations. All of the 16 registers may be used as index registers.

### PIN CONFIGURATION




### PIN CONFIGURATION




| LLCC Function | | LLCC Function | |
|---|---|---|---|
| 1 | D4 | 35 | A4 |
| 2 | D3 | 36 | A5 |
| 3 | D2 | 37 | A6 |
| 4 | D1 | 38 | A7 |
| 5 | D0 | 39 | A8 |
| 6 | AS | 40 | A9 |
| 7 | UDS | 41 | A10 |
| 8 | LDS | 42 | A11 |
| 9 | R/W | 43 | A12 |
| 10 | DTACK | 44 | A13 |
| 11 | BG | 45 | A14 |
| 12 | BGACK | 46 | A15 |
| 13 | BR | 47 | A16 |
| 14 | Vcc | 48 | A17 |
| 15 | CLK | 49 | A18 |
| 16 | GND | 50 | A19 |
| 17 | GND | 51 | A20 |
| 18 | NC | 52 | Vcc |
| 10 | HALT | 53 | A21 |
| 20 | RESET | 54 | A22 |
| 21 | VMA | 55 | A23 |
| 22 | E | 56 | GND |
| 23 | VPA | 57 | GND |
| 24 | BERR | 58 | D15 |
| 25 | IPL2 | 59 | D14 |
| 26 | IPL1 | 60 | D13 |
| 27 | IPL0 | 61 | D12 |
| 28 | FC2 | 62 | D11 |
| 29 | FC1 | 63 | D10 |
| 30 | FC0 | 64 | D9 |
| 31 | NC | 65 | D8 |
| 32 | A1 | 66 | D7 |
| 33 | A2 | 67 | D6 |
| 34 | A3 | 68 | D5 |

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | SPEED |
|---|---|---|
| 64-Pin Ceramic DIP 900mil-wide | 68000-6/BXA | 6MHz |
| | 68000-8/BXA | 8MHz |
| | 68000-10/BXA | 10MHz |
| 68-Pin Ceramic LLCC | 68000-6/BUC | 6MHz |
| | 68000-8/BUC | 8MHz |
| | 68000-10/BUC | 10MHz |

In supervisor mode, the upper byte of the status register and the supervisor stack pointer (SSP) are also available to the programmer. These registers are shown in Figure 2.

The status register, Figure 3, contains the interrupt mask (eight levels available) as well as the condition codes: extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

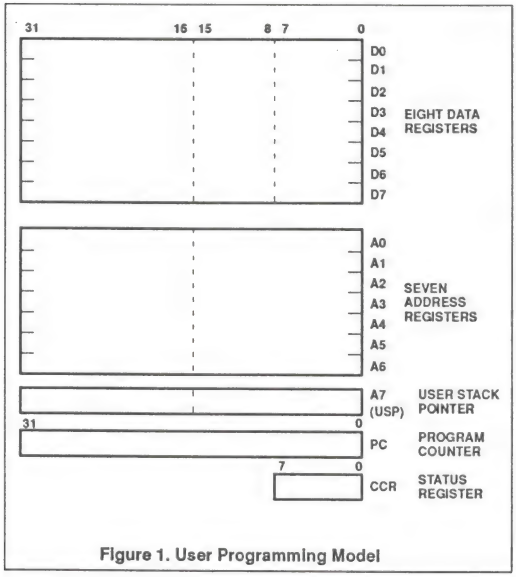



Figure 1. User Programming Model

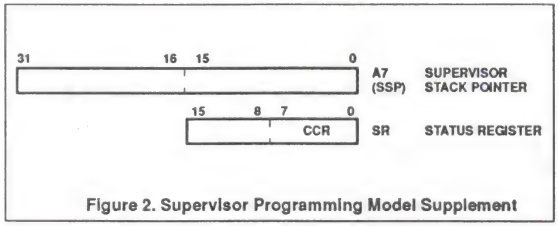



Figure 2. Supervisor Programming Model Supplement

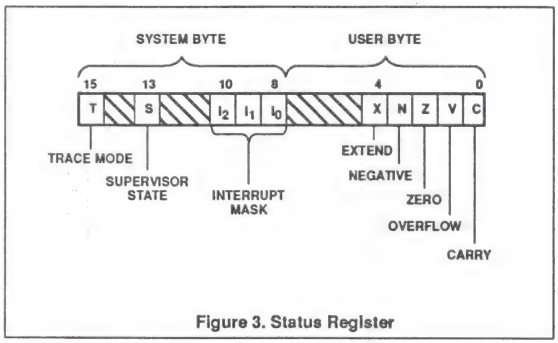



Figure 3. Status Register

## Table 1. Addressing Modes

| ADDRESSING MODES | SYNTAX |
|---|---|
| **Register direct addressing** | |
| Data register direct | Dn |
| Address register direct | An |
| **Absolute data addressing** | |
| Absolute short | xxx.W |
| Absolute long | xxx.L |
| **Program counter relative addressing** | |
| Relative with offset | $d_{16}$(PC) |
| Relative with index and offset | $d_8$(PC,Xn) |
| **Register indirect addressing** | |
| Register indirect | (An) |
| Postincrement register indirect | (An ) + |
| Predecrement register indirect | – (An) |
| Register indirect with offset | $d_{16}$(An) |
| Indexed register indirect with offset | $d_8$(An,Xn) |
| **Immediate data addressing** | |
| Immediate | #xxx |
| Quick immediate | #1 - #8 |
| **Implied addressing** | |
| Implied register | SR/USP/SP/PC |

**NOTES:**

Dn = Data register
An = Address register
Xn = Address or data register used as index register
SR = Status register
PC = Program counter
SP = Stack pointer
USP = User stack pointer
( ) = Effective Address
$d_8$ = 8-bit offset (displacement)
$d_{16}$ = 16-bit offset (displacement)
#xxx = Immediate data

## Data Types and Addressing Modes

Five basic data types are supported. These data types are:

- **Bits**
- **BCD digits (4 bits)**
- **Bytes (8 bits)**
- **Words (16 bits)**
- **Long words (32 bits)**

In addition, operations on other data types such as memory addresses, status word data, etc., are provided in the instruction set.

The 14 address modes, shown in Table 1, include six basic types:

- **Register direct**
- **Register indirect**
- **Absolute**
- **Program counter relative**
- **Immediate**
- **Implied**

Included in the register indirect addressing modes is the capability to do preincrementing, predecrementing, offsetting, and indexing. The program counter relative mode can also be modified via indexing and offsetting.

**Table 2. Instruction Set Summary**

| MNEMONIC | DESCRIPTION |
|---|---|
| ABCD | Add decimal with extend |
| ADD | Add |
| AND | Logical AND |
| ASL | Arithmetic shift left |
| ASR | Arithmetic shift right |
| $B_{CC}$ | Branch conditionally |
| BCHG | Bit test and change |
| BCLR | Bit test and clear |
| BRA | Branch always |
| BSET | Bit test and set |
| BSR | Branch to subroutine |
| BTST | Bit test |
| CHK | Check register against bounds |
| CLR | Clear operand |
| CMP | Compare |
| $DB_{CC}$ | Test condition, decrement and branch |
| DIVS | Signed divide |
| DIVU | Unsigned divide |
| EOR | Exclusive OR |
| EXG | Exchange registers |
| EXT | Sign extend |
| JMP | Jump |
| JSR | Jump to subroutine |
| LEA | Load effective address |
| LINK | Link stack |
| LSL | Logical shift left |
| LSR | Logical shift right |
| MOVE | Move source to destination |
| MULS | Signed multiply |
| MULU | Unsigned multiply |
| NBCD | Negate decimal with extend |
| NEG | Negate |
| NOP | No operation |
| NOT | One's complement |
| OR | Logical OR |
| PEA | Push effective address |
| RESET | Reset external devices |
| ROL | Rotate left without extend |
| ROR | Rotate right without extend |
| ROXL | Rotate left with extend |
| ROXR | Rotate right with extend |
| RTE | Return from exception |
| RTR | Return and restore |
| RTS | Return from subroutine |
| SBCD | Subtract decimal with extend |
| $S_{CC}$ | Set conditional |
| STOP | Stop |
| SUB | Subtract |
| SWAP | Swap data register halves |
| TAS | Test and set operand |
| TRAP | Trap |
| TRAPV | Trap on overflow |
| TST | Test |
| UNLK | Unlink |

## Instruction Set Overview

The 68000 instruction set is shown in Table 2. Some additional instructions are variations, or subsets of these, and they appear in Table 3. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned, multiply and divide, "quick" arithmetic operations, BCD arithmetic, and expanded operations (through traps).

**Table 3. Variations of Instruction Types**

| INSTRUCTION TYPE | VARIATION | DESCRIPTION |
|---|---|---|
| ADD | ADD | Add |
| | ADDA | Add address |
| | ADDQ | Add quick |
| | ADDI | Add immediate |
| | ADDX | Add with extend |
| AND | AND | Logical AND |
| | ANDI | AND immediate |
| | ANDI to CCR | AND immediate to condition codes |
| | ANDI to SR | AND immediate to register status |
| CMP | CMP | Compare |
| | CMPA | Compare address |
| | CMPM | Compare memory |
| | CMPI | Compare immediate |
| EOR | EOR | Exclusive-OR |
| | EORI | Exclusive-OR immediate |
| | EORI to CCR | Exclusive-OR immediate to condition codes |
| | EORI to SR | Exclusive-OR immediate to status register |
| MOVE | MOVE | Move source to destination |
| | MOVEA | Move address |
| | MOVEM | Move multiple registers |
| | MOVEP | Move peripheral data |
| | MOVEQ | Move quick |
| | MOVE from SR | Move from status register |
| | MOVE to CCR | Move to condition codes |
| | MOVE USP | Move user stack pointer |
| NEG | NEG | Negate |
| | NEGX | Negate with extend |
| OR | OR | Logical OR |
| | ORI | OR immediate |
| | ORI to CCR | OR immediate to condition codes |
| | ORI to SR | OR immediate to status register |
| SUB | SUB | Subtract |
| | SUBA | Subtract address |
| | SUBI | Subtract immediate |
| | SUBQ | Subtract quick |
| | SUBX | Subtract with extend |

## DATA ORGANIZATION AND ADDRESSING CAPABILITIES

This section contains a description of the registers and the data organization of the 68000.

### Operand Size

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each instruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. Implicit instructions support some subset of all three sizes.

### Data Organization in Registers

The eight data registers support data operands of 1, 8, 16, or 32 bits. The seven address registers together with the stack pointers support address operands of 32 bits.

#### Data Registers

Each data register is 32 bits wide. Byte operands occupy the low-order 8 bits, word operands the low-order 16 bits, and long-word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as 31.

When a data register is used as either a source or destination operand, only the appropriate low-order portion is changed; the remaining high-order portion is neither used nor changed.

#### Address Registers

Each address register and the stack pointer is 32 bits wide and holds a full 32-bit address. Address registers do not support the sized operands. Therefore, when an address register is used as a source operand, either the low-order word or the entire long-word operand is used depending on the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

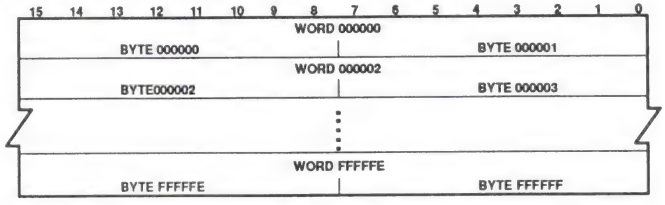



**Figure 4. Word Organization in Memory**

### Data Organization in Memory

Bytes are individually addressable with the high-order byte having an even address the same as the word, as shown in Figure 4. The low-order byte has an odd address that is one count higher than the word address. Instructions and multibyte data are accessed only on word (even byte) boundaries. If a long-word datum is located at address n (n even), then the second word of that datum is located at address n + 2.

The data types supported by the 68000 are: bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary-coded decimal data. Each of these data types is put in memory, as shown in Figure 5. The numbers indicate the order in which the data would be accessed from the processor.

### Addressing

Instructions for the 68000 contain two kinds of information: the type of function to be performed and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

Instructions specify an operand location in one of three ways:

Register specification – the number of the register is given in the register field of their instruction.

Effective address – use of the different effective addressing modes.

Implicit reference – the definition of certain instructions implies the use of specific registers.

### Instruction Format

Instructions are from one to five words in length as shown in Figure 6. The length of the instruction and the operation to be performed is specified by the first word of the instruction which is called the operation word. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

### Program/Data References

The 68000 separates memory references into two classes: program references and data references. Program references, as the name implies, are references to that section of memory that contains the program being executed. Data references refer to that section of memory that contains data. Operand reads are from the data space except in the case of the program counter relative addressing mode. All operand writes are to the data space.

### Register Specification

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

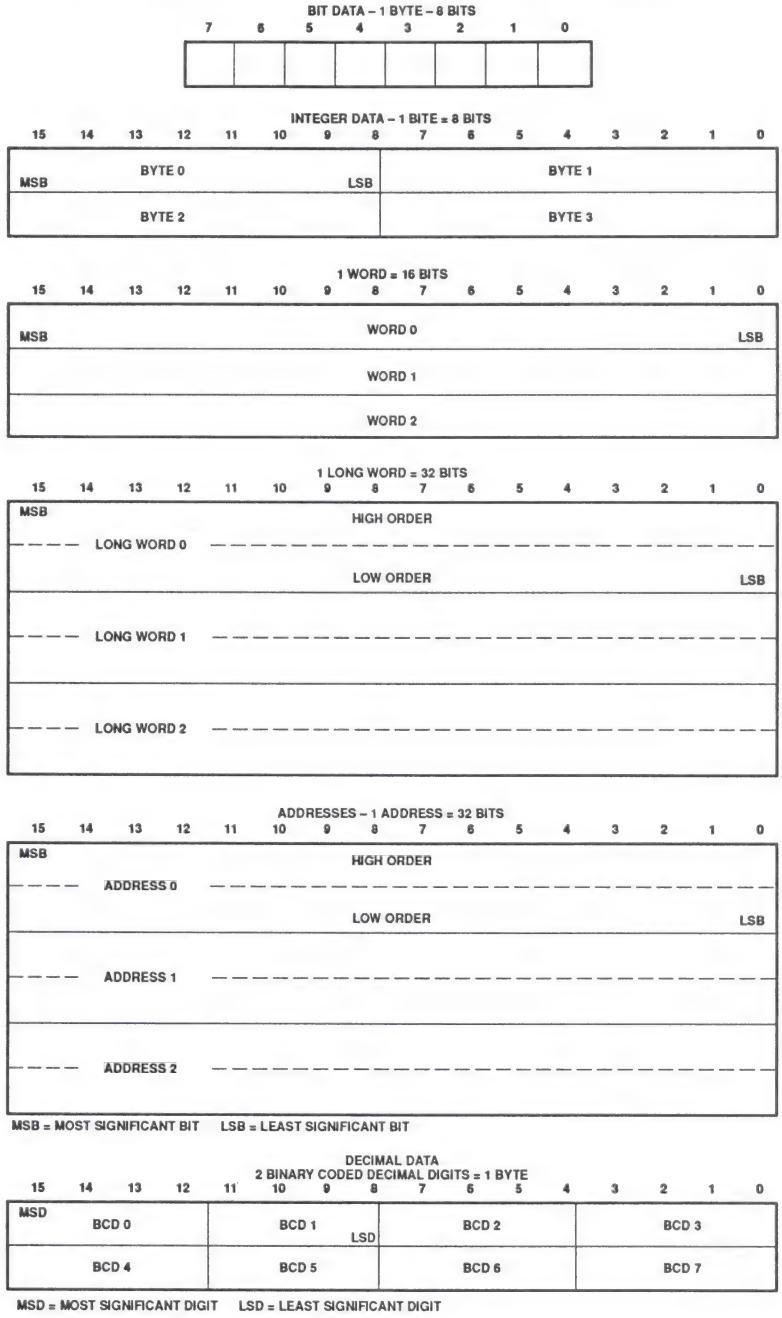

BIT DATA – 1 BYTE – 8 BITS
7 6 5 4 3 2 1 0
INTEGER DATA – 1 BITE = 8 BITS
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MSB
BYTE 0
LSB
BYTE 1
BYTE 2
BYTE 3
1 WORD = 16 BITS
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MSB
WORD 0
LSB
WORD 1
WORD 2
1 LONG WORD = 32 BITS
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MSB
HIGH ORDER
LONG WORD 0
LOW ORDER
LSB
LONG WORD 1
LONG WORD 2
ADDRESSES – 1 ADDRESS = 32 BITS
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MSB
HIGH ORDER
ADDRESS 0
LOW ORDER
LSB
ADDRESS 1
ADDRESS 2
MSB = MOST SIGNIFICANT BIT LSB = LEAST SIGNIFICANT BIT
DECIMAL DATA
2 BINARY CODED DECIMAL DIGITS = 1 BYTE
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MSD
BCD 0
BCD 1
LSD
BCD 2
BCD 3
BCD 4
BCD 5
BCD 6
BCD 7
MSD = MOST SIGNIFICANT DIGIT LSD = LEAST SIGNIFICANT DIGIT

Figure 5. Memory Data Organization

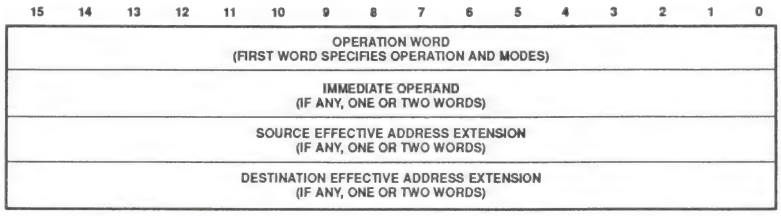

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OPERATION WORD
(FIRST WORD SPECIFIES OPERATION AND MODES)
IMMEDIATE OPERAND
(IF ANY, ONE OR TWO WORDS)
SOURCE EFFECTIVE ADDRESS EXTENSION
(IF ANY, ONE OR TWO WORDS)
DESTINATION EFFECTIVE ADDRESS EXTENSION
(IF ANY, ONE OR TWO WORDS)

Figure 6. Instruction Operation Word General Format

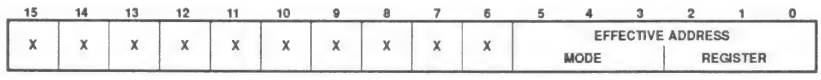



Figure 7. Single-Effective-Address Instruction Operation Word

## Effective Address

Most instructions specify the location of an operand by using the effective address field in the operation word. For example, Figure 7 shows the general format of the single-effective-address instruction operation word. The effective address is composed of two 3-bit fields: the mode field and the register field. The value in the mode field selects the different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction, as shown in Figure 6. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

### Register Direct Modes

These effective addressing modes specify that the operand is in one of 16 multifunction registers.

**Data Register Direct** — The operand is in the data register specified by the effective address register field.

**Address Register Direct** — The operand is in the address register specified by the effective address register field.

### Memory Address Modes

These effective addressing modes specify that the operand is in memory and provide the specific address of the operand.

**Address Register Indirect** — The address of the operand is in the address register specified by the register field. The reference is classified as a data reference with the exception of the jump and jump-to-routine instructions.

**Address Register Indirect with Postincrement** — The address of the operand is in the address register specified by the register field. After the operand address is used, it is incremented by one, two, or four depending on whether the size of the operand is byte, word, or long-word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

**Address Register Indirect with Predecrement** — The address of the operand is in the address register specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long-word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

**Address Register Indirect with Displacement** — This addressing mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference is classified as a data reference with the exception of the jump and jump-to-subroutine instructions.

**Address Register Indirect with Index** — This addressing mode requires one word of extension. The address of the operand is the sum of the address in the address register, the sign-extended displacement integer in the low-order eight bits of the extension word, and contents of the index register. The reference is classified as a data reference with the exception of the jump and jump-to-subroutine instructions.

### Special Address Modes

The special address modes use the effective address register field to specify the special addressing mode instead of a register number.

**Absolute Short Address** — This addressing mode requires one word of extension. The address of the operand is the extension word. The 16-bit address is sign extended before it is used. The reference is classified as a data reference with the exception of the jump and jump-to-subroutine instructions.

**Absolute Long Address** — This addressing mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high-order part of the address is the first extension word; the low-order part of the address is the second extension word. The reference is classified as a data reference with the exception 0f the jump and jump-to-subroutine instructions.

**Program Counter with Displacement** — This addressing mode requires one word of extension. The address of the operand is the sum of the address in the program counter and the sign-extended 16-bit displacement integer in the word. The value in the program counter is the address of the extension word. The reference is classified as a program reference.

**Table 4. Effective Address Encoding Summary**

| ADDRESSING MODE | MODE | REGISTER |
|---|---|---|
| Data register direct | 000 | Register number |
| Address register direct | 001 | Register number |
| Address register indirect | 010 | Register number |
| Address register indirect with postincrement | 011 | Register number |
| Address register indirect with predecrement | 100 | Register number |
| Address register indirect with displacement | 101 | Register number |
| Address register indirect with index | 110 | Register number |
| Absolute short | 111 | 000 |
| Absolute long | 111 | 001 |
| Program counter with displacement | 111 | 010 |
| Program counter with index | 111 | 011 |
| Immediate | 111 | 100 |

**Table 5. Data Movement Operations**

| INSTRUCTION | OPERAND SIZE | OPERATION |
|---|---|---|
| EXG | 32 | Rx ↔ Ry |
| LEA | 32 | EA → An |
| LINK | – | AN → –(SP)<br>SP → An<br>SP + displacement → SP |
| MOVE | 8, 16, 32 | s → (EA)d |
| MOVEM | 16, 32 | (EA) → An, Dn<br>Dn → (EA) |
| MOVEP | 16, 32 | (EA) → Dn<br>Dn → (EA) |
| MOVEQ | 8 | #xxx → Dn |
| PEA | 32 | EA → –(SP) |
| SWAP | 32 | Dn[31:16] ↔ Dn[15:0] |
| UNLK | – | An → SP<br>(SP) + → An |

**NOTES:**
s = source [ ] = bit number ( ) + = indirect with postdecrement
d = destination –( ) = indirect with predecrement # = immediate data

**Program Counter with Index** — This addressing mode requires one word of extension. The address is the sum of the address in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The value in the program counter is the address of the extension word. This reference is classified as a program reference.

**Immediate Data** — This addressing mode requires either one or two words of extension depending on the size of the operation.

Byte operation – operand is low-order byte of extension word.

Word operation – operand is extension word.

Long-word operation – operand is in the two extension words, high-order 16 bits are in the first extension word, low-order 16 bits are in the second extension word.

**Implicit Reference** — Some instructions make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), or the status register (SR). A selected set of instructions may reference the status register by means of the effective address field. These are:

ANDI to CCR
ANDI to SR
EORI to CCR
EORI to SR
ORI to CCR
ORI to SR
MOVE to CCR
MOVE to SR
MOVE from SR

## Effective Address Encoding Summary

Table 4 is a summary of the effective addressing modes discussed in the previous paragraphs.

## System Stack

The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S bit in the status register. If the S bit indicates supervisor state, SSP is the active system stack pointer and the USP cannot be referenced as an address register. If the S bit indicates user state, the USP is the active system stack pointer and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

## INSTRUCTION SET SUMMARY

This section contains an overview of the form and structure of the 68000 instruction set. The instructions form a set of tools that include all the machine functions to perform the following operations:

Data movement
Integer arithmetic
Logical
Shift and rotate
Bit Manipulation
Binary coded decimal
Program control
System control

The complete range of instruction capabilities combined with the flexible addressing modes described previously provide a very flexible base for program development.

## Data Movement Operations

The basic method of data acquisition (transfer and storage) is provided by the move (MOVE) instruction. The move instruction and the effective addressing modes allow both address and data manipulation. Data move instructions allow byte, word, and long-word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long-word operand transfers and ensure that only legal address manipulations are executed. In addition to the general move instruction there are several special data movement instructions: move multiple registers (MOVEM), move peripheral data (MOVEP), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), unlink stack (UNLK), and move quick (MOVEQ). Table 5 is a summary of the data movement operations.

### Table 6. Integer Arithmetic Operations

| INSTRUCTION | OPERAND SIZE | OPERATION |
|---|---|---|
| ADD | 8, 16, 32 | Dn + (EA) → Dn |
| | | (EA) + Dn → (EA) |
| | | (EA) + #xxx → (EA) |
| | 16, 32 | An + (EA) → An |
| ADDX | 8, 16, 32 | Dx + Dy + X → Dx |
| | 16, 32 | –(Ax) + –(Ay) + X → (Ax) |
| CLR | 8, 16, 32 | 0 → EA |
| CMP | 8, 16, 32 | Dn – (EA) |
| | | (EA) – #xxx |
| | | (Ax) + –(Ay)– |
| | 16, 32 | An – (EA) |
| DIVS | 32 ÷ 16 | Dn ÷ (EA) → Dn |
| DIVU | 32 ÷ 16 | Dn ÷ (EA) → Dn |
| EXT | 8 → 16 | $(Dn)_8 \rightarrow Dn_{16}$ |
| | 16 → 32 | $(Dn)_{16} \rightarrow Dn_{32}$ |
| MULS | 16 X 16 → 32 | Dn X (EA) → Dn |
| MULU | 16 X 16 → 32 | Dn X (EA) → Dn |
| NEG | 8, 16, 32 | 0 – (EA) → (EA) |
| NEGX | 8, 16, 32 | 0 – (EA)–X → (EA) |
| SUB | 8, 16, 32 | Dn – (EA) → Dn |
| | | (EA) – Dn → (EA) |
| | | (EA) – #xxx → (EA) |
| | 16, 32 | An – (EA) m→ An |
| SUBX | 8, 16, 32 | Dx – Dy – X → Dx |
| | | – (Ax) – (Ay) – X → (Ax) |
| TAS | 8 | (EA) – 0, 1 → EA[7] |
| TST | 8, 16, 32 | (EA) – 0 |

**NOTES:**
[ ] = bit number
# = immediate data
–( ) = indirect with predecrement
( )+ = indirect with postdecrement

### Table 7. Logical Operations

| INSTRUCTION | OPERAND SIZE | OPERATION |
|---|---|---|
| AND | 8, 16, 32 | Dn ∧ (EA) → Dn |
| | | (EA) ∧ Dn → (EA) |
| | | (EA) ∧ #xxx → (EA) |
| OR | 8, 16, 32 | Dn V (EA) → Dn |
| | | (EA) V Dn → (EA) |
| | | (EA) V #xxx → (EA) |
| EOR | 8, 16, 32 | (EA) ⊕ Dy → (EA) |
| | | (EA) ⊕ #xxx → (EA) |
| NOT | 8, 16, 32 | ~ (EA) → (EA) |

**NOTES:**
# = immediate data
~ = invert
∧ = logical AND
V = logical OR
⊕ = logical Exclusive-OR

## Integer Arithmetic Operations

The arithmetic operations include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV), as well as arithmetic compare (CMP), clear (CLR), and negate (NEG). The add and subtract instructions are available for both address and data operations, with data operations accepting all operand sizes. Address operations are limited to legal address size operands (16 or 32 bits). Data, address, and memory compare operations are also available. The clear and negate instructions may be sued on all sizes of data operands.

The multiply and divide operations are available for signed and unsigned operands using word multiply to produce a long-word product, and a long-word dividend with word divisor to produce a word quotient with a word remainder.

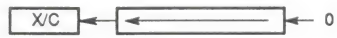
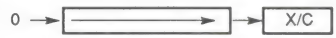
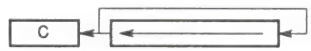
Multiprecision and mixed size arithmetic can be accomplished using a set of extended instructions. These instructions are: add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX).

A test operand (TST) instruction that will set the condition codes as a result of a compare of the operand with zero is also available. Test and set (TAS) is a synchronization instruction useful in multiprocessor systems. Table 6 is a summary of the integer arithmetic operations.

## Logical Operations

Logical operation instructions AND, OR, EOR, and NOT are available for all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provide these logical operations with all sizes of immediate data. Table 7 is a summary of the logical operations.

### Table 8. Shift and Rotate Operations

| INSTRUCTION | OPERAND SIZE | OPERATION |
|---|---|---|
| ASL | 8, 16, 32 |   |
| ASR | 8, 16, 32 | |
| LSL | 8, 16, 32 | |
| LSR | 8, 16, 32 |   |
| ROL | 8, 16, 32 |   |
| ROR | 8, 16, 32 | |
| ROXL | 8, 16, 32 | |
| ROXR | 8, 16, 32 | |

### Shift and Rotate Operations

Shift operations in both directions are provided by the arithmetic instructions ASR and ASL and logical shift instructions LSR and LSL. The rotate instructions (with and without extend) available are ROXR, ROXL, ROR, and ROL. All shift and rotate operations can be performed in either registers or memory. Register shifts and rotates support all operand sizes and allow a shift count specified in a data register.

Memory shifts and rotates are for word operands only and allow only single-bit shifts or rotates.

Table 8 is a summary of the shift and rotate operations.

### Table 9. Bit Manipulation Operations

| INSTRUCTION | OPERAND SIZE | OPERATION |
|---|---|---|
| BTST | 8, 32 | ~bit of (EA) → Z |
| BSET | 8, 32 | ~bit of (EA) → Z<br>1 → bit of EA |
| BCLR | 8, 32 | ~bit of (EA) → Z<br>0 → bit of EA |
| BCHG | 8, 32 | ~bit of (EA) → Z<br>~bit of (EA) → bit of E |

**NOTE:** ~ = invert

### Bit Manipulation Operations

Bit manipulation operations are accomplished using the following instructions: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). Table 9 is a summary of the bit manipulation operations. (Z is bit 2 of the status register.)

### Table 10. Binary Coded Decimal Operations

| INSTRUCTION | OPERAND SIZE | OPERATION |
|---|---|---|
| ABCD | 8 | $Dx_{10} + Dy_{10} + X \rightarrow Dx$<br>$-(Ax)_{10} + -(Ay)_{10} + X \rightarrow (Ax)$ |
| SBCD | 8 | $Dx_{10} - Dy_{10} - X \rightarrow Dx$<br>$-(Ax)_{10} - (Ay)_{10} - X \rightarrow (Ax)$ |
| NBCD | 8 | $0 - (EA)_{10} - X \rightarrow (EA)$ |

**NOTE:** –( ) = indirect with predecrement.

### Table 11. Program Control Operations

| INSTRUCTION | OPERATION |
|---|---|
| **Conditional** | |
| $B_{CC}$ | Branch conditionally (14 conditions)<br>8- and 16-bit displacement |
| $DB_{CC}$ | Test condition, decrement, and branch<br>16-bit displacement |
| $S_{CC}$ | Set byte conditionally (16 conditions) |
| **Unconditional** | |
| BRA | Branch always<br>8- and 16-bit displacement |
| BSR | Branch to subroutine<br>8- and 16-bit displacement |
| JMP | Jump |
| JSR | Jump to subroutine |
| **Returns** | |
| RTR | Return and restore condition codes |
| RTS | Return from subroutine |

### Table 12. System Control Operations

| INSTRUCTION | OPERATION |
|---|---|
| **Privileged** | |
| ANDI To SR | Logical AND to status register |
| EORI to SR | Logical EOR to status register |
| MOVE EA to SR | Load new status register |
| MOVE USP | Move user stack pointer |
| ORI to SR | Lorical OR to status register |
| RESET | Reset external devices |
| RTE | Return from exception |
| STOP | Stop program execution |
| **Trap Generating** | |
| CHK | Check data register against upper bounds |
| TRAP | Trap |
| TRAPV | Trap on overflow |
| **Status Register** | |
| ANDI to CCR | Logical AND to condition codes |
| EORI to CCR | Logical EOR to condition codes |
| MOVE EA to CCR | Load new condition codes |
| MOVE SR to EA | Store status register |
| ORI to CCR | Logical OR to condition codes |

## Binary Coded Decimal Operations

Multiprecision arithmetic operations on binary coded decimal numbers are accomplished using the following instructions: add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 10 is a summary of the binary coded decimal operations.

## Program Control Operations

Program control operations are accomplished using a series of conditional and unconditional branch instructions and return instructions. These instructions are summarized in Table 11.

The conditional instructions provide setting and branching for the following conditions:

CC – carry clear
CS – carry set
EQ – equal
F – never true
GE – greater or equal
GT – greater than
HI – high
LE – less or equal
LS – low or same
LT – less than
MI – minus
NE – not equal
PL – plus
T – always true
VC – no overflow
VS – overflow

## System Control Operations

System control operations are accomplished by using privileged instructions, trap generating instructions, and instructions that use or modify the status register. These instructions are summarized in Table 12.

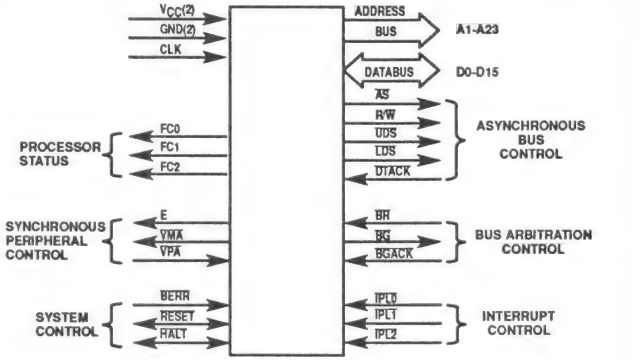



Figure 8. Input and Output Signals

## Table 13. Data Strobe Control of Data Bus

| $\overline{UDS}$ | $\overline{LDS}$ | R/$\overline{W}$ | D8 - D15 | D0 - D7 |
|---|---|---|---|---|
| High | High | – | No valid data | No valid data |
| Low | Low | High | Valid data bits 8 – 15 | Valid data bits 0 – 7 |
| High | Low | High | No valid data | Valid data bits 0 – 7 |
| Low | High | High | Valid data bits 8 – 15 | No valid data |
| Low | Low | Low | Valid data bits 8 – 15 | Valid data bits 0 – 7 |
| High | Low | Low | Valid data bits 0 – 7* | Valid data bits 0 – 7 |
| Low | High | Low | Valid data bits 8 – 15 | Valid data bits 8 – 15* |

NOTE:
* These conditions are a result of current implementation and may not appear on future devices.

## SIGNAL AND BUS OPERATION DESCRIPTION

This section contains a brief description of the input and output signals. A discussion of bus operation during the various machine cycles and operations is also give.

### NOTE

The terms **assertion** and **negation** will be used extensively. This is done to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The term assert or assertion is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation is used to indicate that a signal is inactive or false.

### Signal Description

The input and output signals can be functionally organized into the groups shown in Figure 8. The following paragraphs provide a brief description of the signals and a reference (if applicable) to other paragraphs that contain more detail about the function being performed.

**Address Bus (A1 through A23)**

This 23-bit, unidirectional, three-state bus is capable of addressing 8 megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are all set to a logic high.

**Data Bus (D0 through D15)**

This 16-bit bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0 - D7.

**Asynchronous Bus Control**

Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

**Address Strobe ($\overline{AS}$)** — This signal indicates that there is a valid address on the address bus.

**Read/Write (R/$\overline{W}$)** — This signal defines the data bus transfer as a read or write cycle. The R/$\overline{W}$ signal also works in conjunction with the data strobes as explained in the following paragraph.

**Upper and Lower Data Strobe ($\overline{UDS}$, $\overline{LDS}$)** — These signals control the flow of data on the data bus, as shown in Table 13. When the R/$\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R/$\overline{W}$ line is low the processor will write to the data bus as shown.

**Data Transfer Acknowledge ($\overline{DTACK}$)** — This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated. (Refer to **Asynchronous Versus Synchronous Operation**).

**Bus Arbitration Control**

The three signals, bus request, bus grant, and bus grant acknowledge, form a bus arbitration circuit to determine which device will be the bus master device.

**Bus Request ($\overline{BR}$)** — This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

**Bus Grant ($\overline{BG}$)** — This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

**Bus Grant Acknowledge ($\overline{BGACK}$)** — This input indicates that some other device has become the bus master. This signal should not be asserted until the following four conditions are met::

1. a bus grant has been received,
2. address strobe is inactive which indicates that the microprocessor is not using the bus,
3. data transfer acknowledge is inactive which indicates that neither memory nor peripherals are using the bus, and
4. bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

**Interrupt Control ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$)**

These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. Level seven cannot be masked. The least significant bit is given in $\overline{IPL0}$ and the most significant bit is contained in $\overline{IPL2}$. These lines must remain stable until the processor signals interrupt acknowledge (FC0 - FC2 are all high) to insure that the interrupt is recognized.

**System Control**

The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. the three system control inputs are explained in the following paragraphs.

**Bus Error ($\overline{BERR}$)** — This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices,
2. Interrupt vector number acquisition failure,
3. illegal access request as determined by a memory management unit, or
4. other application dependent errors.

The bus error signal interacts with the halt signal to determine if the current bus cycle should be re-executed or if exception processing should be performed.

Refer to **Bus Error and Halt Operation** for additional information about the interaction of the bus error and halt signals.

**Reset ($\overline{RESET}$)** — This bidirectional signal line acts to reset (start a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of a $\overline{RESET}$ instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external $\overline{HALT}$ and $\overline{RESET}$ signals applied at the same time. Refer to **Reset Operation** for further information.

**Halt ($\overline{HALT}$)** — When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all 3-State lines are put in their high-impedance state (refer to Table 15). Refer to **Bus Error and Halt Operation** for additional information about the interaction between the $\overline{HALT}$ and bus error signals.

When the processor has stopped executing instructions, such as in a double bus fault condition (refer to **Double Bus Faults**), the $\overline{HALT}$ line is driven by the processor to indicate to external devices that the processor has stopped.

**Peripheral Control**

These control signals are used to allow the interfacing of synchronous peripheral devices with the asynchronous 68000. These signals are explained in the following paragraphs.

**Enable (E)** — This signal is the standard enable signal common to all synchronous type peripheral devices. The period for this output is ten 68000 clock periods (six clocks low, four clocks high). Enable is generated by an internal ring counter which may come up in any state (i.e., at power on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

**Valid Peripheral Address ($\overline{VPA}$)** —This input indicates that the device or region addressed is a synchronous family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt. Refer to **Interface with Synchronous Peripherals**.

**Valid Memory Address ($\overline{VMA}$)** — This output is used to indicate to synchronous peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address ($\overline{VPA}$) input which indicates that the peripheral is a synchronous family device.

**Processor Status (FC0, FC1, FC2)**

These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 14. The information indicated by the function code outputs is valid whenever address strobe ($\overline{AS}$) is active.

## Table 14. Function Code Outputs

| FUNCTION CODE OUTPUT | | | |
|---|---|---|---|
| FC2 | FC1 | FC0 | CYCLE TYPE |
| Low | Low | Low | (Undefined, reserved) |
| Low | Low | High | User data |
| Low | High | Low | User program |
| Low | High | High | (Undefined, reserved) |
| High | Low | Low | (Undefined, reserved) |
| High | Low | High | Supervisor data |
| High | High | Low | Supervisor program |
| High | High | High | Interrupt acknowledge |

**Clock (CLK)**

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time and the clock signal must conform to minimum and maximum pulse width times.

**Signal Summary**

Table 15 is a summary of all the signals discussed in the previous paragraphs.

## Bus Operation

The following paragraphs explain control signal and bus operation during data transfer operations, bus arbitration, bus error and halt conditions, and reset operation.

### Data Transfer Operations

1. address bus A1 through A23,
2. data bus D0 through D15, and
3. control signals.

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the 68000 for interlocked multiprocessor communications.

**Read Cycle** — During a read cycle, the processor receives data from the memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions it internally.

A word read cycle flowchart is given in Figure 9. A byte read cycle flowchart is given in Figure 10. Read cycle timing is given in Figure 11. Figure 12 details word and byte read cycle operations.

### Table 15. Signal Summary

| SIGNAL NAME | MNEMONIC | INPUT/OUTPUT | ACTIVE STATE | HI-Z | |
|---|---|---|---|---|---|
| | | | | on $\overline{HALT}$ | on $\overline{BGACK}$ |
| Address bus | A1-A23 | Output | High | Yes | Yes |
| Data bus | D0-D15 | Input/output | High | Yes | Yes |
| Address strobe | $\overline{AS}$ | Output | Low | No | Yes |
| Read/write | R/$\overline{W}$ | Output | Read-high Write-low | No | Yes |
| Upper and lower data strobes | $\overline{UDS}$, $\overline{LDS}$ | Output | Low | No | Yes |
| Data transfer acknowledge | $\overline{DTACK}$ | Input | Low | No | No |
| Bus request | $\overline{BR}$ | Input | Low | No | No |
| Bus grant | $\overline{BG}$ | Output | Low | No | No |
| Bus grant acknowledge | $\overline{BGACK}$ | Input | Low | No | No |
| Interrupt priority level | $\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$ | Input | Low | No | No |
| Bus error | $\overline{BERR}$ | Input | Low | No | No |
| Reset | $\overline{RESET}$ | Input/output | Low | No[1] | No[1] |
| Halt | $\overline{HALT}$ | Input/output | Low | No[1] | No[1] |
| Enable | $\overline{E}$ | Output | High | No | No |
| Valid memory address | $\overline{VMA}$ | Output | Low | No | Yes |
| Valid peripheral address | $\overline{VPA}$ | Input | Low | No | No |
| Function code output | FC0, FC1, FC2 | Output | High | No[2] | Yes |
| Clock | CLK | Input | High | No | No |
| Power input | $V_{CC}$ | Input | – | – | – |
| Ground | GND | Input | – | – | – |

**NOTES:**
1. Open Drain
2. Function codes are placed in high-impedance state during HALT.

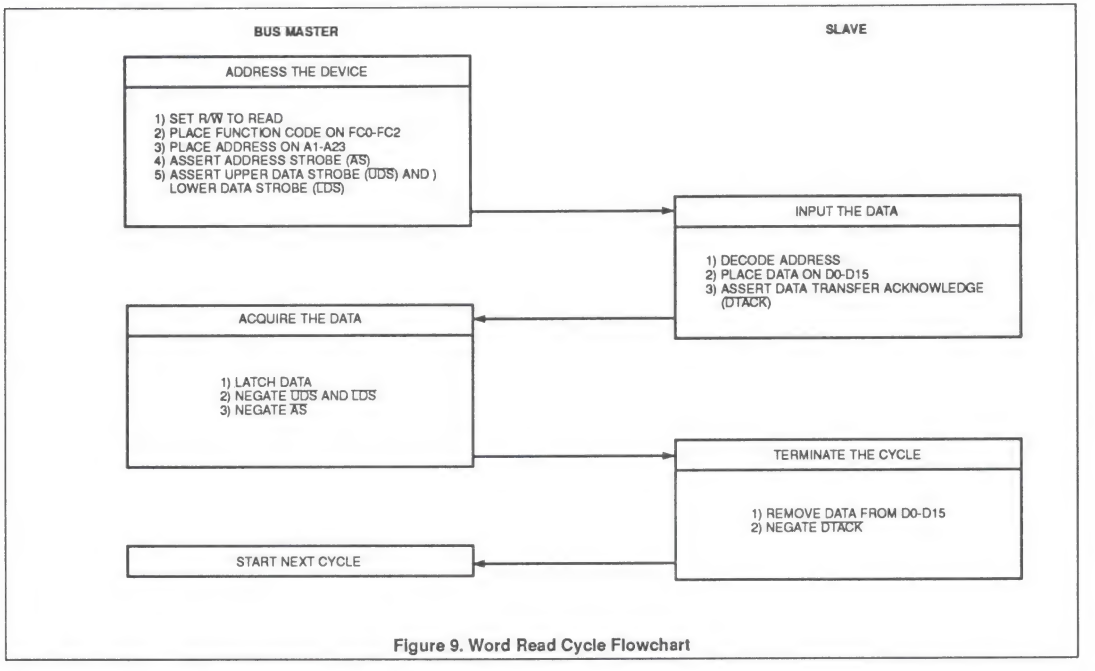

BUS MASTER
SLAVE
ADDRESS THE DEVICE
1) SET R/W TO READ
2) PLACE FUNCTION CODE ON FC0-FC2
3) PLACE ADDRESS ON A1-A23
4) ASSERT ADDRESS STROBE (AS)
5) ASSERT UPPER DATA STROBE (UDS) AND )
LOWER DATA STROBE (LDS)
INPUT THE DATA
1) DECODE ADDRESS
2) PLACE DATA ON D0-D15
3) ASSERT DATA TRANSFER ACKNOWLEDGE (DTACK)
ACQUIRE THE DATA
1) LATCH DATA
2) NEGATE UDS AND LDS
3) NEGATE AS
TERMINATE THE CYCLE
1) REMOVE DATA FROM D0-D15
2) NEGATE DTACK
START NEXT CYCLE

**Figure 9. Word Read Cycle Flowchart**

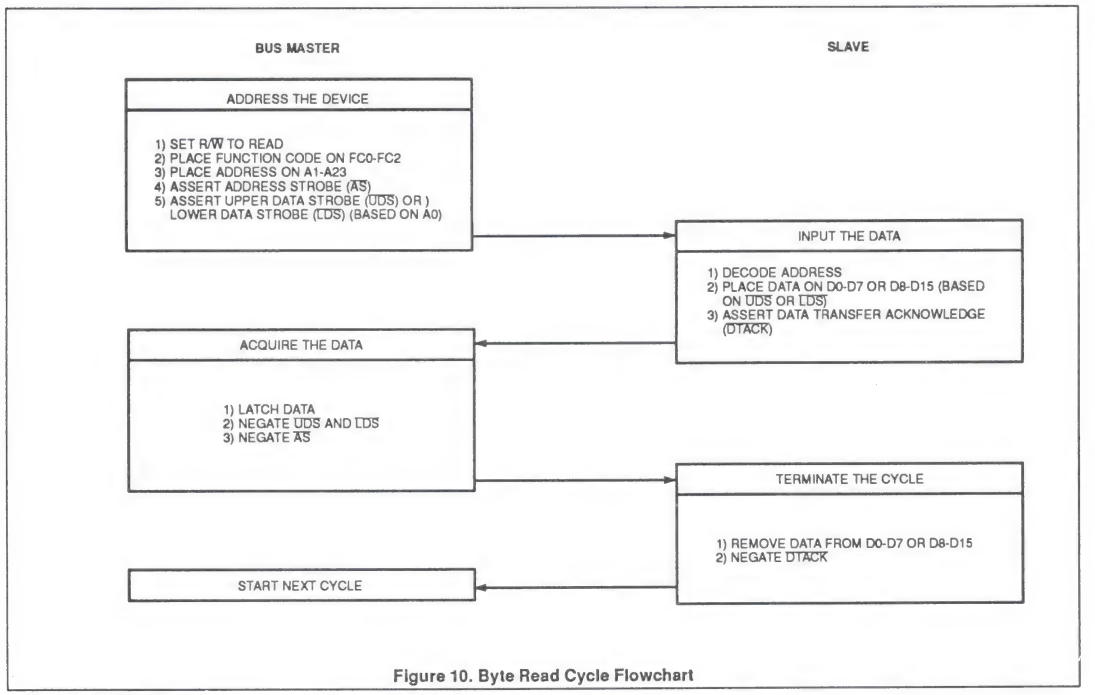

BUS MASTER
SLAVE
ADDRESS THE DEVICE
1) SET R/W TO READ
2) PLACE FUNCTION CODE ON FC0-FC2
3) PLACE ADDRESS ON A1-A23
4) ASSERT ADDRESS STROBE (AS)
5) ASSERT UPPER DATA STROBE (UDS) OR )
LOWER DATA STROBE (LDS) (BASED ON A0)
INPUT THE DATA
1) DECODE ADDRESS
2) PLACE DATA ON D0-D7 OR D8-D15 (BASED ON UDS OR LDS)
3) ASSERT DATA TRANSFER ACKNOWLEDGE (DTACK)
ACQUIRE THE DATA
1) LATCH DATA
2) NEGATE UDS AND LDS
3) NEGATE AS
TERMINATE THE CYCLE
1) REMOVE DATA FROM D0-D7 OR D8-D15
2) NEGATE DTACK
START NEXT CYCLE

**Figure 10. Byte Read Cycle Flowchart**

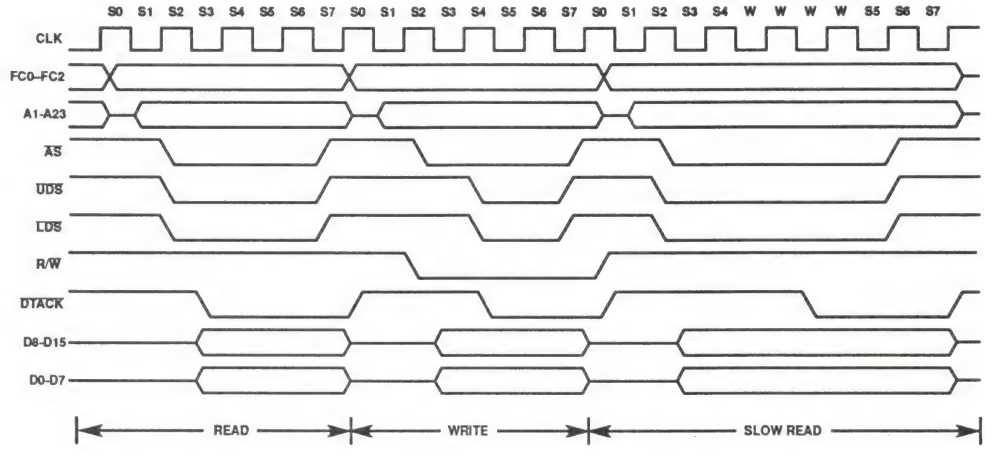



Figure 11. Read and Write Cycle Timing Diagram

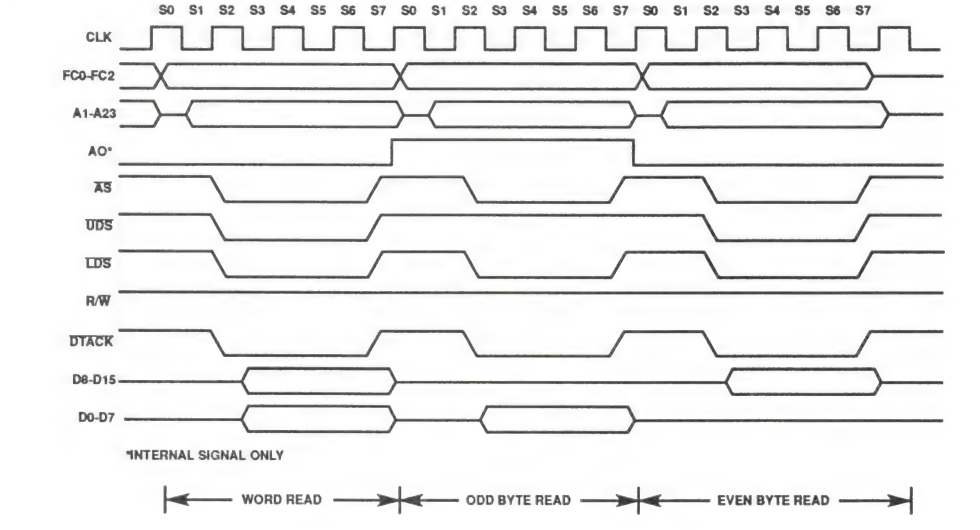



Figure 12. Word and Byte Read Cycle Timing Diagram

**Write Cycle** — During a write cycle, the processor sends data to either the memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued. A word write cycle flowchart is given in Figure 13. A byte write cycle flowchart is given in Figure 14. Write cycle timing is given in Figure 11. Figure 15 details word and byte write cycle operation.

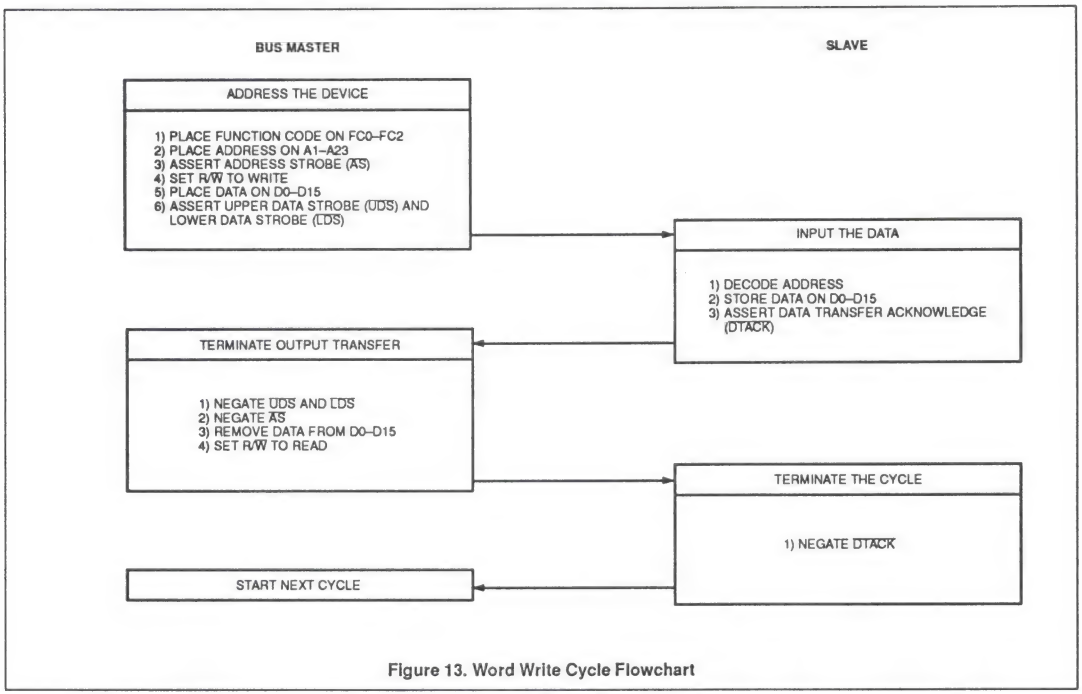

BUS MASTER
SLAVE
ADDRESS THE DEVICE
1) PLACE FUNCTION CODE ON FC0–FC2
2) PLACE ADDRESS ON A1–A23
3) ASSERT ADDRESS STROBE (AS)
4) SET R/W TO WRITE
5) PLACE DATA ON D0–D15
6) ASSERT UPPER DATA STROBE (UDS) AND LOWER DATA STROBE (LDS)
INPUT THE DATA
1) DECODE ADDRESS
2) STORE DATA ON D0–D15
3) ASSERT DATA TRANSFER ACKNOWLEDGE (DTACK)
TERMINATE OUTPUT TRANSFER
1) NEGATE UDS AND LDS
2) NEGATE AS
3) REMOVE DATA FROM D0–D15
4) SET R/W TO READ
TERMINATE THE CYCLE
1) NEGATE DTACK
START NEXT CYCLE

**Figure 13. Word Write Cycle Flowchart**

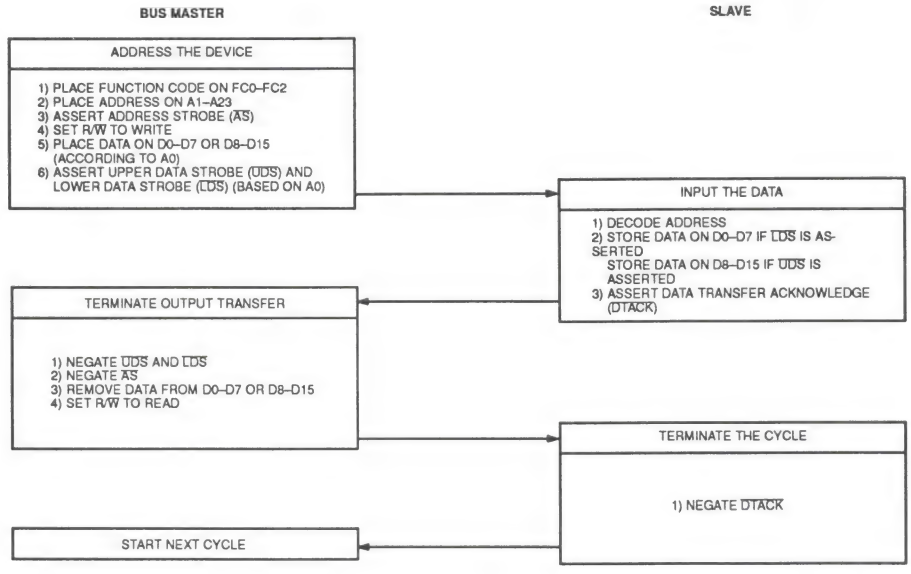

BUS MASTER
SLAVE
ADDRESS THE DEVICE
1) PLACE FUNCTION CODE ON FC0–FC2
2) PLACE ADDRESS ON A1–A23
3) ASSERT ADDRESS STROBE (AS)
4) SET R/W TO WRITE
5) PLACE DATA ON D0–D7 OR D8–D15 (ACCORDING TO A0)
6) ASSERT UPPER DATA STROBE (UDS) AND LOWER DATA STROBE (LDS) (BASED ON A0)
INPUT THE DATA
1) DECODE ADDRESS
2) STORE DATA ON D0–D7 IF LDS IS ASSERTED
STORE DATA ON D8–D15 IF UDS IS ASSERTED
3) ASSERT DATA TRANSFER ACKNOWLEDGE (DTACK)
TERMINATE OUTPUT TRANSFER
1) NEGATE UDS AND LDS
2) NEGATE AS
3) REMOVE DATA FROM D0–D7 OR D8–D15
4) SET R/W TO READ
TERMINATE THE CYCLE
1) NEGATE DTACK
START NEXT CYCLE

Figure 14. Byte Write Cycle Flowchart

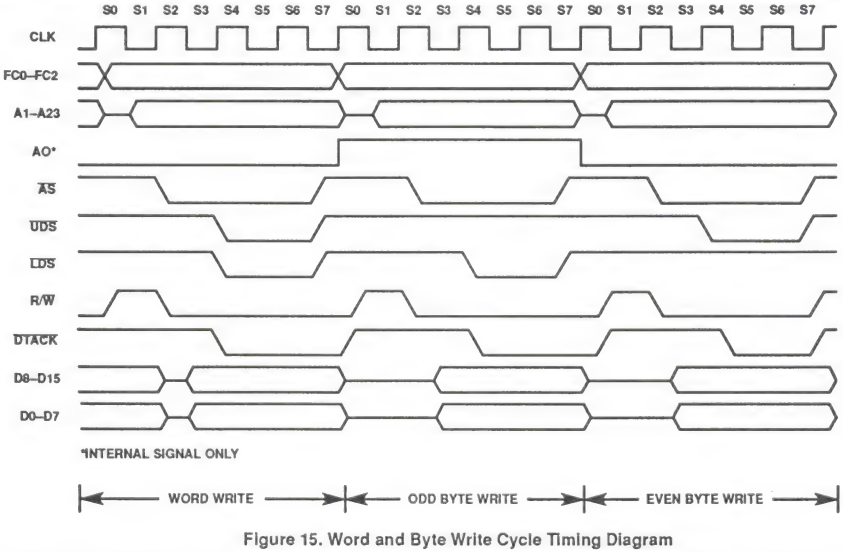



Figure 15. Word and Byte Write Cycle Timing Diagram

**Read-Modify-Write Cycle** — The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the 68000, this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write cycles are byte operations. A read-modify-write cycle flowchart is given in Figure 16 and a timing diagram is given in Figure 17.

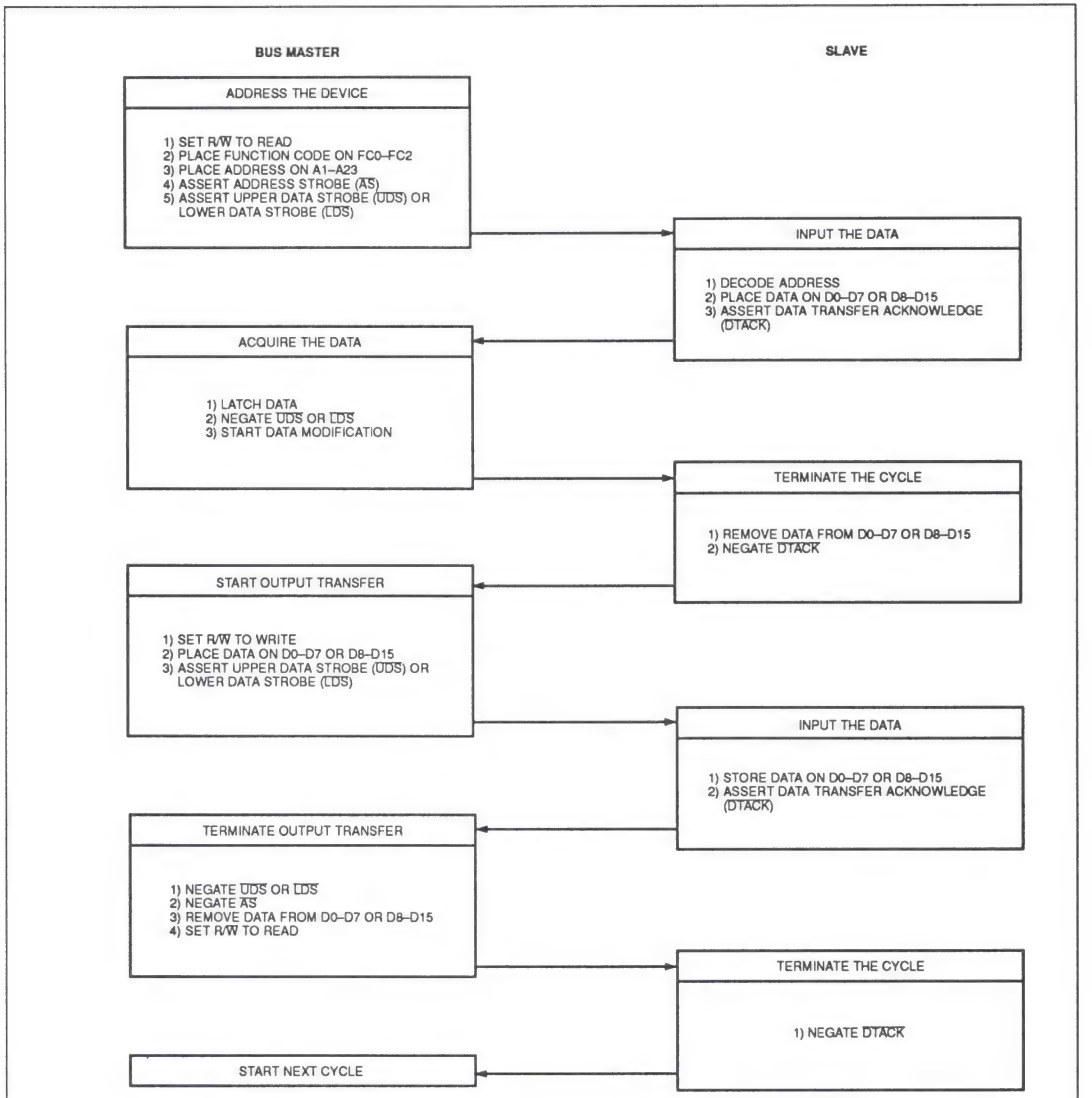

BUS MASTER
SLAVE
ADDRESS THE DEVICE
1) SET R/W TO READ
2) PLACE FUNCTION CODE ON FC0–FC2
3) PLACE ADDRESS ON A1–A23
4) ASSERT ADDRESS STROBE (AS)
5) ASSERT UPPER DATA STROBE (UDS) OR LOWER DATA STROBE (LDS)
INPUT THE DATA
1) DECODE ADDRESS
2) PLACE DATA ON D0–D7 OR D8–D15
3) ASSERT DATA TRANSFER ACKNOWLEDGE (DTACK)
ACQUIRE THE DATA
1) LATCH DATA
2) NEGATE UDS OR LDS
3) START DATA MODIFICATION
TERMINATE THE CYCLE
1) REMOVE DATA FROM D0–D7 OR D8–D15
2) NEGATE DTACK
START OUTPUT TRANSFER
1) SET R/W TO WRITE
2) PLACE DATA ON D0–D7 OR D8–D15
3) ASSERT UPPER DATA STROBE (UDS) OR LOWER DATA STROBE (LDS)
INPUT THE DATA
1) STORE DATA ON D0–D7 OR D8–D15
2) ASSERT DATA TRANSFER ACKNOWLEDGE (DTACK)
TERMINATE OUTPUT TRANSFER
1) NEGATE UDS OR LDS
2) NEGATE AS
3) REMOVE DATA FROM D0–D7 OR D8–D15
4) SET R/W TO READ
TERMINATE THE CYCLE
1) NEGATE DTACK
START NEXT CYCLE

**Figure 16. Read-Modify-Write Cycle Flowchart**

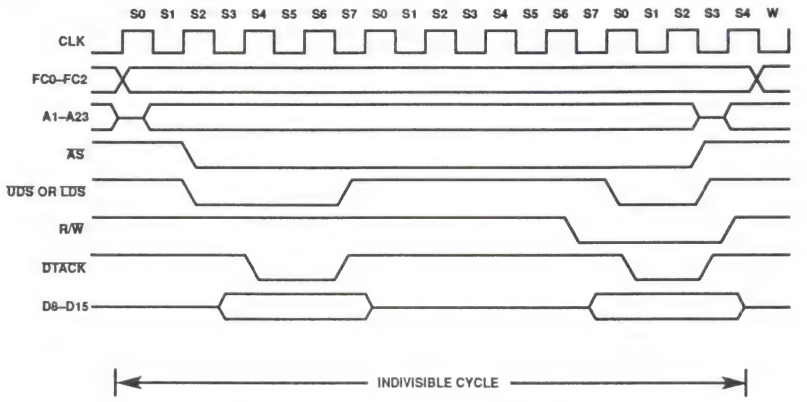



**Figure 17. Read-Modify-Write Cycle Timing Diagram**

**Bus Arbitration**

Bus arbitration is a technique used by master-type devices to request, be granted, and acknowledge bus mastership. In its simplest form, it consists of the following:

1. asserting a bus mastership request,
2. receiving a grant that the bus is available at the end of the current cycle, and
3. acknowledging that mastership has been assumed.

Figure 18 is a flowchart showing the detail involved in a request from a single device. Figure 19 is a timing diagram for the same operation. This technique allows processing of bus requests during data transfer cycles.

The timing diagram shows that the bus request is negated at the time that an acknowledge is asserted. This type of operation would be true for a system consisting of the processor and one device capable of bus mastership. In systems having a number of devices capable of bus mastership, the bus request line from each device is wire-ORed to the processor. In this system, it is easy to see that there could be more than one bus request being made. The timing diagram shows that the bus grant signal is negated a few clock cycles after the transition of the acknowledge ($\overline{BGACK}$) signal.

However, if the bus requests are still pending, the processor will assert another bus grant within a few clock cycles after it was negated. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

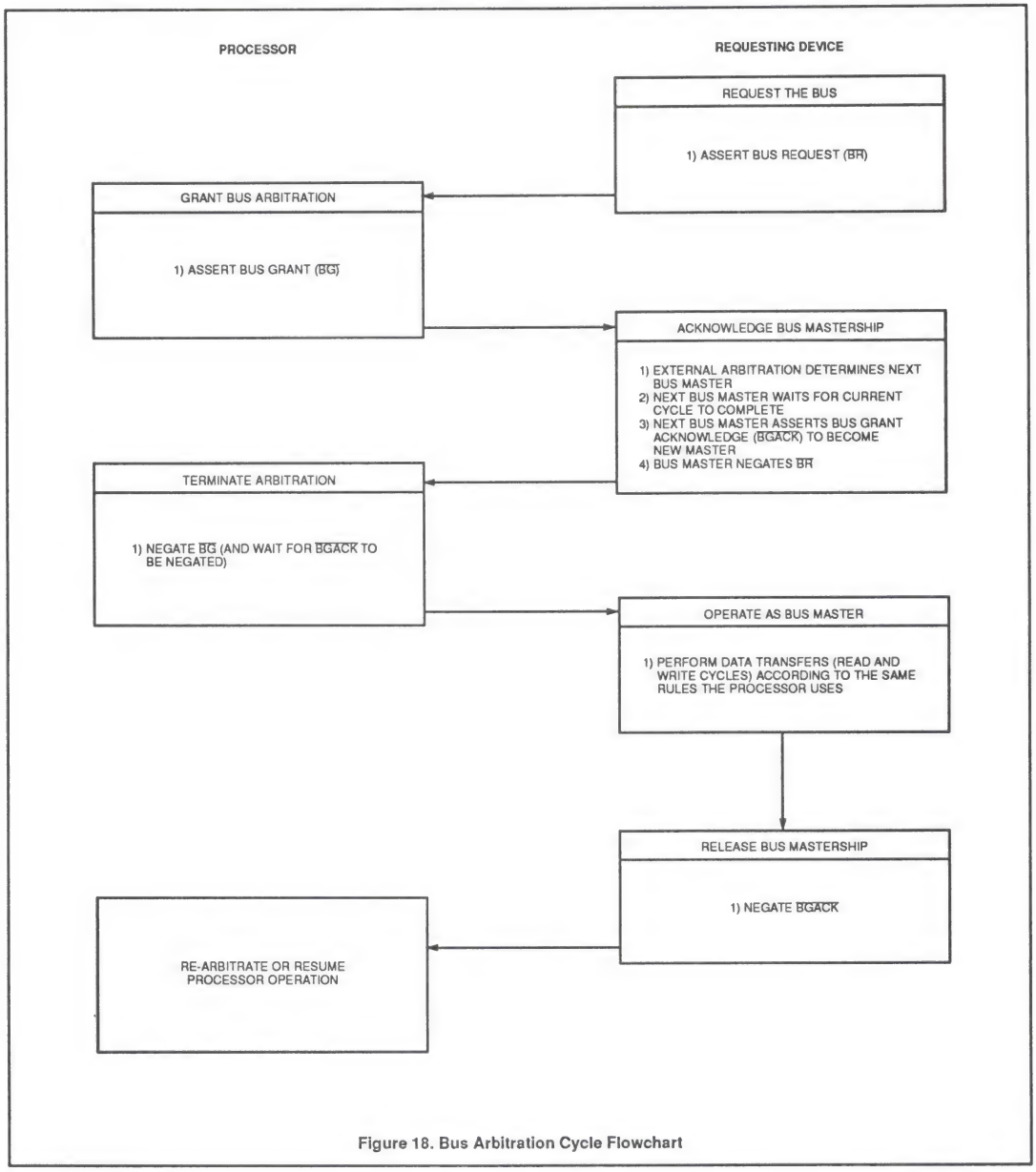

PROCESSOR
REQUESTING DEVICE
REQUEST THE BUS
1) ASSERT BUS REQUEST (BR)
GRANT BUS ARBITRATION
1) ASSERT BUS GRANT (BG)
ACKNOWLEDGE BUS MASTERSHIP
1) EXTERNAL ARBITRATION DETERMINES NEXT BUS MASTER
2) NEXT BUS MASTER WAITS FOR CURRENT CYCLE TO COMPLETE
3) NEXT BUS MASTER ASSERTS BUS GRANT ACKNOWLEDGE (BGACK) TO BECOME NEW MASTER
4) BUS MASTER NEGATES BR
TERMINATE ARBITRATION
1) NEGATE BG (AND WAIT FOR BGACK TO BE NEGATED)
OPERATE AS BUS MASTER
1) PERFORM DATA TRANSFERS (READ AND WRITE CYCLES) ACCORDING TO THE SAME RULES THE PROCESSOR USES
RELEASE BUS MASTERSHIP
1) NEGATE BGACK
RE-ARBITRATE OR RESUME PROCESSOR OPERATION

**Figure 18. Bus Arbitration Cycle Flowchart**

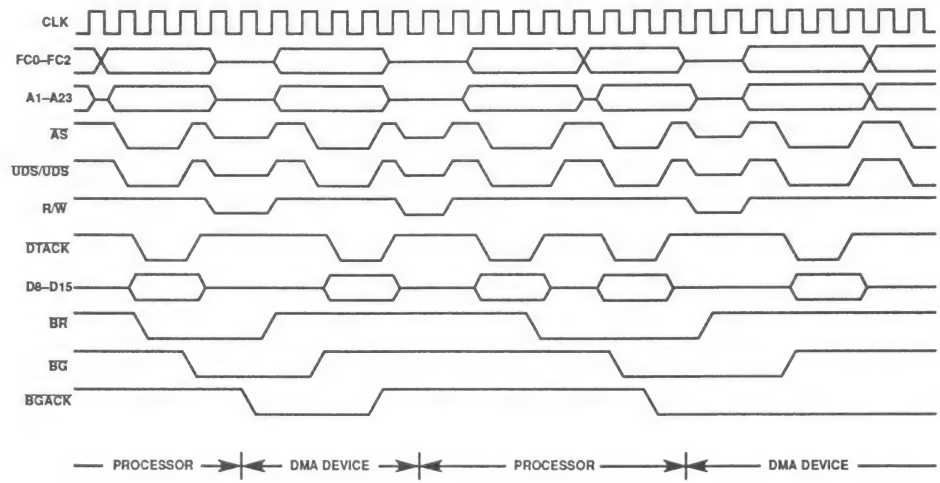



Figure 19. 68000 Bus Arbitration Cycle Timing Diagram

**Requesting the Bus** — External devices capable of becoming bus masters request the bus by asserting the bus request ($\overline{BR}$) signal. This is a wire-ORed signal (although it need not be constructed from open-collector devices) that indicates to the processor that some external device requires control of the external bus. The processor is effectively at a lower bus priority level than the external device and will relinquish the bus after it has completed the last bus cycle it has started.

When no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows ordinary processing to continue if the arbitration circuitry responded to noise inadvertently.

**Receiving the Bus Grant** — The processor asserts bus grant ($\overline{BG}$) as soon as possible. Normally this is immediately after internal synchronization. The only exception to this occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe ($\overline{AS}$) signal. In this case, but grant will be delayed until $\overline{AS}$ is asserted to indicate external devices that a bus cycle is being executed.

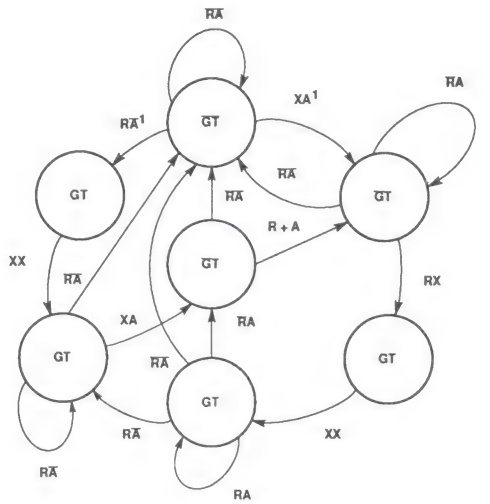
The bus grant signal may be routed through a daisy-chained network or through a specific priority-encoded network. The processor is not affected by the external method of arbitration as long as the protocol is obeyed.

**Acknowledgment of Mastership** — Upon receiving a bus grant, the requesting device waits until address strobe, data transfer acknowledge, and bus grant acknowledge are negated before issuing its own $\overline{BGACK}$. The negation of the address strobe indicates that the previous master has completed its cycle; the negation of bus grant acknowledge indicates that the previous master has released the bus. (While address strobe is asserted, no device is allowed to "break into" a cycle.) The negation of data transfer acknowledge indicates the previous slave has terminated its connection to the previous master. Note that in some applications data transfer acknowledge might not enter into this function. General purpose devices would then be connected such that they were only dependent on address strobe. When bus grant acknowledge is issued, the device is a bus master until it negates bus grant acknowledge. Bus grant acknowledge should not be negated until after the bus cycle(s) is (are) completed. Bus mastership is terminated at the negation of bus grant acknowledge.

The bus request from the granted device should be dropped after bus grant acknowledge is asserted. If a bus request is still pending, another bus grant will be asserted within a few clocks of the negation of the bus grant. Refer to **Bus Arbitration Control**. Note that the processor does not perform any external bus cycles before it re-asserts bus grant.

**Bus Arbitration Control**

The bus arbitration control unit in the SCN68000 is implemented with a finite state machine. A state diagram of this machine is shown in Figure 20. All asynchronous signals to the SCN68000 are synchronized before being used internally. This synchronization is accomplished in a maximum of one cycle of the system clock, assuming that the asynchronous input setup time (#47) has been met (see Figure 21). The input signal is sampled on the falling edge of the clock and is valid internally after the next falling edge.




**NOTES:**
R = Bus request internal
A = Bus grant acknowledge internal
G = Bus grant
T = Three-state control to bus control logic[2]
X = Don't care
1. State machine will not change if the bus is S0 or S1. Refer to Bus Arbitration Control.
2. The address bus will be placed in the high-impedance state if T is asserted and $\overline{AS}$ is negated.

**Figure 20. 68000 Bus Arbitration Control Unit State Diagram**

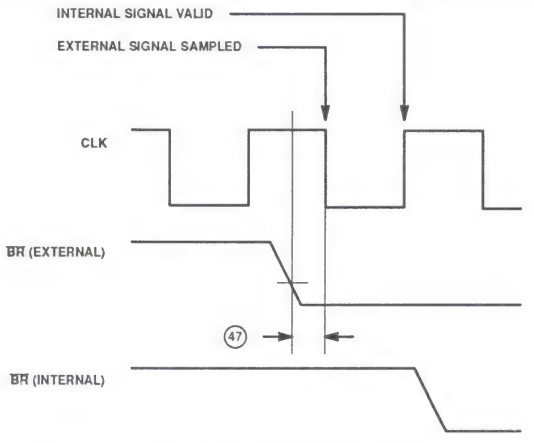



**Figure 21. Timing Relationship of External Asynchronous Inputs to Internal Signals**

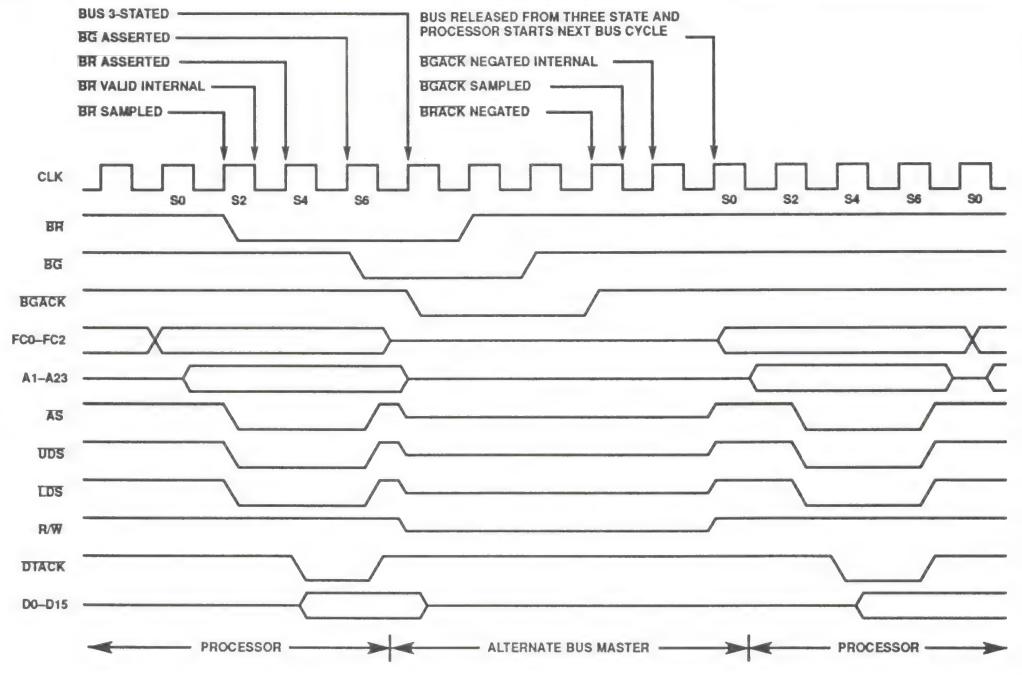



**Figure 22. Bus Arbitration Timing Diagram—Processor Active**

As shown in Figure 20, input signals labeled R and A are internally synchronized on the bus request and bus grant acknowledge pins, respectively. The bus grant output is labeled G and the internal 3-State control signal T. If T is true, the address, data, and control buses are placed in a high-impedance state when $\overline{AS}$ is negated. All signals are shown in positive logic (active high) regardless of their true active voltage level. State changes (valid outputs) occur on the next rising edge after the internal signal is valid.

A timing diagram of the bus arbitration sequence during a processor bus cycle is shown in Figure 22. the bus arbitration sequence while the bus is inactive (i.e., executing internal operations such as a multiply instruction) is shown in Figure 23.

If a bus request is made at a time when the MPU has already begun a bus cycle but $\overline{AS}$ has not been asserted (bus state S0), $\overline{BG}$ will not be asserted on the next rising edge. Instead, $\overline{BG}$ will be delayed until the second rising edge following its internal assertion. This sequence is shown in Figure 24.

### Bus Error and Halt Operation

In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems will require a different maximum response time, a bus error input is provided. External circuitry must be used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error signal is received, the processor has two options: initiate a bus error exception sequence or try running the bus cycle again.

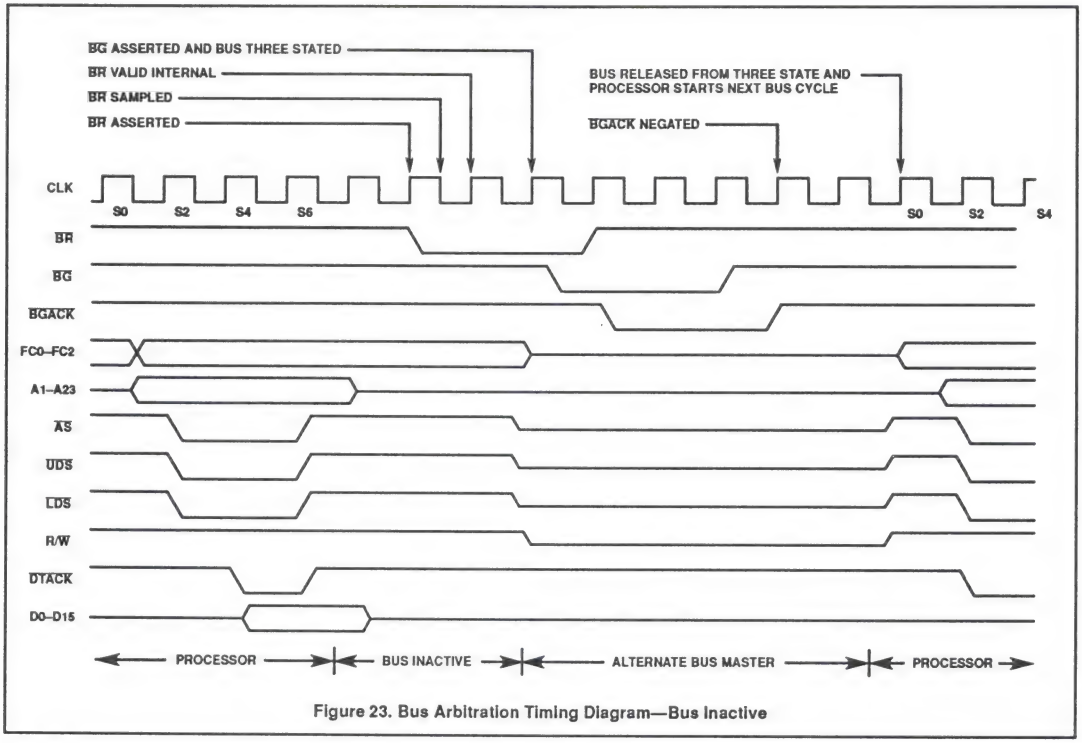



Figure 23. Bus Arbitration Timing Diagram—Bus Inactive

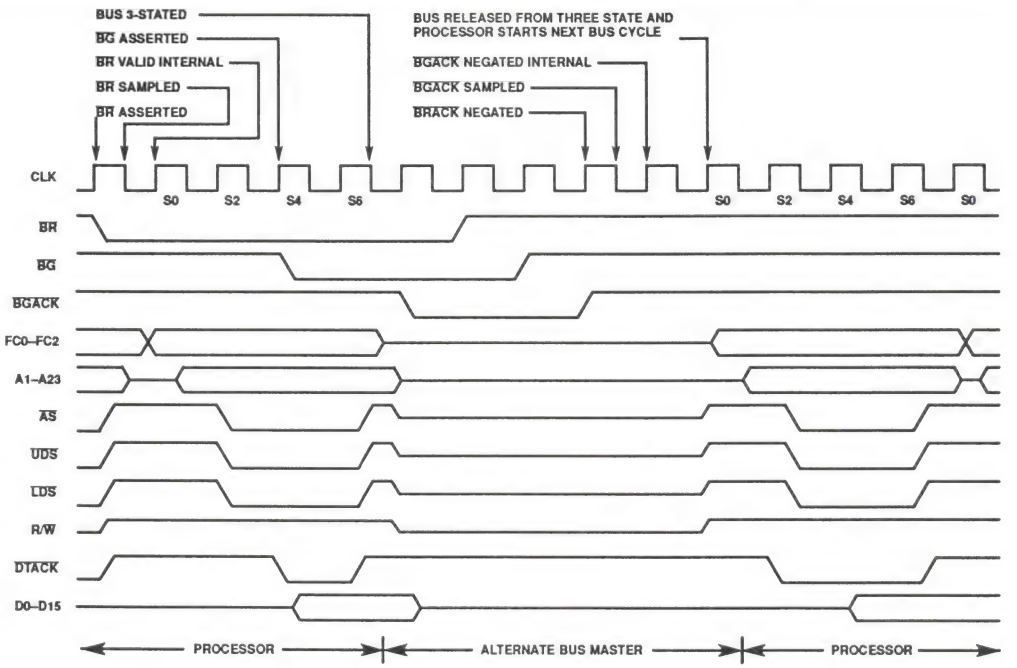



**Figure 24. Bus Arbitration Timing Diagram—Special Case**

**Bus Error Operation** — When the bus error signal is asserted, the current bus cycle is terminated. If $\overline{BERR}$ is asserted before the falling edge of S2, $\overline{AS}$ will be negated in S7 in either a read or write cycle. As long as $\overline{BERR}$ remains asserted, the data and address buses will be in the high-impedance state. When $\overline{BERR}$ is negated, the processor will begin stacking for exception processing. Figure 25 is a timing diagram for the exception sequence. The sequence is composed of the following elements:

1. stacking the program counter and status register,
2. stacking the error information,
3. reading the bus error vector table entry, and
4. executing the bus error handler routine.

The stacking of the program counter and the status register is the same as if an interrupt had occurred. Several additional items are stacked when a bus error occurs. These items are used to determine the nature of the error and correct it, if possible. The bus error vector is vector number two located at address $000008. The processor loads the new program counter from this location. A software bus error handler routine is then executed by the processor. Refer to **Exception Processing** for additional information.

**Re-Run Operation** — When, during a bus cycle, the processor receives a bus error signal and the halt pin is being driven by an external device, the processor enters the re-run sequence. Figure 26 is a timing diagram for re-running the bus cycle.

The processor terminates the bus cycle, then puts the address and data output lines in the high-impedance state. The processor remains "halted", and will not run another bus cycle until the halt signal is removed by external logic. Then the processor will re-run the previous cycle using the same function codes, the same data (for a write operation), and the same controls. The bus error signal should be removed at least one clock cycle before the halt signal is removed.

NOTE
The processor will not re-run a read-modify-write cycle. This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a test-and-set operation is performed without ever releasing $\overline{AS}$, if $\overline{BERR}$ and $\overline{HALT}$ are asserted during a read-modify-write bus cycle, a bus error operation results.

**Halt Operation** — The halt input signal to the 68000 performs a halt/run/single-step function in a similar fashion to the synchronous device halt function. The halt and run modes are somewhat self-explanatory in that when the halt signal is constantly active the processor "halts" (does nothing) and when the halt signal is constantly inactive the processor "runs" (does something).

This single-step mode is derived from correctly timed transitions on the halt signal input. It forces the processor to execute a single bus cycle by entering the run mode until the processor starts a bus cycle then changing to the halt mode. thus, the single-step mode allows the user to proceed through (and therefore debut) processor operations one bus cycle at a time.

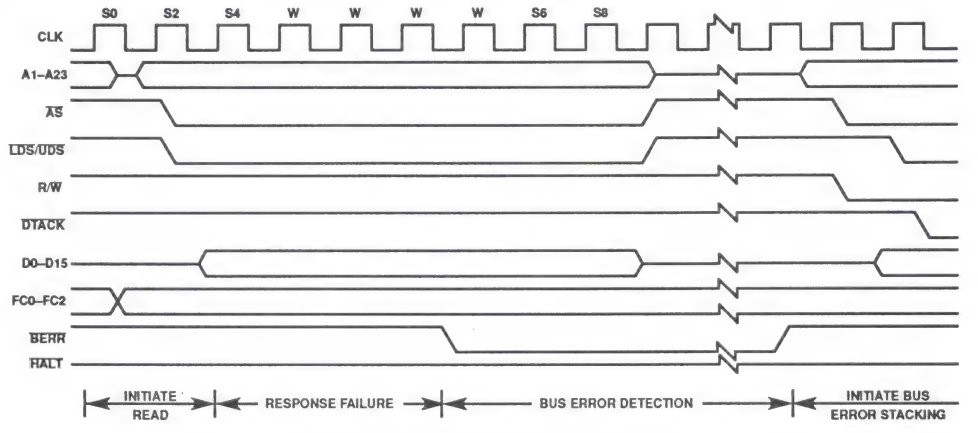



Figure 25. Bus Error Timing Diagram

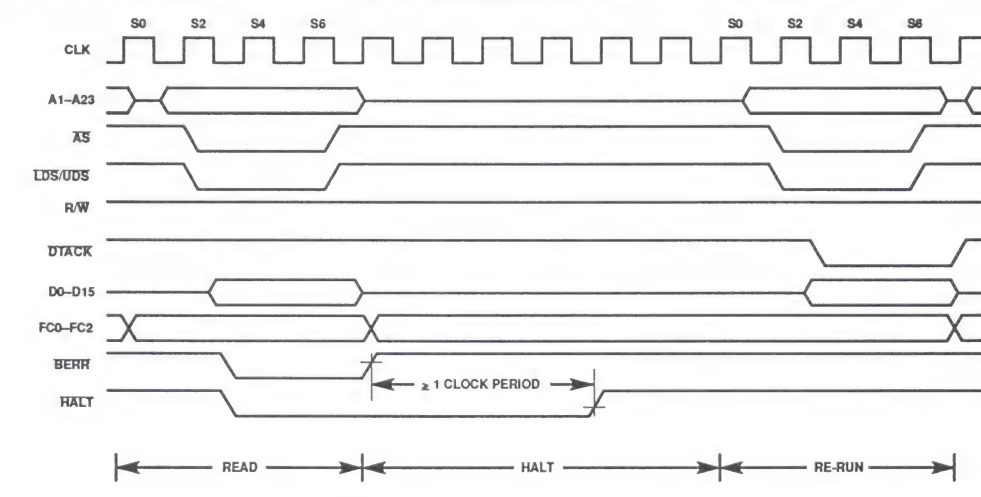



Figure 26. Re-Run Bus Cycle Timing Diagram

Figure 27 details the timing required for correct single-step operations. Some care must be exercised to avoid harmful interactions between the bus error signal and the halt pin when using the single-cycle mode as a debugging tool. This is also true of interactions between the halt and reset lines since these can reset the machine.

When the processor completes a bus cycle after recognizing that the halt signal is active, most 3-State signals are put in the high-impedance state, these include:

1. address lines, and
2. data lines.

This is required for correct performance of the re-run bus cycle operation.

While the processor is honoring the halt request, bus arbitration performs as usual. That is, halting has no effect on bus arbitration. It is the bus arbitration function that removes the control signals from the bus.

The halt function and the hardware trace capability allow the hardware debugger to trace single bus cycles or single instructions at a time. These processor capabilities, along with a software debugging package, give total debugging flexibility.

**Double Bus Faults** — When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row. This is commonly referred to as a double bus fault. When a double bus fault occurs, the processor will halt. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

Note that a bus cycle which is re-run does not constitute a bus error exception and does not contribute to a double bus fault. Note also that this means that as long as the external hardware requests it, the processor will continue to re-run the same bus cycle.

The bus error pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor.

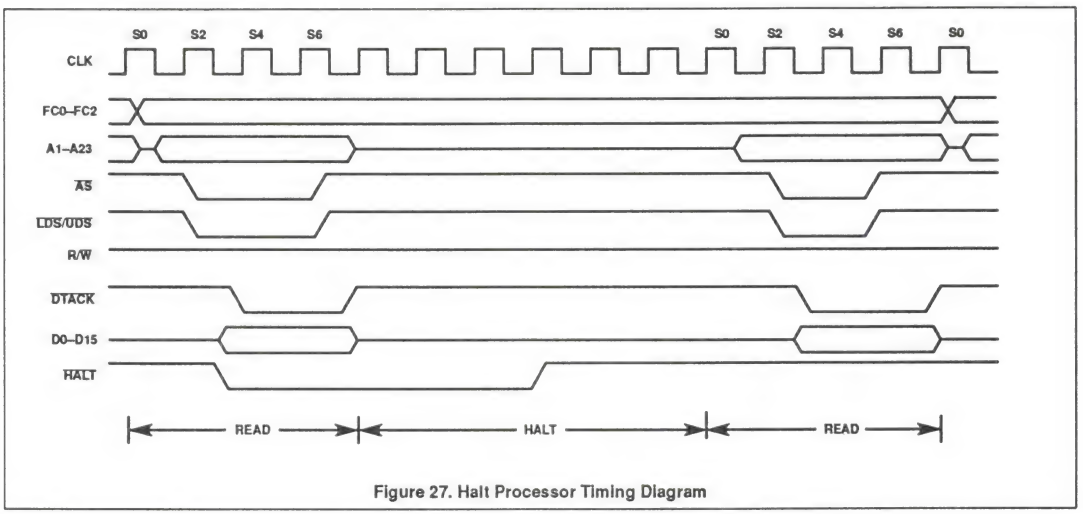



Figure 27. Halt Processor Timing Diagram

**Reset Operation**

The reset signal is a bidirectional signal that allows either the processor or an external signal to reset the system. Figure 28 is a timing diagram for the reset operation. Both the halt and reset lines must be asserted to ensure total reset of the processor.

When the reset and halt lines are driven by an external device, it is recognized as an entire system reset, including the processor. The processor responds by reading the reset vector table entry (vector number zero, address $000000) and loads it into the supervisor stack pointer (SSP). Vector table entry number one at address $000004 is read next and loaded into the program counter. The processor initializes the status register to an interrupt level of seven. No other registers are affected by the reset sequence.

When a reset instruction is executed, the processor drives the reset pin for 124 clock periods. In this case, the processor is trying to reset the rest of the system. Therefore, there is no effect on the internal state of the processor. All of the processor's internal registers and the status register are unaffected by the execution of a reset instruction. All external devices connected to the reset line will be reset at the completion of the reset instruction.

Asserting the reset and halt lines for ten clock cycles will cause a processor reset, except when $V_{CC}$ is initially applied to the processor. In this case, an external reset must be at least 100ms.

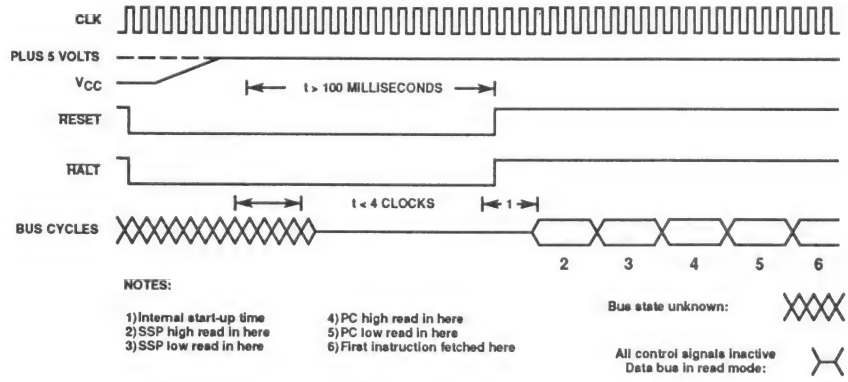



Figure 28. Reset Operation Timing Diagram

### Table 16. DTACK, BERR, and HALT Assertion Results

| CASE NO. | CONTROL SIGNAL | ASSERTED ON RISING EDGE OF STATE | | RESULT |
|---|---|---|---|---|
| | | N | N+2 | |
| 1 | DTACK<br>BERR<br>HALT | A<br>NA<br>NA | S<br>X<br>X | Normal cycle terminate and continue. |
| 2 | DTACK<br>BERR<br>HALT | A<br>NA<br>A | S<br>X<br>S | Normal cycle terminate and halt. Continue when HALT removed. |
| 3 | DTACK<br>BERR<br>HALT | NA<br>NA<br>A | A<br>NA<br>S | Normal cycle terminate and halt. Continue when HALT removed. |
| 4 | DTACK<br>BERR<br>HALT | X<br>A<br>NA | X<br>S<br>NA | Terminate and take bus error trap. |
| 5 | DTACK<br>BERR<br>HALT | NA<br>A<br>NA | X<br>S<br>A | Terminate and re-run. |
| 6 | DTACK<br>BERR<br>HALT | X<br>A<br>A | X<br>S<br>S | Terminate and re-run when HALT removed. |
| 7 | DTACK<br>BERR<br>HALT | NA<br>NA<br>A | X<br>A<br>S | Terminate and re-run when HALT removed. |

**NOTES:**
N–the number of the current even bus state (e.g., S4, S6, etc.)
A–signal is asserted in this bus state
NA–signal is not asserted in this state
X–don't care
S–signal was asserted in previous state and remains asserted in this state

### Table 17. BERR and HALT Negation Results

| CONDITIONS OF TERMINATION | CONTROL SIGNAL | NEGATED ON RISING EDGE OF STATE | | | RESULTS–NEXT CYCLE |
|---|---|---|---|---|---|
| | | N | | N+2 | |
| Bus Error | BERR<br>HALT | •<br>• | or<br>or | •<br>• | Takes bus error trap. |
| Re-run | BERR<br>HALT | •<br>• | or<br>or | •<br>• | Illegal sequence; usually traps to vector number 0. |
| Re-run | BERR<br>HALT | • | | • | Re-runs the bus cycle. |
| Normal | BERR<br>HALT | •<br>• | or | •<br>• | May lengthen next cycle. |
| Normal | BERR<br>HALT | • | or | •<br>none | If next cycle is started it will be terminated as a bus error. |

**NOTE:**
• = Signal is negated in this bus state.

## The Relationship of DTACK, BERR, and HALT

In order to properly control termination of a bus cycle for a re-run or a bus error condition, DTACK, BERR, and HALT should be asserted and negated on the rising edge of the 68000 clock. This will assure that when two signals are asserted simultaneously, the required set-up time (#47) for both of them will be met during the same bus state.

This, or some equivalent precaution, should be designed external to the 68000. Parameter #48 (see AC Electrical Characteristics for # references) is intended to ensure this operation in a totally asynchronous system, and may be ignored if the above conditions are met.

The preferred bus cycle terminations may be summarized as follows (case numbers refer to Table 16):

**Normal Termination:**
DTACK occurs first (Case 1).

**Halt Termination:**
HALT is asserted at the same time or before DTACK and BERR remains negated (Cases 2 and 3):

**Bus Error Termination:**
BERR is asserted in lieu of, at the same time, or before DTACK (Case 4); BERR is negated at the same time or after DTACK.

**Re-Run Termination:**
HALT and BERR are asserted in lieu of, at the same time, or before DTACK (Cases 6 and 7); HALT must be held at least one cycle after BERR. Case 5 indicates BERR may precede HALT.

Table 16 details the resulting bus cycle termination under various combinations of control signal sequences. The negation of these same control signals under several conditions is shown in Table 17 (DTACK is assumed to be negated normally in all cases; for best results, both DTACK and BERR should be negated when address strobe is negated).

**Example A:**
A system uses a watch-dog timer to terminate accesses to unpopulated address space. The timer asserts DTACK and BERR simultaneously after time out (Case 4).

**Example B:**
A system uses error detection on RAM contents. Designer may (a) delay DTACK until data verified and return BERR and HALT simultaneously to re-run error cycle (Case 6), or if valid, return DTACK (Case 1); (b) delay DTACK until data verified and return BERR at same time as DTACK if data in error (Case 4).

## Asynchronous Versus Synchronous Operation

### Asynchronous Operation

To achieve clock frequency independence at a system level, the 68000 can be used in an asynchronous manner. This entails using only the bus handshake lines ($\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DTACK}$, $\overline{BERR}$, $\overline{HALT}$, and $\overline{VPA}$) to control this data transfer. Using this method, $\overline{AS}$ signals the start of a bus cycle and the data strobes are used as a condition for valid data on a write cycle. The slave device (memory or peripheral) then responds by placing the requested data on the data bus for a read cycle or latching data on a write cycle and asserting the data transfer acknowledge signal ($\overline{DTACK}$) to terminate the bus cycle. If no slave responds or the access is invalid, external control logic asserts the $\overline{BERR}$, or $\overline{BERR}$ and $\overline{HALT}$ signal to abort or rerun the bus cycle.

The $\overline{DTACK}$ signal is allowed to be asserted before the data from a slave device is valid on a read cycle. the length of time that $\overline{DTACK}$ may precede data is given as parameter #31 and it must be met in any asynchronous system to insure that valid data is latched into the processor. Notice that there is no maximum time specified from the assertion of $\overline{AS}$ to the assertion of $\overline{DTACK}$. This is because the MPU will insert wait cycles of one clock period each until $\overline{DTACK}$ is recognized.

### Synchronous Operation

To allow for those systems which use the system clock as a signal to generate $\overline{DTACK}$ and other asynchronous inputs, the asynchronous input setup time is given as parameter #47. If this setup is met on an input, such as $\overline{DTACK}$, the processor is guaranteed to recognize that signal on the next falling edge of the system clock. However, the converse is not true—if the input signal does not meet the setup time it is not guaranteed not to be recognized. In addition, if $\overline{DTACK}$ is recognized on a falling edge, valid data will be latched into the processor (on a read cycle) on the next falling edge provided that the data meets the setup time given as parameter #27. Given this, parameter #31 may be ignored. Note that if $\overline{DTACK}$ is asserted, with the required setup time, before the falling edge of S4, no wait states will be incurred and the bus cycle will run at its maximum speed of four clock periods.

**NOTE:** During an active bus cycle, $\overline{VPA}$ and $\overline{BERR}$ is sampled on every falling edge of the clock starting with S2. $\overline{DTACK}$ is sampled on every falling edge of the clock starting with S4 and data is latched on the falling edge of S6 during a read. The bus cycle will then be terminated in S7 except when $\overline{BERR}$ is asserted in the absence of $\overline{DTACK}$, in which case it will terminate one clock cycle later in S9. $\overline{VPA}$ is sampled only on the third falling edge of the system clock before the rising edge of the E clock.

## PROCESSING STATES

This section describes the actions of the 68000 which are outside the normal processing associated with the execution of instructions. The functions of the bits in the supervisor portion of the status register are covered; the supervisor/user bit, the trace enable bit, and the processor interrupt priority mask. Finally, the sequence of memory references and actions taken by the processor on exception conditions are detailed.

The 68000 is always in one of three processing states: normal, exception, or halted. The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of the normal state is the stopped state which the processor enters when a stop instruction is executed. In this state, no further references are made.

The exception processing state is associated with interrupts, trap instructions, tracing, and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

## Privilege States

The processor operates in one of two states of privilege: the "supervisor" state or the "user" state. The privilege state determines which operations are legal, are used to choose between the supervisor stack pointer and the user stack pointer in instruction references, and may be used by an external memory management device to control and translate accesses.

The privilege state is a mechanism for providing security in a computer system, Programs should access only their own code and data areas, and ought to be restricted from accessing information which they do not need and must not modify.

The privilege mechanism provides security by allowing most programs to execute in user state. in this state, the accesses are controlled, and the effects on other parts of the system are limited. The operating system executes in the supervisor state, has access to all resources, and performs the overhead tasks for the user state programs.

### Supervisor State

The supervisor state is the higher state of privilege. For instruction execution, the supervisor state is determined by the S bit of the status register; if the S bit is asserted (high), the processor is in the supervisor state. All instructions can be executed in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly access the supervisor stack pointer.

All exception processing is done in the supervisor state, regardless of the setting of the S bit. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the supervisor stack pointer.

### User State

The user state is the lower state of privilege. For instruction execution, the user state is determined by the S bit of the status register; if the S bit is negated (low), the processor is executing instructions in the user state.

Most instructions execute the same in user state as in the supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the stop instruction or the reset instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole state register are privileged. To aid in debugging programs which are to be used as operating systems, the move to user stack pointer (MOVE to USP) and move from user stack pointer (MOVE from USP) instructions are also privileged.

The bus cycles generated by an instruction executed in the user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in the user privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly, access the user stack pointer.

**Table 18. Bus Cycle Classification**

| FUNCTION CODE OUTPUT | | | REFERENCE CLASS |
|---|---|---|---|
| FC2 | FC1 | FC0 | |
| 0 | 0 | 0 | (Unassigned) |
| 0 | 0 | 1 | User data |
| 0 | 1 | 0 | User program |
| 0 | 1 | 1 | (Unassigned) |
| 1 | 0 | 0 | (Unassigned) |
| 1 | 0 | 1 | Supervisor data |
| 1 | 1 | 0 | Supervisor program |
| 1 | 1 | 1 | Interrupt acknowledge |

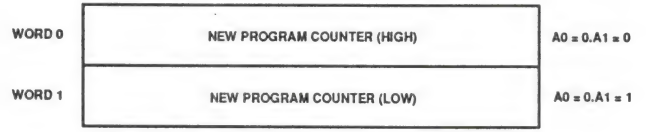
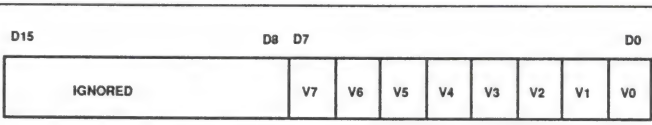



Figure 29. Format of Vector Table Entries




Where:
V7 is the MSB of the vector number.
V8 is the LSB of the vector number.

Figure 30. Vector Number Format

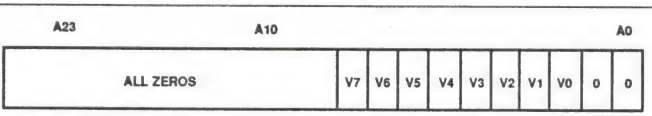



Figure 31. Exception Vector Address Calculation

**Privilege State Changes**

Once the processor is in the user state and executing instructions, only exceptional processing can change the privilege state. During exception processing, the current setting of the S bit of the status register is saved and the S bit is asserted, putting the processor in the supervisor state. Therefore, when instruction execution resumes at the address specified to process the exception, the processor is in the supervisor privilege state.

**Reference Classification**

When the processor makes a reference, it classifies the kind of reference being made, the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor state, such as interrupt acknowledge. Table 18 lists the classification of references.

## Exception Processing

Before discussing the details of interrupts, traps, and tracing, a general description of exception processing is in order. The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made and the status register is set for exception processing. In the second step the exception vector is determined and the third step is the saving of the current processor context. In the fourth step a new context is obtained and the processor switches to instruction processing.

**Exception Vectors**

Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length (Figure 29), except for the reset vector which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an 8–bit number which, when multiplied by four, gives the address of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8–bit vector number (Figure 30) to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 24–bit address, shown in Figure 31. The memory layout for exception vectors is given in Table 19.

**Table 19. Exception Vector Table**

| VECTOR NUMBER(S) | ADDRESS | | | ASSIGNMENT |
|---|---|---|---|---|
| | Dec | Hex | Space | |
| 0 | 0 | 000 | SP | Reset: initial SSP |
| – | 4 | 004 | SP | Reset: initial PC |
| 2 | 8 | 008 | SD | Bus error |
| 3 | 12 | 00C | SD | Address error |
| 4 | 16 | 010 | SD | Illegal instruction |
| 5 | 20 | 014 | SD | Zero divide |
| 6 | 24 | 018 | SD | CHK instruction |
| 7 | 28 | 01C | SD | TRAPV instruction |
| 8 | 32 | 020 | SD | Privilege violation |
| 9 | 36 | 024 | SD | Trace |
| 10 | 40 | 028 | SD | Line 1010 emulator |
| 11 | 44 | 02C | SD | Line 1111 emulator |
| 12* | 48 | 030 | SD | (Unassigned, reserved) |
| 13* | 52 | 034 | SD | (Unassigned, reserved) |
| 14* | 56* | 038 | SD | (Unassigned, reserved) |
| 15 | 60 | 03C | SD | Uninitialized interrupt vector |
| 16–23* | 64 | 04C | SD | (Unassigned, reserved) |
| | 95 | 05F | | – |
| 24 | 96 | 060 | SD | Spurious interrupt |
| 25 | 100 | 064 | SD | Level 1 interrupt autovector |
| 26 | 104 | 068 | SD | Level 2 interrupt autovector |
| 27 | 108 | 06C | SD | Level 3 interrupt autovector |
| 28 | 112 | 070 | SD | Level 4 interrupt autovector |
| 29 | 116 | 074 | SD | Level 5 interrupt autovector |
| 30 | 120 | 078 | SD | Level 6 interrupt autovector |
| 31 | 124 | 07C | SD | Level 7 interrupt autovector |
| 32–47 | 128 | 080 | SD | TRAP instruction vectors |
| | 191 | 0BF | | – |
| 48–63* | 192 | 0C0 | SD | (Unassigned, reserved) |
| | 255 | 0FF | | – |
| 64–255 | 256 | 100 | SD | User interrupt vectors |
| | 1023 | 3FF | | – |

**NOTE:**
* Vector numbers 12, 13, 14, 16 through 23, and 48 through 63 are reserved for future enhancements by Signetics. No user peripheral devices should be assigned these numbers.

As shown in Table19, the memory layout is 512 words long (1024 bytes). It starts at address 0 and proceeds through address 1023. This provides 255 unique vectors; some of these are reserved for TRAPs and other system functions. Of the 255, there are 192 reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the systems designer.

**Kinds of Exceptions**

Exceptions can be generated by either internal or external causes. The externally generated exceptions are the interrupts and the bus error and reset requests. The interrupts are requests from peripheral devices for processor action while the bus error and reset interrupts are used for access control and processor restart. The internally generated exceptions come from instructions, or from address errors or tracing.

The trap (TRAP), trap on overflow (TRAPV), check data register against upper bounds (CHK), and divide (DIV) instructions all can generate exceptions as part of their instruction execution. In addition, illegal instructions, word fetches from odd addresses, and privilege violations cause exceptions. Tracing behaves like a very high–priority internally–generated interrupt after each instruction execution.

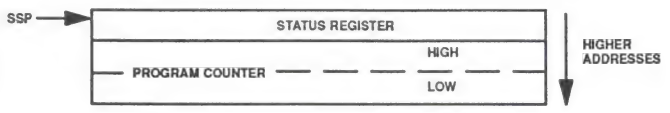



Figure 32. Exception Stack Order (Groups 1 and 2)

## Table 20. Exception Grouping and Priority

| GROUP | EXCEPTION | PROCESSING |
|---|---|---|
| 0 | **Reset**<br>address error<br>bus error | Exception processing begins within two clock cycles |
| 1 | Trace<br>interrupt<br>illegal<br>privilege | Exception processing begins before the next instruction |
| 2 | TRAP, TRAPV,<br>CHK,<br>zero divide | Exception processing is started by normal instruction execution |

**Exception Processing Sequence**

Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S bit is asserted, putting the processor into the supervisor privilege state. Also, the T bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch and classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the address of the exception vector.

The third step is to save the current processor status, except for the reset exception. The current program counter value and the saved copy of the status register are stacked using the supervisor stack pointer as shown in Figure 32. The program counter value stacked usually points to the next unexecuted instruction; however, for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented from the address of the instruction which caused the error. Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

**Multiple Exceptions**

These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The Group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted and the exception processing to commence within two clock cycles.

The Group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The Group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, CHK, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while Group 2 exceptions have lowest priority. Within Group 0, reset has highest priority, followed by bus error and then address error. Within Group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and privilege violation. Since only one instruction can be executed at a time, there is no priority relation within Group 2.

The priority relation between two exceptions determines which is taken, or taken first, if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is aborted. In another example, if an interrupt request occurs during the execution of an instruction while the T bit is asserted, the trace exception has priority, and is processed first. Before instruction processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine. A summary of exception grouping and priority is given in Table 20.

## Exception Processing Detailed Discussion

Exceptions have a number of sources and each exception has processing which is peculiar to it. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

**Reset**

The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered. The processor is forced into the supervisor state and the trace state is forced off. The processor interrupt priority mask is set at level seven. The vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space. Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The power–up/restart code should be pointed to by the initial program counter.

The reset instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

**Interrupts**

Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the

processor. Interrupt priority levels are numbered from one to seven, with level seven being the highest priority. the status register contains a 3–bit mask which indicates the current processor priority, and interrupts are inhibited for all priority levels less than or equal to the current processor priority.

An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not force immediate exception processing, but are made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in the following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. A copy of the status register is saved, the privilege state is sent to the supervisor stack, tracing is suppressed, and the processor priority level is set to the level of the interrupt acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus. If external logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the program counter and status register on the supervisor stack. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine. A flowchart for the interrupt acknowledge sequence is given in Figure 33, a timing diagram is given in Figure 34, and the interrupt processing sequence is shown in Figure 35.

Priority level seven is a special case. Level seven interrupts cannot be inhibited by the interrupt priority mask, thus providing a "non–maskable interrupt" capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven. Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction.

**Uninitialized Interrupt**

An interrupt device asserts $\overline{VPA}$ or provides an interrupt during an interrupt acknowledge cycle to the 68000. If the vector register has not been initialized, the responding 68000 family peripheral will provide vector 15, the uninitialized interrupt vector. This provides a uniform way to recover from a programming error.

**Spurious Interrupt**

If during the interrupt acknowledge cycle no device responds by asserting $\overline{DTACK}$ or $\overline{VPA}$, the bus error line should be asserted to terminate the vector acquisition. The processor separates the processing of this error from bus error by fetching the spurious interrupt vector instead of the bus error vector. The processor then proceeds with the usual exception processing.

**Instruction Traps**

Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

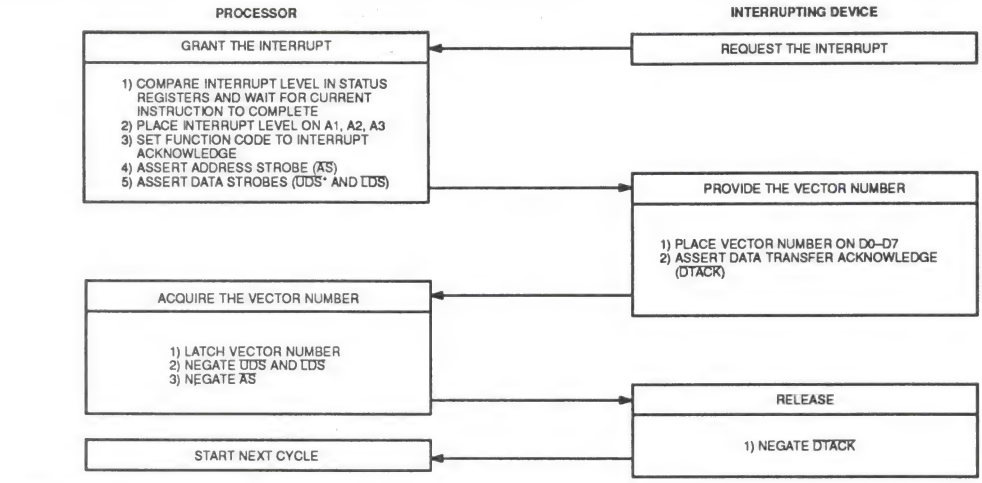
Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception and is useful for implementing system calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithmetic overflow or a subscript out of bounds.

The signed divide (DIVS) and unsigned (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

**Illegal and Unimplemented Instructions**

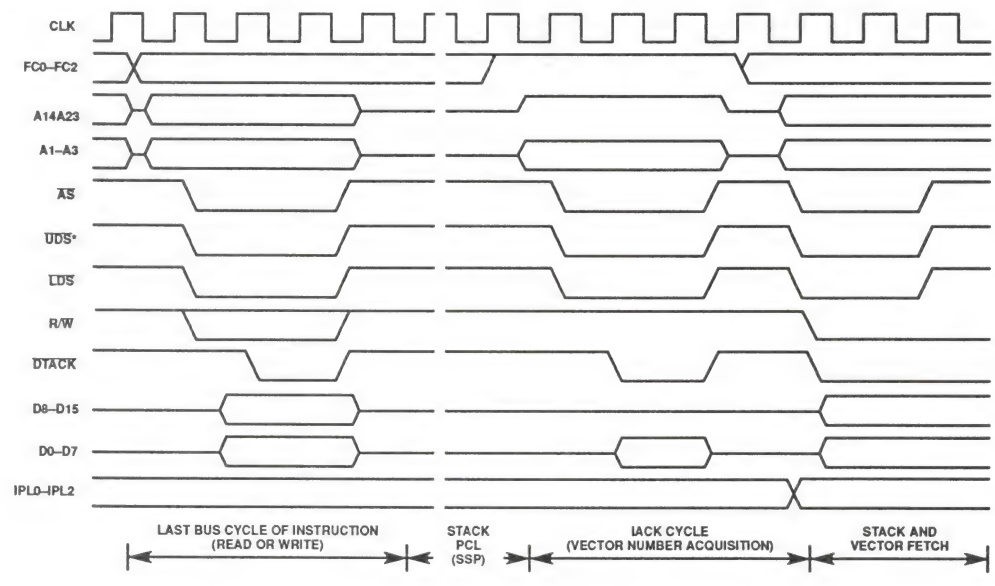
"Illegal instruction" is the term used to refer to any of the word bit patterns which are not the bit pattern of the first word of a legal instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs. Signetics reserves the right to define instructions whose opcodes may be any of the illegal instructions. Three bit patterns will always force an illegal instruction trap on all 68000 family compatible microprocessors. They are: $\overline{4AFA}$, $\overline{4AFB}$, and $\overline{4AFC}$. Two of the patterns, $\overline{4AFA}$ and $\overline{4AFB}$, are reserved for Signetics systems products. The third pattern, $\overline{4AFC}$, is reserved for customer use.

Word patterns with bits 15 through 12 equaling 1010 or 1111 are distinguished as unimplemented instructions and separate exception vectors are given to these patterns to permit efficient emulation. This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.


PROCESSOR
INTERRUPTING DEVICE
GRANT THE INTERRUPT
REQUEST THE INTERRUPT
1) COMPARE INTERRUPT LEVEL IN STATUS REGISTERS AND WAIT FOR CURRENT INSTRUCTION TO COMPLETE
2) PLACE INTERRUPT LEVEL ON A1, A2, A3
3) SET FUNCTION CODE TO INTERRUPT ACKNOWLEDGE
4) ASSERT ADDRESS STROBE (AS)
5) ASSERT DATA STROBES (UDS* AND LDS)
PROVIDE THE VECTOR NUMBER
1) PLACE VECTOR NUMBER ON D0–D7
2) ASSERT DATA TRANSFER ACKNOWLEDGE (DTACK)
ACQUIRE THE VECTOR NUMBER
1) LATCH VECTOR NUMBER
2) NEGATE UDS AND LDS
3) NEGATE AS
RELEASE
1) NEGATE DTACK
START NEXT CYCLE

NOTE:
* Although a vector number is one byte, both data strobes are asserted due to the microcode used for exception. The processor does not recognize anything on data lines D8 through D15 at this time.

**Figure 33. Vector Acquisition Flowchart**




NOTE:
* Although a vector number is one byte, both data strobes are asserted due to the microcode used for exception processing. The processor does not recognize anything on data lines D8 through D15 at this time.

**Figure 34. Interrupt Acknowledge Cycle Timing Diagram**

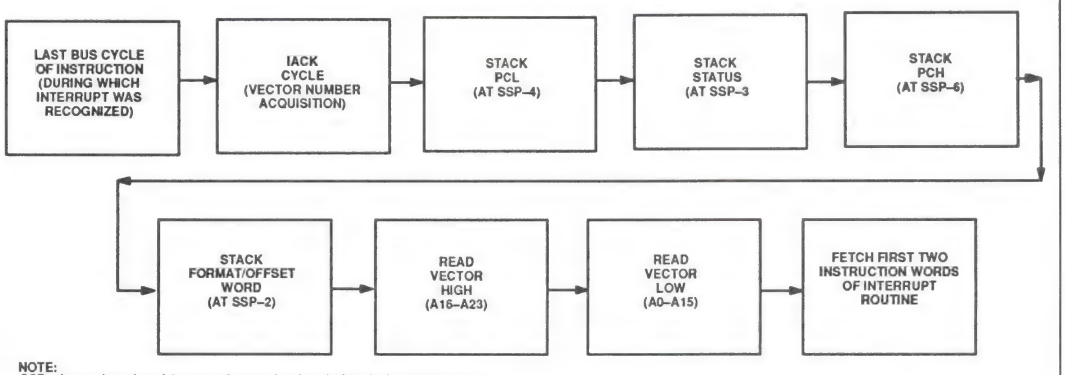

LAST BUS CYCLE OF INSTRUCTION (DURING WHICH INTERRUPT WAS RECOGNIZED)
IACK CYCLE (VECTOR NUMBER ACQUISITION)
STACK PCL (AT SSP–4)
STACK STATUS (AT SSP–3
STACK PCH (AT SSP–6)
STACK FORMAT/OFFSET WORD (AT SSP–2)
READ VECTOR HIGH (A16–A23)
READ VECTOR LOW (A0–A15)
FETCH FIRST TWO INSTRUCTION WORDS OF INTERRUPT ROUTINE
NOTE:
SSP refers to the value of the supervisor stack pointer before the interrupt occurs.

**Figure 35. Interrupt Processing Sequence**

**Privilege Violations**

In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

| | |
|---|---|
| STOP | AND Immediate to SR |
| RESET | EOR Immediate to SR |
| RTE | OR Immediate to SR |
| MOVE to SR | MOVE to USP |

**Tracing**

To aid in program development, the 68000 includes a facility to allow instruction–by–instruction tracing. In the trace state, after each instruction is executed an exception is forced, allowing a debugging program to monitor the execution of the program under test.

The trace facility uses the T but in the supervisor portion of the status register. If the T bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated after the execution of that instruction is completed. If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is indeed executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception. If, during the execution of the instruction an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

**Bus Error**

Bus error exceptions occur when the external logic requests that a bus error be processed by an exception. The current bus cycle which the processor is making is then aborted. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing.

Exception processing for the bus error follows the usual sequence of steps. The status register is copied, the supervisor state is entered, and the trace state is turned off. The vector number is generated to refer to the bus error vector. Since the processor was not between instructions when the bus error exception request was made, the context of the processor is more detailed. To save more of this context, additional information is saved on the supervisor stack. The program counter and the copy of the status register are of course saved. The value saved for the program counter is advanced by some amount, one to five words beyond the address of the first word of the instruction which made the reference causing the bus error. If the bus error occurred during the fetch of the next instruction, the saved program counter has a value in the vicinity of the current instruction, even if the current instruction is a branch, a jump, or a return instruction. Besides the usual information, the processor saves its internal copy of the first word of the instruction being processed and the address which was being accessed by the aborted bus cycle. Specific information about the access is also saved: whether it was a read or a write, whether or not the processor was processing an instruction, and the classification displayed on the function code outputs when the bus error occurred. The processor is processing an instruction if it is in the normal state or processing a Group 2 exception; the processor is not processing an instruction if it is processing a Group 0 or a Group 1 exception. Figure 36 illustrates how this information is organized on the supervisor stack. Although this information is not sufficient in general to effect full recovery from the bus error, it does allow software diagnosis. Finally, the processor commences instruction processing at the address contained in vector number two. It is the responsibility of the error handler routine to clean up the stack and determine where to continue execution.

If a bus error occurs during the exception processing for a bus error, address error, or reset, the processor is halted and all processing ceases. This simplifies the detection of catastrophic system failure, since the processor removes itself from the system rather than destroy any memory contents. Only the RESET pin can restart a halted processor.

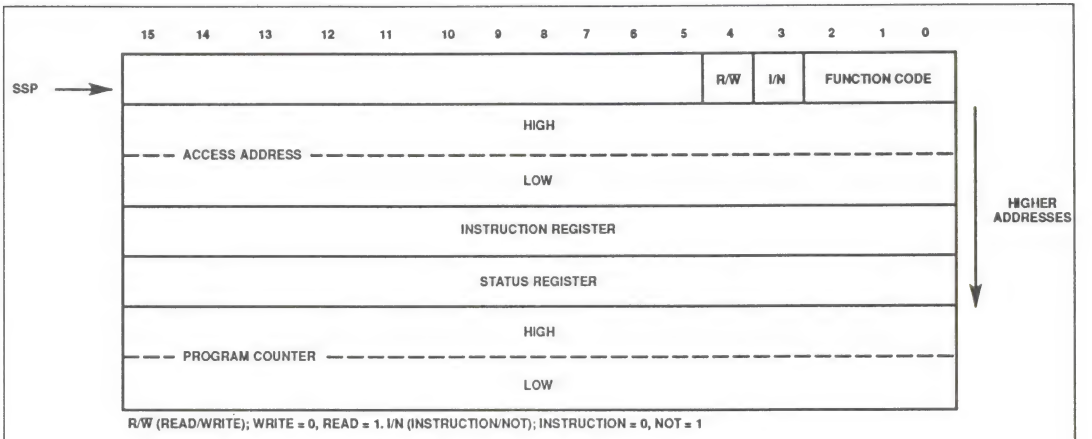


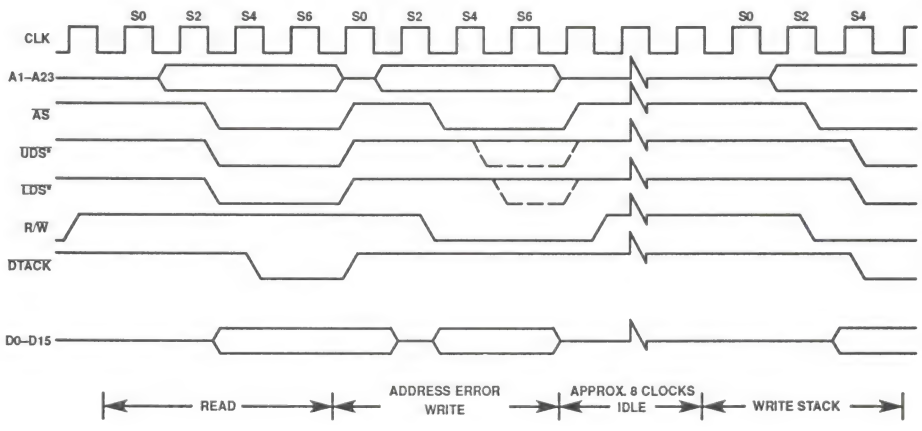

Figure 36 Exception Stack Order (Group 0)

**Address Error**

Address error exceptions occur when the processor attempts to access a word or a long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted and the processor ceases whatever processing it is currently doing and begins exception processing. After the exception processing commences, the sequence is the same as that for bus error including the information that is stacked, except that the vector number refers to the address error vector instead. Likewise, if an address error occurs during the exception processing for a bus error, address error, or reset, the processor is halted. As shown in figure 37, an address error will execute a short bus cycle followed by exception processing.

## INTERFACE WITH SYNCHRONOUS PERIPHERALS

To interface the synchronous peripherals with the asynchronous 68000, the processor modifies its bus cycle to meet the synchronous cycle requirements whenever a synchronous device address is detected. This is possible since both processors use memory mapped I/O. Figure 38 is a flowchart of the interface operation between the processor and synchronous devices.




NOTE:
*UDS and LDS are asserted on mask sets R9M, BF4, T6E, DL6, CC1, and GN7.

Figure 37. Address Error Timing Diagram

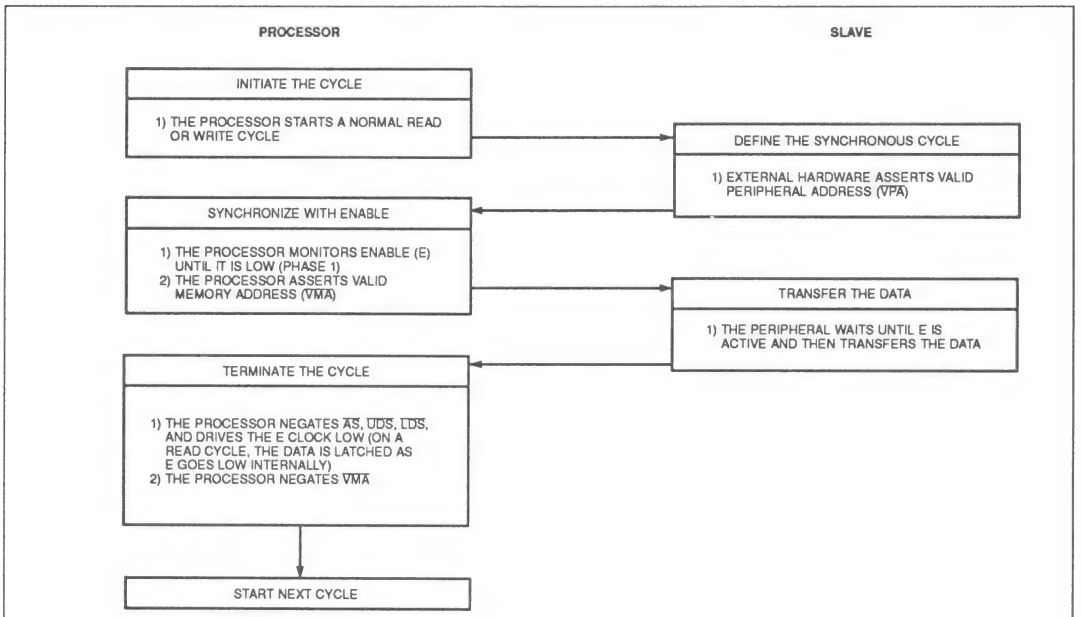

PROCESSOR
SLAVE
INITIATE THE CYCLE
1) THE PROCESSOR STARTS A NORMAL READ OR WRITE CYCLE
DEFINE THE SYNCHRONOUS CYCLE
1) EXTERNAL HARDWARE ASSERTS VALID PERIPHERAL ADDRESS (VPA)
SYNCHRONIZE WITH ENABLE
1) THE PROCESSOR MONITORS ENABLE (E) UNTIL IT IS LOW (PHASE 1)
2) THE PROCESSOR ASSERTS VALID MEMORY ADDRESS (VMA)
TRANSFER THE DATA
1) THE PERIPHERAL WAITS UNTIL E IS ACTIVE AND THEN TRANSFERS THE DATA
TERMINATE THE CYCLE
1) THE PROCESSOR NEGATES AS, UDS, LDS, AND DRIVES THE E CLOCK LOW (ON A READ CYCLE, THE DATA IS LATCHED AS E GOES LOW INTERNALLY)
2) THE PROCESSOR NEGATES VMA
START NEXT CYCLE

**Figure 38. Synchronous Interfacing Flowchart**

## Data Transfer Operation

Three signals on the processor provide the synchronous interface. They are: enable (E), valid memory address ($\overline{VMA}$), and valid peripheral address ($\overline{VPA}$). Enable corresponds to the E or phase 2 signal in existing synchronous systems. The bus frequency is one tenth of the incoming 68000 clock frequency. The timing of E allows 1MHz peripherals to be used with 8MHz 68000s. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive $\overline{VPA}$ accesses on successive E pulses.

Synchronous cycle timing is given in figures 39, 40, 48, and 49. At state zero (S0) in the cycle, the address bus is in the high–impedance state. A function code is asserted on the function code output lines. One–half clock later, in state 1, the address bus is released from the high–impedance state.

During state 2, the address strobe ($\overline{AS}$) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/$\overline{W}$) signal is switched to low (write) during state 2. One–half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus. The processor now inserts wait states until it recognizes the assertion of $\overline{VPA}$.

The $\overline{VPA}$ input signals the processor that the address on the bus is the address of a synchronous device (or an area reserved for synchronous devices) and that the bus should conform to the phase 2 transfer characteristics of the synchronous bus. Valid peripheral address is derived by decoding the address bus, conditioned by the address strobe. Chip select for the synchronous peripherals should be derived by decoding the address bus conditioned by $\overline{VMA}$.

After recognition of $\overline{VPA}$, the processor assures that the enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the synchronous peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal. Figures 39 and 40 depict the best and worst case synchronous cycle timing. This cycle length is dependent strictly on when $\overline{VPA}$ is asserted in relationship to the E clock.

If we assume that external circuitry asserts $\overline{VPA}$ as soon as possible after the assertion of $\overline{AS}$, then $\overline{VPA}$ will be recognized as being asserted on the falling edge of S4. In this case, no "extra" wait cycles will be inserted prior to the recognition of $\overline{VPA}$ asserted and only the wait cycles inserted to synchronize with the E clock will determine the total length of the cycle. In any case, the synchronization delay will be some integral number of clock cycles within the following two extremes:

1. Best Case — $\overline{VPA}$ is recognized as being asserted on the falling edge three clock cycles before E rises (or three clock cycles after E falls).
2. Worst Case — $\overline{VPA}$ is recognized as being asserted on the falling edge two clock cycles before E rises (or four clock cycles after E falls).

During a read cycle, the processor latches the peripheral data in state 6. For all cycles the processor negates the address and data strobes one–half clock cycle later in state 7 and the enable signal goes low at this time. Another half clock later, the address bus is put in the high–impedance state. During a write cycle, the data bus is put in the high–impedance state and the read/write signal is switched high. The peripheral logic must remove $\overline{VPA}$ within one clock after the address strobe is negated.

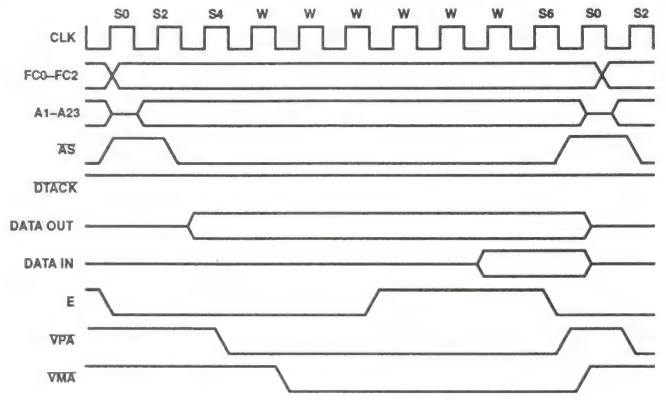



Figure 39. 68000 to Synchronous Peripheral Timing — Best Case

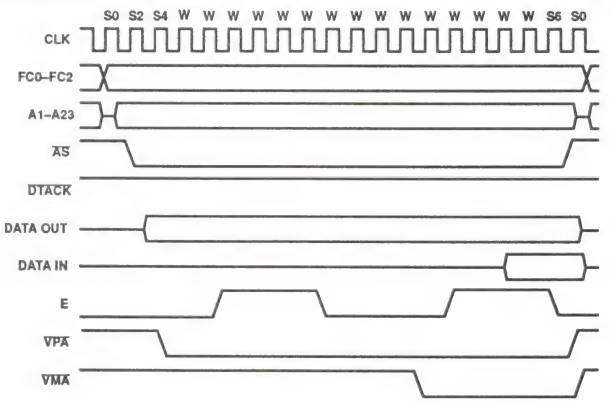



Figure 39. 68000 to Synchronous Peripheral Timing — Worst Case

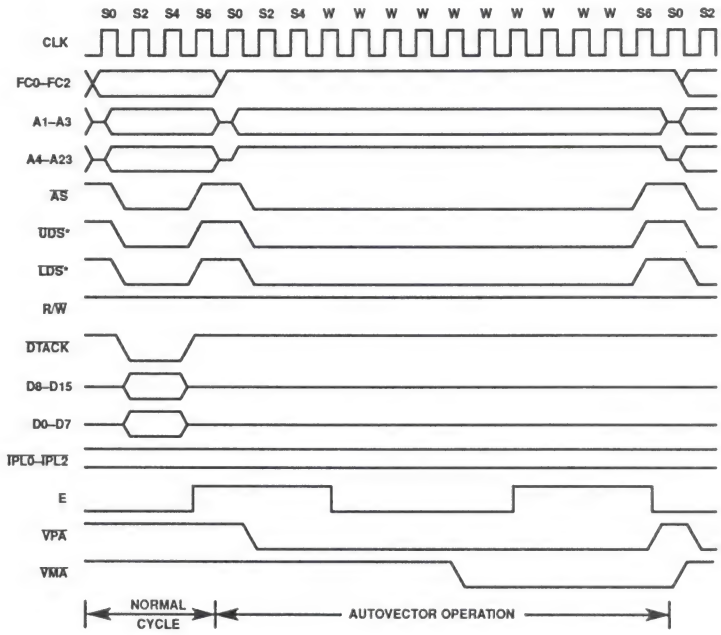
$\overline{\text{DTACK}}$ should not be asserted while $\overline{\text{VPA}}$ is asserted. Notice that the 68000 $\overline{\text{VMA}}$ is active low, contrasted with the active high synchronous $\overline{\text{VMA}}$. This allows the processor to put its buses in the high–impedance state on DMA requests without inadvertently selecting the peripherals.

## Interrupt Interface Operation

During an interrupt cycle while the processor is fetching the vector, the $\overline{\text{VPA}}$ is asserted, the 68000 will assert $\overline{\text{VMA}}$ and complete a normal synchronous read cycle as shown in Figure 41. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is known as autovectoring. The seven autovectors are vector numbers 25 through 31 (decimal).

Autovectoring operates in the same fashion (but is not restricted to) the synchronous interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the synchronous and the 68000's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since $\overline{\text{VMA}}$ is asserted during autovectoring, care should be taken to insure the synchronous peripheral address decoding prevents unintended accesses.




NOTE:
*Although UDS and LDS are asserted, no data is read from the bus during the autovector cycle. The vector number is generated internally.

**Figure 41. Autovector Operation Timing Diagram**

## INSTRUCTION SET AND EXECUTION TIMES

### Instruction Set

The following paragraphs provide information about the addressing categories and instruction set of the 68000.

**Addressing Categories**

Effective address modes may be categorized by the ways in which they may be used. The following classifications will be used in the instruction definitions.

These categories may be combined, so that additional, more restrictive, classifications may be defined. For example, the instruction descriptions use such classifications as alterable memory or data alterable. The former refers to those addressing modes which are both alterable and memory addresses, and the latter refers to addressing modes which are both data and alterable.

Table 21 shows the various categories to which each of the effective address modes belong. Table 22 is the instruction set summary.

Data — If an effective address mode may be used to refer to data operands, it is considered a data addressing effective address mode.

Memory — If an effective address mode may be used to refer to memory operands, it is considered a memory addressing effective address mode.

Alterable — If an effective address mode may be used to refer to alterable (writable) operands, it is considered an alterable addressing effective address mode.

Control — If an effective address mode may be used to refer to memory operands without an associated size, it is considered a control addressing effective address mode.

### Table 21. Effective Addressing Mode Categories

| EFFECTIVE ADDRESS MODES | MODE | REGISTER | ADDRESSING CATEGORIES | | | |
|---|---|---|---|---|---|---|
| | | | Data | Memory | Control | Alterable |
| Dn | 000 | Register number | X | – | – | X |
| An | 001 | Register number | – | – | – | X |
| (An) | 010 | Register number | X | X | X | X |
| (An)+ | 011 | Register number | X | X | – | X |
| –(An) | 100 | Register number | X | X | – | X |
| d(An) | 101 | Register number | X | X | X | X |
| d(An, ix) | 110 | Register number | X | X | X | X |
| xxx.W | 111 | 000 | X | X | X | X |
| xxx.L | 111 | 001 | X | X | X | X |
| d(PC) | 111 | 010 | X | X | X | – |
| d(PC, ix) | 111 | 011 | X | X | X | – |
| #xxx | 111 | 100 | X | X | – | – |

### Table 22. Instruction Set

| MNEMONIC | DESCRIPTION | OPERATION | CONDITION CODES | | | | |
|---|---|---|---|---|---|---|---|
| | | | X | N | Z | V | C |
| ABCD | Add decimal with extend | $(Destination)_{10} + (Source)_{10} + X \rightarrow Destination$ | • | U | • | U | • |
| ADD | Add binary | (Destination) + (Source) → Destination | • | • | • | • | • |
| ADDA | Add address | (Destination) + (Source) → Destination | – | – | – | – | – |
| ADDI | Add immediate | (Destination) + Immediate Data → Destination | • | • | • | • | • |
| ADDQ | Add quick | (Destination) + Immediate Data → Destination | • | • | • | • | • |
| ADDX | Add extended | (Destination) + (Source) + X → Destination | • | • | • | • | • |
| AND | AND logical | (Destination ∧ (Source) → Destination | – | • | • | 0 | 0 |
| ANDI | AND immediate | (Destination) ∧ Immediate Data → Destination | – | • | • | 0 | 0 |
| ANDI to CCR | AND immediate to condition codes | (Source) ∧ CCR → CCR | • | • | • | • | • |
| ANDI to SR | AND immediate to status register | (Source) ∧ SR → SR | • | • | • | • | • |
| ASL, ASR | Arithmetic shift | (Destination) Shifted by <count> → Destination | • | • | • | • | • |
| $B_{cc}$ | Branch conditionally | If $_{CC}$ then PC + d → PC | – | – | – | – | – |
| BCHG | Test a bit and change | ~(<bit number>) OF Destination → Z<br>~(<bit number>) OF Destination →<br><bit number> OF Destination | – | – | • | – | – |
| BCLR | Test a bit and clear | ~(<bit number>) OF Destination → Z<br>0 → <bit number> → OF Destination | – | – | • | – | – |
| BRA | Branch always | PC + d → PC | – | – | – | – | – |
| BSET | Test a bit and set | ~(<bit number>) OF Destination → Z<br>1 → <bit number> OF Destination | – | – | • | – | – |
| BSR | Branch to subroutine | PC → –(SP); PC + d → PC | – | – | – | – | – |
| BTST | Test a bit | ~)<bit number>) OF Destination → Z | – | – | • | – | – |
| CHK | Check register against bounds | If Dn < 0 or Dn >(<ea>) then TRAP | – | • | U | U | U |
| CLR | Clear an operand | 0 → Destination | – | 0 | 1 | 0 | 0 |
| CMP | Compare | (Destination)–(Source) | – | • | • | • | • |
| CMPA | Compare address | (Destination)–(Source) | – | • | • | • | • |
| CMPI | Compare immediate | (Destination)–Immediate Data | – | • | • | • | • |

**Table 22. Instruction Set** (Continued)

| MNEMONIC | DESCRIPTION | OPERATION | CONDITION CODES | | | | |
|---|---|---|---|---|---|---|---|
| | | | X | N | Z | V | C |
| CMPM | Compare memory | (Destination)–(Source) | – | • | • | • | • |
| $DB_{CC}$ | Test condition, decrement and branch | if ~ cc then Dn–1 → Dn; if Dn≠–1 then PC + d → PC | – | – | – | – | – |
| DIVS | Signed divide | (Destination)/(Source) → Destination | – | • | • | • | 0 |
| DIVU | Unsigned divide | (Destination)/(Source) → Destination | – | • | • | • | 0 |
| EOR | Exclusive–OR logical | (Destination)⊕(Source) → Destination | – | • | • | 0 | 0 |
| EORI | Exclusive–OR immediate | (Destination)⊕Immediate Data → Destination | – | • | • | 0 | 0 |
| EORI to CCR | Exclusive–OR immediate to condition codes | (Source)⊕CCR → CCR | • | • | • | • | • |
| EORI to SR | Exclusive–OR immediate to status register | (Source)⊕SR → SR | • | • | • | • | • |
| EXG | Exchange register | Rx ↔ Ry | – | – | – | – | – |
| EXT | Sign extend | (Destination) Sign–extended → Destination | – | • | • | 0 | 0 |
| JMP | Jump | Destination → PC | – | – | – | – | – |
| JSR | Jump to subroutine | PC → –(SP); Destination → PC | – | – | – | – | – |
| LEA | Load effective address | Destination → An | – | – | – | – | – |
| LINK | Link and allocate | An → –(SP); SP → An; SP + Displacement → SP | – | – | – | – | – |
| LSL, LSR | Logical shift | (Destination) Shifted by <count> → Destination | • | • | • | 0 | • |
| MOVE | Move data from source to destination | (Source) → Destination | – | • | • | 0 | 0 |
| MOVE to CCR | Move to condition code | (Source) → CCR | • | • | • | • | • |
| MOVE to SR | Move to status register | (Source) → SR | • | • | • | • | • |
| MOVE from SR | Move from status register | SR → Destination | – | – | – | – | – |
| MOVE USP | Move user stack pointer | USP → An; An → USP | – | – | – | – | – |
| MOVEA | Move address | (Source) → Destination | – | – | – | – | – |
| MOVEM | Move multiple registers | Registers → Destination (Source) → Registers | – | – | – | – | – |
| MOVEP | Move peripheral data | (Source) → Destination | – | – | – | – | – |
| MOVEQ | Move quick | Immediate Data → Destination | – | • | • | 0 | 0 |
| MULS | Signed multiply | (Destination) X (Source) → Destination | – | • | • | 0 | 0 |
| MULU | Unsigned multiply | (Destination) X (Source) → Destination | – | • | • | 0 | 0 |
| NBCD | Negate decimal with extend | $0–(Destination)_{10}–X$ → Destination | • | U | • | U | • |
| NEG | Negate | 0–(Destination) → Destination | • | • | • | • | • |
| NEGX | Negate with extend | 0–(Destination)–X → Destination | • | • | • | • | • |
| NOP | No operation | – | – | – | – | – | – |
| NOT | Logical complement | ~(Destination) → Destination | – | • | • | 0 | 0 |
| OR | Inclusive–OR logical | (Destination) ∨ (Source) → Destination | – | • | • | 0 | 0 |
| ORI | Inclusive–OR immediate | (Destination) ∨ Immediate Data → Destination | – | • | • | 0 | 0 |
| ORI to CCR | Inclusive–OR immediate to conditions codes | (Source) ∨ CCR → CCR | • | • | • | • | • |
| ORI to SR | Inclusive–OR immediate to status register | (Source) ∨ SR → SR | • | • | • | • | • |
| PEA | Push effective address | Destination → –(SP) | – | – | – | – | – |

**Table 22. Instruction Set** (Continued)

| MNEMONIC | DESCRIPTION | OPERATION | CONDITION CODES | | | | |
|---|---|---|---|---|---|---|---|
| | | | X | N | Z | V | C |
| RESET | Reset external devices | – | – | – | – | – | – |
| ROL, ROR | Rotate (without extend) | (Destination) Rotated by <count> → Destination | – | • | • | 0 | • |
| ROXL, ROXR | Rotate with extend | (Destination) Rotated by <count> → Destination | • | • | • | 0 | • |
| RTE | Return from exception | (SP) + → SR; (SP) + → PC | • | • | • | • | • |
| RTR | Return and restore condition codes | (SP) + → CC; (SP) + → PC | • | • | • | • | • |
| RTS | Return from subroutine | (SP) + → PC | – | – | – | – | – |
| SBCD | Subtract decimal with extend | $(Destination)_{10}$–$(Source)_{10}$–X → Destination | • | U | • | U | • |
| $S_{CC}$ | Set according to condition | If $_{CC}$ then 1's → Destination else 0's → Destination | – | – | – | – | – |
| STOP | Load status register and stop | Immediate Data → SR; STOP | • | • | • | • | • |
| SUB | Subtract binary | (Destination)–(Source) → Destination | • | • | • | • | • |
| SUBA | Subtract address | (Destination)–(Source) → Destination | – | – | – | – | – |
| SUBI | Subtract immediate | (Destination)–Immediate Data → Destination | • | • | • | • | • |
| SUBQ | Subtract quick | (Destination)–Immediate Data → Destination | • | • | • | • | • |
| SUBX | Subtract with extend | (Destination)–(Source)–X → Destination | • | • | • | • | • |
| SWAP | Swap register halves | Register [31:16]↔Register [15:0] | – | • | • | 0 | 0 |
| TAS | Test and set an operand | (Destination) Tested → CC; 1 → [7] OF Destination | – | • | • | 0 | 0 |
| TRAP | Trap | PC → –(SSP); SR → –(SSP); (Vector) → PC | – | – | – | – | – |
| TRAPV | Trap on overflow | If V then TRAP | – | – | – | – | – |
| TST | Test and operand | (Destination) Tested → CCC | – | • | • | 0 | 0 |
| UNLK | Unlink | An → SP; (SP) + → An | – | – | – | – | – |

**NOTES:**

[ ] = bit number
⊕ logical exclusive OR
∧ logical AND
∨ logical OR
~ logical complement

• affected
– unaffected
0 cleared
1 set
U undefined

**Instruction Prefetch**

The 68000 uses a two–word tightly–coupled instruction prefetch mechanism to enhance performance. This mechanism is described in terms of the microcode operations involved. If the execution of an instruction is defined to begin when the microroutine for that instruction is entered, some features of the prefetch mechanism can be described.

1. When execution of an instruction begins, the operation word and the word following have already been fetched. The operation word is in the instruction decoder.
2. In the case of multi–word instructions, as each additional word of the instruction is used internally, a fetch is made to the instruction stream to replace it.
3. The last fetch for an instruction from the instruction stream is made when the operation word is discarded and decoding is started on the next instruction.
4. If the instruction is a single–word instruction causing a branch, the second word is not used. But because this word is fetched by the preceding instruction, it is impossible to avoid this superfluous fetch.
5. In the case of an interrupt or trace exception, both words are not used.
6. The program counter usually points to the last word fetched from the instruction stream.

## Instruction Execution Times

The following paragraphs contain listings of the instruction execution times in terms of external clock (CLK) periods. In this timing data, it is assumed that both memory read and write cycle times are four clock periods.

Any wait states caused by a longer memory cycle must be added to the total instruction time. The number of bus read and write cycles for each instruction is also included with the timing data. The timing data is enclosed in parentheses following the execution periods and is shown as (r/w) where r is the number of read cycles and w is the number of write cycles.

**NOTE**

The number of periods includes instruction fetch and all applicable operand fetches and stores.

### Table 23. Effective Address Calculation Times

| ADDRESSING MODE | | BYTE,WORD | LONG |
|---|---|---|---|
| **Register** | | | |
| Dn | Data register direct | 0(0/0) | 0(0/0) |
| An | Address register direct | 0(0/0) | 0(0/0) |
| **Memory** | | | |
| (An) | Address register indirect | 4(1/0) | 8(2/0) |
| (An)+ | Address register indirect with postincrement | 4(1/0) | 8(2/0) |
| –(An) | Address register indirect with predecrement | 6(1/0) | 10(2/0) |
| d(An) | Address register indirect with displacement | 8(2/0) | 12(3/0) |
| d(An,ix)* | Address register indirect with index | 10(2/0) | 14(3/0) |
| xxx.W | Absolute short | 8(2/0) | 12(3/0) |
| xxx.L | Absolute long | 12(3/0) | 16(4/0) |
| d(PC) | Program counter with displacement | 8(2/0) | 12(3/0) |
| d(PC,ix)* | Program counter with index | 10(2/0) | 14(3/0) |
| #xxx | Immediate | 4(1/0) | 8(2/0) |

NOTE:
* The size of the index register (ix) does not affect execution time.

**Effective Address Operand Calculation Timing**

Table 23 lists the number of clock periods required to compute an instruction's effective address. It includes fetching of any extension words, the address computation, and fetching of the memory operand. The number of bus read and write cycles is shown in parentheses as (r/w). Note there are no write cycles involved in processing the effective address.

**Move Instruction Execution Times**

Tables 24 and 25 indicate the number of clock periods for the move instruction. This data includes instruction fetch, operand reads, and operand writes. The number of bus read and write cycles is shown in parentheses as (r/w).

### Table 24. Move Byte Instruction Execution Times

| SOURCE | DESTINATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Dn | An | (An) | (An)+ | –(An) | d(An) | d(An,Ix)* | xxx.W | xxx.L |
| Dn | 4(1/0) | 4(1/0) | 8(1/1) | 8(1/1) | 8(1/1) | 12(2/1) | 14(2/1) | 12(2/1) | 16(3/1) |
| An | 4(1/0) | 4(1/0) | 8(1/1) | 8(1/1) | 8(1/1) | 12(2/1) | 14(2/1) | 12(2/1) | 16(3/1) |
| (An) | 8(2/0) | 8(2/0) | 12(2/1) | 12(2/1) | 12(2/1) | 16(3/1) | 18(3/1) | 16(3/1) | 20(4/1) |
| (An)+ | 8(2/0) | 8(2/0) | 12(2/1) | 12(2/1) | 12(2/1) | 16(3/1) | 18(3/1) | 16(3/1) | 20(4/1) |
| –(An) | 10(2/0) | 10(2/0) | 14(2/1) | 14(2/1) | 14(2/1) | 18(3/1) | 20(3/1) | 18(3/1) | 22(4/1) |
| d(An) | 12(3/0) | 12(3/0) | 16(3/1) | 16(3/1) | 16(3/1) | 20(4/1) | 22(4/1) | 20(4/1) | 24(5/1) |
| d(An,ix)* | 14(3/0) | 14(3/0) | 18(3/1) | 18(3/1) | 18(3/1) | 22(4/1) | 24(4/1) | 22(4/1) | 26(5/1) |
| xxx.W | 12(3/0) | 12(3/0) | 16(3/1) | 16(3/1) | 16(3/1) | 20(4/1) | 22(4/1) | 20(4/1) | 24(5/1) |
| xxx.L | 16(4/0) | 16(4/0) | 20(4/1) | 20(4/1) | 20(4/1) | 24(5/1) | 26(5/1) | 24(5/1) | 28(6/1) |
| d(PC) | 12(3/0) | 12(3/0) | 16(3/1) | 16(3/1) | 16(3/1) | 20(4/1) | 22(4/1) | 20(4/1) | 24(5/1) |
| d(PC,ix)* | 14(3/0) | 14(3/0) | 18(3/1) | 18(3/1) | 18(3/1) | 22(4/1) | 24(4/1) | 22(4/1) | 26(5/1) |
| #xxx | 8(2/0) | 8(2/0) | 12(2/1) | 12(2/1) | 12(2/1) | 16(3/1) | 18(3/1) | 16(3/1) | 20(4/1) |

NOTE:
* The size of the index register (ix) does not affect execution time.

## Table 25. MOVE LONG Instruction Execution Times

| SOURCE | DESTINATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Dn | An | (An) | (An)+ | –(An) | d(An) | d(An,Ix)* | xxx.W | xxx.L |
| Dn | 4(1/0) | 4(1/0) | 12(1/2) | 12(1/2) | 12(1/2) | 16(2/2) | 18(2/2) | 16(2/2) | 20(3/2) |
| An | 4(1/0) | 4(1/0) | 12(1/2) | 12(1/2) | 12(1/2) | 16(2/2) | 18(2/2) | 16(2/2) | 20(3/2) |
| (An) | 12(3/0) | 12(3/0) | 20(3/2) | 20(3/2) | 20(3/2) | 24(4/2) | 26(4/2) | 24(4/2) | 28(5/2) |
| (An)+ | 12(3/0) | 12(3/0) | 20(3/2) | 20(3/2) | 20(3/2) | 24(4/2) | 26(4/2) | 24(4/2) | 28(5/2) |
| –(An) | 14(3/0) | 14(3/0) | 22(3/2) | 22(3/2) | 22(3/2) | 26(4/2) | 28(4/2) | 26(4/2) | 30(5/2) |
| d(An) | 16(4/0) | 1(4/0) | 24(4/2) | 24(4/2) | 24(4/2) | 28(5/2) | 30(5/2) | 28(5/2) | 32(6/2) |
| d(An,ix)* | 18(4/0) | 18(4/0) | 26(4/2) | 26(4/2) | 26(4/2) | 30(5/2) | 32(5/2) | 30(5/2) | 34(6/2) |
| xxx.W | 16(4/0) | 16(4/0) | 24(4/2) | 24(4/2) | 24(4/2) | 28(5/2) | 30(5/2) | 28(5/2) | 32(6/2) |
| xxx.L | 20(5/0) | 20(5/0) | 28(5/2) | 28(5/2) | 28(5/2) | 32(6/2) | 34(6/2) | 32(6/2) | 36(7/2) |
| d(PC) | 16(4/0) | 16(4/0) | 24(4/2) | 24(4/2) | 24(4/2) | 28(5/2) | 30(5/2) | 28(5/2) | 32(5/2) |
| d(PC,ix)* | 18(4/0) | 18(4/0) | 26(4/2) | 26(4/2) | 26(4/2) | 30(5/2) | 32(5/2) | 30(5/2) | 34(6/2) |
| #xxx | 12(3/0) | 12(3/0) | 20(3/2) | 20(3/2) | 20(3/2) | 24(4/2) | 26(4/2) | 24(4/2) | 28(5/2) |

**NOTE:**
* The size of the index register (ix) does not affect execution time.

**Standard Instruction Execution Times**
The number of clock periods shown in Table 26 indicates the time required to perform the operations, store the results, and read the next instruction. The number of bus read and write cycles is shown in parentheses as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

In Table 26 the headings have the following meanings: An = address register operand, DN = data register operand, ea = an operand specified by an effective address, and M = memory effective address operand.

## Table 26. Standard Instruction Execution Times

| INSTRUCTION | SIZE | op<ea>, An◊ | op<ea>, Dn | op Dn, <M> |
|---|---|---|---|---|
| ADD | byte, word | 8(1/0)+ | 4(1/0)+ | 8(1/1)+ |
| | long | 6(1/0)+** | 6(1/0)+** | 12(1/2)+ |
| AND | byte, word | – | 4(1/0)+ | 8(1/1)+ |
| | long | – | 6(1/0)+** | 12(1/2)+ |
| CMP | byte, word | 6(1/0)+ | 4(1/0)+ | – |
| | long | 6(1/0)+ | 6(1/0)+ | – |
| DIVS | – | – | 158(1/0)+* | – |
| DIVU | – | – | 140(1/0)+* | – |
| EOR | byte, word | – | 4(1/0)*** | 8(1/1)+ |
| | long | – | 8(1/0)*** | 12(1/2)+ |
| MULS | – | – | 70(1/0)+* | – |
| MULU | – | – | 70(1/0)+* | – |
| OR | byte, word | – | 4(1/0)+ | 8(1/1)+ |
| | long | – | 6(1/0)+** | 12(1/2)+ |
| SUB | byte, word | 8(1/0)+ | 4(1/0)+ | 8(1/1)+ |
| | long | 6(1/0)+** | 6(1/0)+** | 12(1/2)+ |

**NOTES:**
+ Add effective address calculation time.
◊ Word or long word only.
* Indicates maximum value.
** The base time of 6 clock periods is increased to 8 if the effective address mode is register direct or immediate (effective) address time should also be added).
*** Only available effective address mode is data register direct.
DIVS, DIVU – The divide algorithm used by the 68000 provides less than 10% difference between the best and worst case timings.
MULS, MULU – The multiply algorithm requires 38 + 2n clocks where n is defined as:
MULU: n= the number of ones in the <ea>.
MULS: n = concatenate the <ea> with a zero as the LSB; n is the resultant number of 10 or 01 patterns in the 17-bit source; i.e., worst case happens when the source is $5555.

**Immediate Instruction Execution Times**

The number of clock periods shown in Table 27 includes the time to fetch immediate operands, perform the operations, store the results, and read the next 9operation. The number of bus read and write cycles is shown in parentheses as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

In Table 27, the headings have the following meanings: # = immediate operand, DN = data register operand, An = address register operand, M = memory operand, and SR = status register.

## Table 27. Immediate Instruction Execution Times

| INSTRUCTION | SIZE | op#, Dn | op#, An | op#, M |
|---|---|---|---|---|
| ADDI | byte, word | 8(2/0) | – | 12(2/1)+ |
| | long | 16(3/0) | – | 20(3/2)+ |
| ADDQ | byte, word | 4(1/0) | 8(1/0)* | 8(1/1)+ |
| | long | 8(1/0) | 8(1/0) | 12(1/2)+ |
| ANDI | byte, word | 8(2/0) | – | 12(2/1)+ |
| | long | 16(3/0) | – | 20(3/1)+ |
| CMPI | byte, word | 8(2/0) | – | 8(2/0)+ |
| | long | 14(3/0) | – | 12(3/0)+ |
| EORI | byte, word | 8(2/0) | – | 12(2/1)+ |
| | long | 16(3/0) | – | 20(3/2)+ |
| MOVEQ | long | 4(1/0) | – | – |
| ORI | byte, word | 8(2/0) | – | 12(2/1)+ |
| | long | 16(3/0) | – | 20(3/2)+ |
| SUBI | byte, word | 8(2/0) | – | 12(2/1)+ |
| | long | 16(3/0) | – | 20(3/2)+ |
| SUBQ | byte, word | 4(1/0) | 8(1/0)* | 8(1/1)+ |
| | long | 8(1/0) | 8(1/0) | 12(1/2)+ |

NOTE:
+ add effective address calculation time
* word only

**Single Operand Instruction Execution Times**

Table 28 indicates the number of clock periods for the single operand instructions. The number of bus read and write cycles is shown in parentheses as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

## Table 28. Single Operand Instruction Execution Times

| INSTRUCTION | SIZE | REGISTER | MEMORY |
|---|---|---|---|
| CLR | byte, word | 4(1/0) | 8(1/1)+ |
| | long | 6(1/0) | 12(1/2)+ |
| NBCD | byte | 6(1/0) | 8(1/1)+ |
| NEG | byte, word | 4(1/0) | 8(1/1)+ |
| | long | 6(1/0) | 12(1/2)+ |
| NEGX | byte, word | 4(1/0) | 8(1/1)+ |
| | long | 6(1/0) | 12(1/2)+ |
| NOT | byte, word | 4(1/0) | 8(1/1)+ |
| | long | 6(1/0) | 12(1/2)+ |
| Scc | byte, false | 4(1/0) | 8(1/1)+ |
| | byte, true | 6(1/0) | 8(1/1)+ |
| TAS | byte | 4(1/0) | 10(1/1) |
| TST | byte, word | 4(1/0) | 4(1/0)+ |
| | long | 4(1/0) | 4(1/0)+ |

NOTE:
+ add effective address calculation time

### Shift/Rotate Instruction Execution Times

Table 29 indicates the number of clock periods for the shift and rotate instructions. The number of bus read and write cycles is shown in parentheses as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

**Table 29. Shift/Rotate Instruction Execution Times**

| INSTRUCTION | SIZE | REGISTER | MEMORY |
|---|---|---|---|
| ASR, ASL | byte, word | 6 + 2n(1/0) | 8(1/1)+ |
| | long | 8 + 2n(1/0) | – |
| LSR, LSL | byte, word | 6 + 2n(1/0) | 8(1/1)+ |
| | long | 8 + 2n(1/0) | – |
| ROR, ROL | byte, word | 6 + 2n(1/0) | 8(1/1)+ |
| | long | 8 + 2n(1/0) | – |
| ROXR, ROXL | byte, word | 6 + 2n(1/0) | 8(1/1)+ |
| | long | 8 + 2n(1/0) | – |

NOTE:
+ add effective address calculation time
n is the shift or rotate count

### Bit Manipulation Instruction Execution Times

Table 30 indicates the number of clock periods required for the bit manipulation instructions. The number of bus read and write cycles is shown in parentheses as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

**Table 30. Bit Manipulation Instruction Execution Times**

| INSTRUCTION | SIZE | DYNAMIC | | STATIC | |
|---|---|---|---|---|---|
| | | Register | Memory | Register | Memory |
| BCHG | byte | – | 8(1/1)+ | – | 12(2/1)+ |
| | long | 8(1/0)* | – | 12(2/0)* | – |
| BCLR | byte | – | 8(1/1)+ | – | 12(2/1)+ |
| | long | 10(1/0)+ | – | 14(2/0)* | – |
| BSET | byte | – | 8(1/1)+ | – | 12(2/1)+ |
| | long | 8(1/0)* | – | 12(2/0)* | – |
| BTST | byte | – | 4(1/0)+ | – | 8(2/0)+ |
| | long | 6(1/0) | – | 10(2/0) | – |

NOTES:
+ add effective calculation time
* indicates maximum value

### Conditional Instruction Execution Times

Table 31 indicates the number of clock periods required for the conditional instructions. The number of bus read and write cycles is indicated in parentheses as (r/w). The number of clock periods and the number of read and write cycles must be added respectively to those of the effective address calculation where indicated.

**Table 31. Conditional Instruction Execution Times**

| INSTRUCTION | DISPLACEMENT | BRANCH TAKEN | BRANCH NOT TAKEN |
|---|---|---|---|
| $B_{CC}$ | byte | 10(2/0) | 8(1/0) |
| | word | 10(2/0) | 12(2/0) |
| BRA | byte | 10(2/0) | – |
| | word | 10(2/0) | – |
| BSR | byte | 18(2/2) | – |
| | word | 18(2/2) | – |
| $DB_{CC}$ | CC true | – | 12(2/0) |
| | CC false | 10(2/0) | 14(3/0) |

## Table 32. JMP, JSR, LEA, PEA, and MOVEM Instruction Execution Times

| INSTRUCTION | SIZE | (An) | (An)+ | –(An) | d(An) | d(An, Ix)+ | xxx.W | xxx.L | d(PC) | d(PC,Ix)* |
|---|---|---|---|---|---|---|---|---|---|---|
| JMP | – | 8(2/0) | – | – | 10(2/0) | 14(3/0) | 10(2/0) | 12(3/0) | 10(2/0) | 14(3/0) |
| JSR | – | 16(2/2) | – | – | 18(2/2) | 22(2/2) | 18(2/2) | 20(3/2) | 18(2/2) | 22(2/2) |
| LEA | – | 4(1/0) | – | – | 8(2/0) | 12(2/0) | 8(2/0) | 12(3/0) | 8(2/0) | 12(2/0) |
| PEA | – | 12(1/2) | – | – | 16(2/2) | 20(2/2) | 16(2/2 | 20(3/2) | 16(2/2) | 20(2/2) |
| MOVEM M → R | word | 12 + 4n (3 + n/0) | 12 + 4n (3 + n/0) | – | 16 + 4n (4 + n/0) | 18 + 4n (4 + n/0) | 16 + 4n (4 + n/0) | 20 + 4n (5 + n/0) | 16 + 4n (4 + n/0) | 18 _ 4n (4 + n/0) |
| | long | 12 + 8n (3 + 2n/0) | 12 + 8n 3 + 2n/0) | – | 16 + 8n (4 + 2n/0) | 18 + 8n (4 + 2n/0) | 16 + 8n (4 + 2n/0) | 20 + 8n (5 + 2n/0) | 16 + 8n (4 + 2n/0) | 18 + 8n (4 + 2n/0) |
| MOVEM R → M | word | 8 + 4n (2/n) | – | 8 + 4n (2/n) | 12 + 4n (3/n) | 14 + 4n (3/n) | 12 + 4n (3/n) | 16 + 4n (4/n) | – – | – – |
| | long | 8 + 8n (2/2n) | – – | 8 + 8n (2/2n) | 12 + 8n (3/2n) | 14 + 8n (3/2n) | 12 + 8n (3/2n) | 16 + 8n (4/2n) | – – | – – |

**NOTES:**
n is the number of registers to move
* is the size of the index register (ix) and does not affect the instruction's execution time

### JMP, JSR, LEA, PEA, and MOVEM Instruction Execution Times

Table 32 indicates the number of clock periods required for the jump, jump-to-subroutine, load effective address, push effective address, and move multiple registers instructions. The number of bus read and write cycles is shown in parentheses as (r/w).

### Multi-Precision Instruction Execution Times

Table 33 indicates the number of clock periods for the multi-precision instructions. The number of clock periods includes the time to fetch both operands, perform the operations, store the results, and read the next instructions. The number of read and write cycles is shown in parentheses as (r/w).

In Table 33, the headings have the following meanings: Dn = data register operand and M = memory operand.

## Table 33. Multi-Precision Instruction Times

| INSTRUCTION | SIZE | op Dn, Dn | op M, M |
|---|---|---|---|
| ADDX | byte, word | 4(1/0) | 18(3/1) |
| | long | 8(1/0) | 30(5/2) |
| CMPM | byte, word | – | 12(3/0) |
| | long | – | 20(5/0) |
| SUBX | byte, word | 4(1/0) | 18(3/1) |
| | long | 8(1/0) | 30(5/2) |
| ABCD | byte | 6(1/0) | 18(3/1) |
| SBCD | byte | 6(1/0) | 18(3/1) |

### Table 34. Miscellaneous Instruction Execution Times

| INSTRUCTION | SIZE | REGISTER | MEMORY |
|---|---|---|---|
| ANDI to CCR | byte | 20(3/0) | – |
| ANDI to SR | word | 20(3/0) | – |
| CHK | – | 10(1/0)+ | – |
| EORI to CCR | byte | 20(3/0) | – |
| EORI to SR | word | 20(3/0) | – |
| ORI to CCR | byte | 20(3/0) | – |
| ORI to SR | word | 20(3/0) | – |
| MOVE from SR | – | 6(1/0) | 8(1/1)+ |
| MOVE to CCR | – | 12(2/0) | 12(2/0)+ |
| MOVE to SR | – | 12(2/0) | 12(2/0)+ |
| EXG | – | 6(1/0) | – |
| EXT | word | 4(1/0) | – |
| | long | 4(1/0) | – |
| LINK | – | 16(2/2) | – |
| MOVE from USP | – | 4(1/0) | – |
| MOVE to USP | – | 4(1/0) | – |
| NOP | – | 4(1/0) | – |
| RESET | – | 132(1/0) | – |
| RTE | – | 20(5/0) | – |
| RTR | – | 20(5/0) | – |
| RTS | – | 16(4/0) | – |
| STOP | – | 4(0/0) | – |
| SWAP | – | 4(1/0) | – |
| TRAPV | – | 4(1/0) | – |
| UNLK | – | 12(3/0) | – |

**NOTE:**
+ add effective address calculation time

### Table 35. Move Peripheral Instruction Execution Times

| INSTRUCTION | SIZE | REGISTER→ MEMORY | MEMORY → REGISTER |
|---|---|---|---|
| MOVEP | word | 16(2/2) | 16(4/0) |
| | long | 24(2/4) | 25(6/0) |

**Miscellaneous Instruction Execution Times**
Tables 34 and 35 indicate the number of clock periods for the following miscellaneous instructions. The number of bus read and write cycles is shown in parentheses as (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

**Exception Processing Execution Times**
Table 36 indicates the number of clock periods for exception processing. The number of clock periods includes the time for all stacking,. the vector fetch, and the fetch of the first two instruction words of the handler routine. the number of bus read and write cycles is shown in parentheses as (r/w).

### Table 36. Exception Processing Execution Times

| EXCEPTION | PERIODS |
|---|---|
| Address error | 50(4/7) |
| Bus error | 50(4/7) |
| CHK instruction | 44(5/4)+ |
| Divide by zero | 42(5/4) |
| Illegal instruction | 34(4/3) |
| Interrupt | 44(5/3)* |
| Privilege violation | 34(4/3) |
| $\overline{\text{RESET}}$** | 40(6/0) |
| Trace | 34(4/3) |
| TRAP instruction | 38(4/4) |
| TRAPV instruction | 34(4/3) |

NOTES:
+ add effective address calculation time.
* The interrupt acknowledge cycle is assumed to take four clock periods.
** Indicates the time from when $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ are first sampled as negated to when instruction execution starts.

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage range | –0.3 to +7.0 | V |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $P_D$ | Maximum power dissipation, ($P_D$) | 1.75 | W |
| | Lead temperature (soldering 5 seconds) | 270 | °C |
| $T_J$ | Junction temperature | 150 | °C |
| $\theta_{JC}$ | Thermal resistance, junction to case | 15, dual-in-line | °C/W |
| $\theta_{JA}$ | Thermal resistance, junction to ambient | 30, dual-in-line<br>50, LCC | °C/W |

NOTE:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$).

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$<br>$V_{SS}$ | Supply voltage | 4.75 to 5.25<br>0 | V<br>V |
| $V_{IH}$ | High level input voltage (logic inputs) | 2.0 to $V_{CC}$ | V |
| $V_{IL}$ | Low level input voltage (logic inputs) | GND to 0.8 | V |
| | Minimum high level output voltage | 2.4 | V |
| | Maximum low level output voltage | 0.5 | V |
| | Frequency of operation:<br>68000–6<br>68000–8<br>68000–10 | <br>4.0 to 6.0<br>4.0 to 8.0<br>4.0 to 10.0 | <br>MHz<br>MHz<br>MHz |
| $T_C$ | Case operating temperature range ($T_C$) | –55°C to +110°C | °C |

## DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = 5.0VDC ±5%; $T_C$ =–55°C TO +110°C (see figures 42, 43, and 44)

| SYMBOL | PARAMETER | TEST CONDITIONS –55°C<$T_C$<+110°C, $V_{CC}$=5V ±5% | | LIMITS Min | LIMITS Max | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage all outputs | $I_{OH}$ = –400µA | | 2.4 | | V |
| $V_{OH}$ | High-level output voltage enable only | R pullup = 1.1 kΩ<br>$I_{OH}$ –400µA | | $V_{CC}$–.75 | | V |
| $V_{OL}$ | Low-level output voltage A23-1, FCO-2, $\overline{BG}$ | $I_{OL}$ = 3.2mA | $V_{CC}$ = 4.75V | | 0.5 | V |
| $V_{OL}$ | Low-level output voltage $\overline{HALT}$ | $I_{OL}$ = 1.6mA | $V_{CC}$ = 4.75V | | 0.5 | V |
| $V_{OL}$ | Low-level output voltage $\overline{AS}$, R/$\overline{W}$, D-15-0, $\overline{UDS}$, $\overline{LDS}$, $\overline{VMA}$, E | $I_{OL}$ = 5.3mA | $V_{CC}$ = 4.75V | | 0.5 | V |
| $V_{OL}$ | Low-level output voltage $\overline{RESET}$ | $I_{OL}$ = 5.0mA | $V_{CC}$ = 4.75V | | 0.5 | V |
| $I_{OHZ}$ | High-impedance (off-state) output current (HIGH) | $V_O$ = 2.4V | | | 20 | µA |
| $I_{OLZ}$ | High-impedance (off-state) output current (LOW) | $V_O$ = 0.4V | | | –20 | µA |
| $I_{IH}$ | High-level input current; all inputs[1] | $V_{IN}$ = 5.25V | | | 2.5 | µA |
| $I_{IL}$ | Low-level input current; all inputs[1] | $V_{IN}$ = 0 | | | 2.5 | µA |
| $I_{CC}$ | Supply current[2] | $V_{CC}$ = 5.25V | | | 333 | mA |
| $C_{IN}$ | Capacitance[3] | $V_{IN}$ = 0V<br>frequency = 1MHz | | | 20 | pF |

## Power Considerations

The average chip-junction temperature, $T_J$, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A$ = ambient temperature, °C
$\theta_{JA}$ = package thermal resistance, junction-to-ambient, °C/W
$P_D$ = $P_{INT} + P_{I/O}$
$P_{INT}$ = $I_{CC} \times V_{CC}$, watts-chip internal power
$P_{I/O}$ = power dissipation on input and output pins — user determined

For most applications $P_{I/O} << P_{INT}$ and can be neglected..

An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K + (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = T_D \bullet (T_A + 273°C) + \bullet_{JA} \bullet P_D 2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

Figure 45 illustrates the graphic solution to the equations, given above, for the specification power dissipations of 1.50 and 1.75 watts over the ambient temperature range of –55°C to 125°C using an average $\theta_{JA}$ of 40°C/W to represent various 68000 packages.

However, actual $\theta_{JA}$'s in the range of 30°C to 50°C/W only change the curves slightly.

The total thermal resistance of a package ($\theta_{JA}$) can be separated into two components, $\theta_{JC}$ and $\theta_{CA}$, representing the barrier to heat flow from the semiconductor junction to the package (case) surface ($\theta_{JC}$) and from the case to the outside ambient ($\theta_{CA}$). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

$\theta_{JC}$ is a device related and cannot be influenced by the user. However, $\theta_{CA}$ is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convention. Thus, good thermal management on the part of the user can significantly reduce $\theta_{CA}$ so that $\theta_{JA}$ approximately equals $\theta_{JC}$. Substitution of $\theta_{JC}$ for $\theta_{JA}$ in equation (1) will result in a lower semiconductor junction temperature.

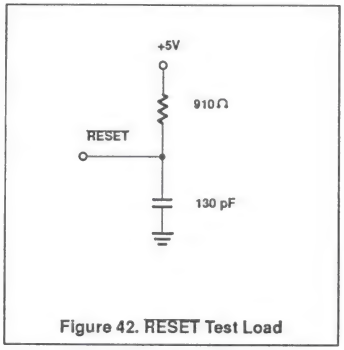



Figure 42. RESET Test Load

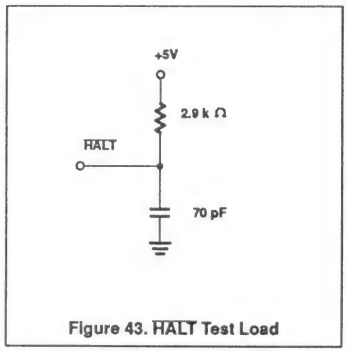



Figure 43. HALT Test Load

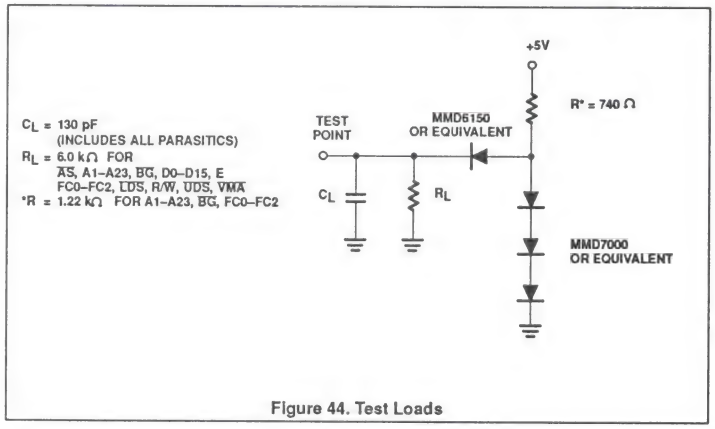



Figure 44. Test Loads

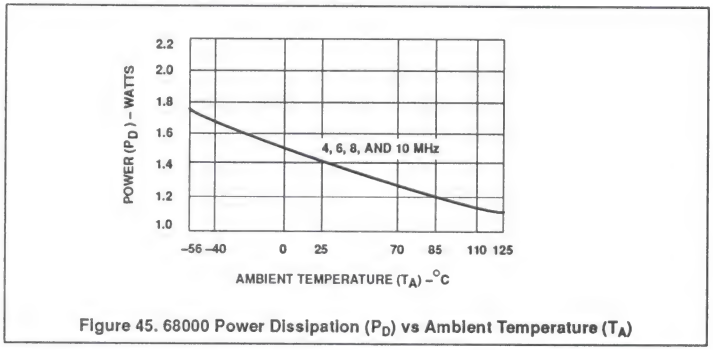



Figure 45. 68000 Power Dissipation ($P_D$) vs Ambient Temperature ($T_A$)

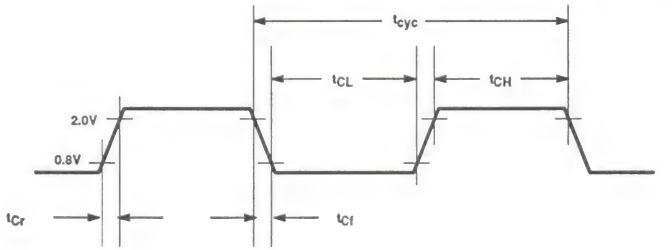
Values for thermal resistance presented in this data sheet are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

## AC ELECTRICAL CHARACTERISTICS — Clock Timing (see Figure 46)

| CHARACTERISTIC | SYMBOL | 6MHz | | 8MHz | | 10MHz | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Frequency of operation | F | | 6.0 | | 8.0 | | 10.0 | MHz |
| Cycle time | $t_{cyc}$ | 167 | 250 | 125 | 250 | 100 | 250 | ns |
| Clock pulse width | $t_{CL}$<br>$t_{CH}$ | 75<br>75 | 125<br>125 | 55<br>55 | 125<br>125 | 45<br>45 | 125<br>125 | ns<br>ns |
| Rise and fall times | $t_{Cr}$<br>$t_{Cf}$ | –<br>– | 10<br>10 | –<br>– | 10<br>10 | –<br>– | 10<br>10 | ns<br>ns |

## 37. Maximum Power Dissipation by Package Type Modes

| PACKAGE TYPE | TEMPERATURE (°C) | MAXIMUM POWER DISSIPATION (WATTS) PER FREQUENCY (MHz) | |
|---|---|---|---|
| | | 6/8MHz | 10MHz |
| Ceramic | 0 to 70<br>–40 to 85 | 1.50<br>1.65 | 1.50<br>1.65 |
| Plastic | 0 to 70<br>–40 to 85 | 1.50<br>1.65 | 1.50<br>1.65 |
| Pin grid array | 0 to 70<br>–40 to 85 | 1.50<br>1.65 | 1.50<br>1.65 |
| Plastic LCC | 0 to 70 | 1.50 | 1.50 |




NOTE:

Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2V.

Figure 46. Clock Input Timing Diagram

## AC ELECTRICAL CHARACTERISTICS[1]—Read and Write Cycles $-55°C \leq T_C \leq +110°C$ (See Figures 47 and 48)

| NO. | SYMBOL | CHARACTERISTIC | 6MHz | | 8MHz | | 10MHz | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | $t_{CYC}$ | Clock Period | 167 | 250 | 125 | 250 | 100 | 250 | ns |
| 2 | $t_{CL}$ | Clock width low | 75 | 125 | 55 | 125 | 45 | 125 | ns |
| 3 | $t_{CH}$ | Clock width high | 75 | 125 | 55 | 125 | 45 | 125 | ns |
| 4 | $t_{Cf}$ | Clock fall time | – | 10 | – | 10 | – | 10 | ns |
| 5 | $t_{Cr}$ | Clock rise time | – | 10 | – | 10 | – | 10 | ns |
| 6 | $t_{CLAV}$ | Clock low to address valid | – | 80 | – | 70 | – | 60 | ns |
| 6A | $t_{CHFCV}$ | Clock high to FC valid | – | 80 | – | 70 | – | 60 | ns |
| 7[7] | $t_{CHAZx}$ | Clock high to address data high impedance (maximum) | – | 100 | – | 80 | – | 70 | ns |
| 8[8] | $t_{CHAZn}$ | Clock high to address/FC invalid (minimum) | 0 | – | 0 | – | 0 | – | ns |
| 9[9] | $t_{CHSLx}$ | Clock high to $\overline{AS}$, $\overline{DS}$ low (maximum) | – | 70 | 0 | 60 | 0 | 55 | ns |
| 10[10] | $t_{CHSLn}$ | Clock high to $\overline{AS}$, $\overline{DS}$ low (minimum) | – | – | – | – | – | – | ns |
| 11[11] | $t_{AVSL}$ | Address valid to $\overline{AS}$, $\overline{DS}$ (read) low/$\overline{AS}$ write | 35 | – | 30 | – | 20 | – | ns |
| 11A[7,11] | $t_{FCVSL}$ | FC valid to $\overline{AS}$, $\overline{DS}$ (read) low/$\overline{AS}$ (write) | 70 | – | 60 | – | 50 | – | ns |
| 12[9] | $t_{CLSH}$ | Clock low to $\overline{AS}$, $\overline{DS}$ high | – | 80 | – | 70 | – | 55 | ns |
| 13[7,11] | $t_{SHAZ}$ | $\overline{AS}$, $\overline{DS}$ high to address/FC invalid | 40 | – | 30 | – | 20 | – | ns |
| 14[7,11] | $t_{SL}$ | $\overline{AS}$, $\overline{DS}$ width low (read)/$\overline{AS}$ (write) | 337 | – | 240 | – | 195 | – | ns |
| 14A[7,11] | $t_{DWPW}$ | $\overline{DS}$ width low (write) | 170 | – | 115 | – | 95 | – | ns |
| 15[7,11] | $t_{SH}$ | $\overline{AS}$, $\overline{DS}$ width high | 180 | – | 150 | – | 105 | – | ns |
| 16[7] | $t_{CHSZ}$ | Clock high to $\overline{AS}$,$\overline{DS}$ high impedance | – | 100 | – | 80 | – | 70 | ns |
| 17[7,11] | $t_{SHRH}$ | $\overline{AS}$, $\overline{DS}$ high to R/$\overline{W}$ high | 50 | – | 40 | – | 20 | – | ns |
| 18[9] | $t_{CHRHx}$ | Clock high to R/$\overline{W}$ high (maximum) | – | 80 | – | 70 | – | 60 | ns |
| 19[10] | $t_{CHRHn}$ | Clock high to R/$\overline{W}$ high (minimum) | – | – | – | – | – | – | ns |
| 20[9] | $t_{CHRL}$ | Clock high to R/$\overline{W}$ low | – | 80 | – | 70 | – | 60 | ns |
| 20A[7,15] | $t_{ASRV}$ | $\overline{AS}$ low to R/$\overline{W}$ valid | – | 20 | – | 20 | – | 20 | ns |
| 21[7,11] | $t_{AVRL}$ | Address valid to R/$\overline{W}$ low | 25 | – | 20 | – | 0 | – | ns |
| 21A[7,11] | $t_{FCVRL}$ | FC valid to R/$\overline{W}$ low | 70 | – | 60 | – | 50 | – | ns |
| 22[7,11] | $t_{RLSL}$ | R/$\overline{W}$ low to $\overline{DS}$ low (write) | 140 | – | 80 | – | 50 | – | ns |
| 23 | $t_{CLDO}$ | Clock low to data out valid | – | 80 | – | 70 | – | 55 | ns |
| 24[13] | $t_{CHRZ}$ | Clock high to R/$\overline{W}$, $\overline{VMA}$ high impedance | – | – | – | – | – | – | ns |
| 25[7,11] | $t_{SHDO}$ | $\overline{DS}$ high to data out invalid | 40 | – | 30 | – | 20 | – | ns |
| 26[11] | $t_{DOSL}$ | Data out valid to $\overline{DS}$ low (write) | 35 | – | 30 | – | 20 | – | ns |
| 27[7,17] | $t_{DICL}$ | Data in to clock low (setup time) | 25 | – | 15 | – | 10 | – | ns |
| 28[7,11] | $t_{SHDAH}$ | $\overline{AS}$, $\overline{DS}$ high to $\overline{DTACK}$ high | 0 | 167 | 0 | 125 | 0 | 100 | ns |
| 29[7] | $t_{SHDI}$ | $\overline{DS}$ high to data invalid (hold time) | 0 | – | 0 | – | 0 | – | ns |
| 30[7] | $t_{SHBEH}$ | $\overline{AS}$, $\overline{DS}$ high to $\overline{BERR}$ high | 0 | – | 0 | – | 0 | – | ns |
| 31[7,11,17] | $t_{DALDI}$ | $\overline{DTACK}$ low to data valid (Setup time) | – | 120 | – | 90 | – | 65 | ns |
| 32[7] | $t_{RH,f}$ | $\overline{HALT}$ and $\overline{RESET}$ input transition time | 0 | 200 | 0 | 200 | 0 | 200 | ns |
| 33 | $t_{CHGL}$ | Clock high to $\overline{BG}$ low | – | 80 | – | 70 | – | 60 | ns |
| 34[7] | $t_{CHGH}$ | Clock high to $\overline{BG}$ high | – | 80 | – | 70 | – | 60 | ns |
| 35[7] | $t_{BRLGL}$ | $\overline{BR}$ low to $\overline{BG}$ low | 1.5 | 3.5 | 1.5 | 3.5 | 1.5 | 3.5 | Clk. per. |

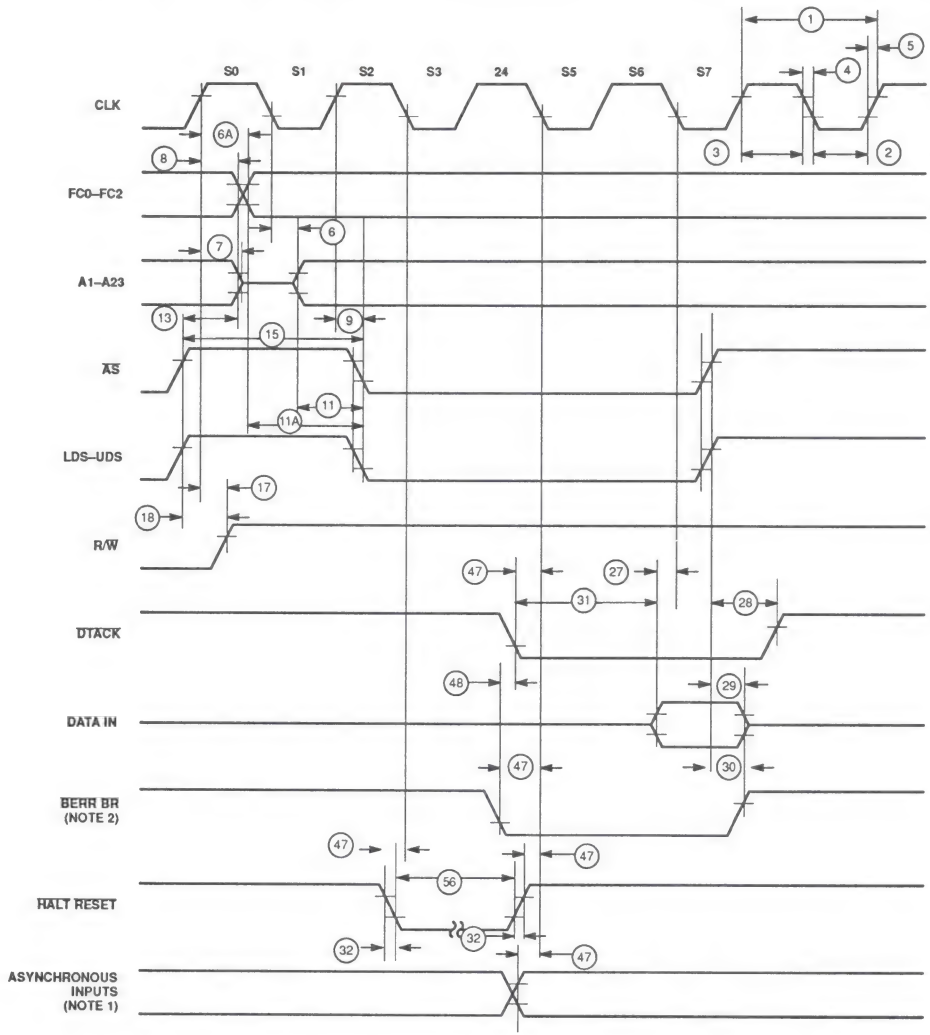
## AC ELECTRICAL CHARACTERISTICS[1]—Read and Write Cycles (Continued)

| NO. | SYMBOL | CHARACTERISTIC | 6MHz | | 8MHz | | 10MHz | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 36[7,18] | $t_{BRHGH}$ | $\overline{BR}$ high to $\overline{BG}$ high | 1.5 | +100 | 1.5 | +90 | 1.5 | +80 | Clk. per. |
| 37[7] | $t_{GALGH}$ | $\overline{BGACK}$ low to $\overline{BG}$ low | 1.5 | NS | 1.5 | NS | 1.5 | NS | Clk. per. |
| 37A[7] | $t_{BGKBR}$ | $\overline{BGACK}$ low to $\overline{BR}$ high (to prevent rearbitration) | 20ns | 1.5 | 20ns | 1.5 | 20ns | 1.5 | Clk. per. |
| 38[7] | $t_{GLZ}$ | $\overline{BG}$ low to bus high impedance (with $\overline{AS}$ high) | – | 100 | – | 80 | – | 70 | ns |
| 39[7] | $t_{GH}$ | $\overline{BG}$ width high | 1.5 | – | 1.5 | – | 1.5 | – | Clk. per. |
| 40 | $t_{CLVML}$ | Clock low to $\overline{VMA}$ low | – | 80 | – | 70 | – | 70 | ns |
| 41 | $t_{CLC}$ | Clock low to E transition | – | 85 | – | 70 | – | 55 | ns |
| 42[7] | $t_{Er,f}$ | E output rise and fall time | – | 25 | – | 25 | – | 25 | ns |
| 43[7] | $t_{VMLEH}$ | $\overline{VMA}$ low to E high | 240 | – | 200 | – | 150 | – | ns |
| 44[7] | $t_{SHVPH}$ | $\overline{AS}$, $\overline{DS}$ high to $\overline{VPA}$ high | 0 | 160 | 0 | 120 | 0 | 90 | ns |
| 45[7] | $t_{ELAI}$ | E low to address /$\overline{VMA}$/FC invalid | 35 | – | 30 | – | 10 | – | ns |
| 46[7] | $t_{BGL}$ | $\overline{BGACK}$ width | 1.5 | – | 1.5 | – | 1.5 | – | Clk. per. |
| 47[17] | $t_{ASI}$ | Asynchronous input setup time | 25 | – | 20 | – | 20 | – | ns |
| 48[7,14] | $t_{BELDAL}$ | $\overline{BERR}$ low to $\overline{DTACK}$ low | 25 | – | 20 | – | 20 | – | ns |
| 49[7] | $t_{ELSI}$ | E low to $\overline{AS}$, $\overline{DS}$ invalid | –80 | +80 | –70 | +70 | –55 | +55 | ns |
| 50[7] | $t_{EH}$ | E width high | 600 | – | 450 | – | 350 | – | ns |
| 51[7] | E width low | $t_{EL}$ | 900 | – | 700 | – | 550 | – | ns |
| 52[7,16] | $t_{CIEHX}$ | E extended rise time | – | – | – | – | – | – | ns |
| 53[7] | $t_{CHDO}$ | Data hold from clock high | 0 | – | 0 | – | 0 | – | ns |
| 54[5,7] | $t_{ELDOZ}$ | Data hold from E low (write) | 40 | – | 30 | – | 20 | – | ns |
| 55[7] | $t_{RLDO}$ | R/$\overline{W}$ to data bus impdeance change | 35 | – | 30 | – | 20 | – | ns |
| 56[7,12] | $r_{HRPW}$ | $\overline{HALT}$/$\overline{RESET}$ pulse width | 10 | – | 10 | – | 10 | – | Clk. per. |
| 57 | $t_{GABD}$ | $\overline{BGACK}$ high to control bus driven | 1.5 | – | 1.5 | – | 1.5 | – | Clk. per. |
| 58[18] | $t_{GHBD}$ | $\overline{BG}$ high to control bus driven | 1.5 | – | 1.5 | – | 1.5 | – | Clk. per. |

**NOTES:**

1. After $V_{CC}$ has been applied for 100 ms.
2. All outputs unloaded except for load capacitance. Clock should be either 4MHz or $F_{MAX}$. Low; HALT, RST, (Part is held in reset). High; $\overline{DTACK}$, BR, BGACK, IPLQ-2, VPA, BERR.
3. Guaranteed but not tested.
4. $V_{CC} = 5V \pm 5\%$
5. After $V_{CC}$ has been applied for 100ms.
6. All outputs unloaded except for load capacitance. Clock should be either 4MHz or $F_{MAX}$. Low; $\overline{HALT}$, $\overline{RST}$, (Part is held in reset). High; $\overline{DTACK}$, BR, BGACK, IPLQ–2, VPA, BERR.
7. As a minimum, tested initially and for process or design changes only.
8. For invalid, as a minimum, tested initially and for process and design changes only.
9. For a loading capacitance of less than or equal to 50pF, subtract 5ns from the values given in the maximum column.
10. Combined with the above parameter. Previous specification of 0ns was theoretical and not attainable.
11. Actual value depends on clock period.
12. For power up, the MPU must be held in RESET state for 100ms to all stabilization of on–chip circuitry. After the system is powered up, 56 refers to the minimum pulse width required to reset the system.
13. Combined with 16, control bus specification
14. If 47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, 48 may be 0ns.
15. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 10ns from the values given in these columns.
16. Deleted, useful only if E clock used to drive clock input on MC6809 Microprocessor.
17. If the asynchronous setup time (47) requirements are satisfied, the $\overline{DTACK}$ low to data setup time (#31) requirement can be ignored. the data must only satisfy the data in to clock–low setup time (#27) for the following cycle.
18. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BTACK}$.

These waveforms should only be referenced in regard to the edge–to–edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

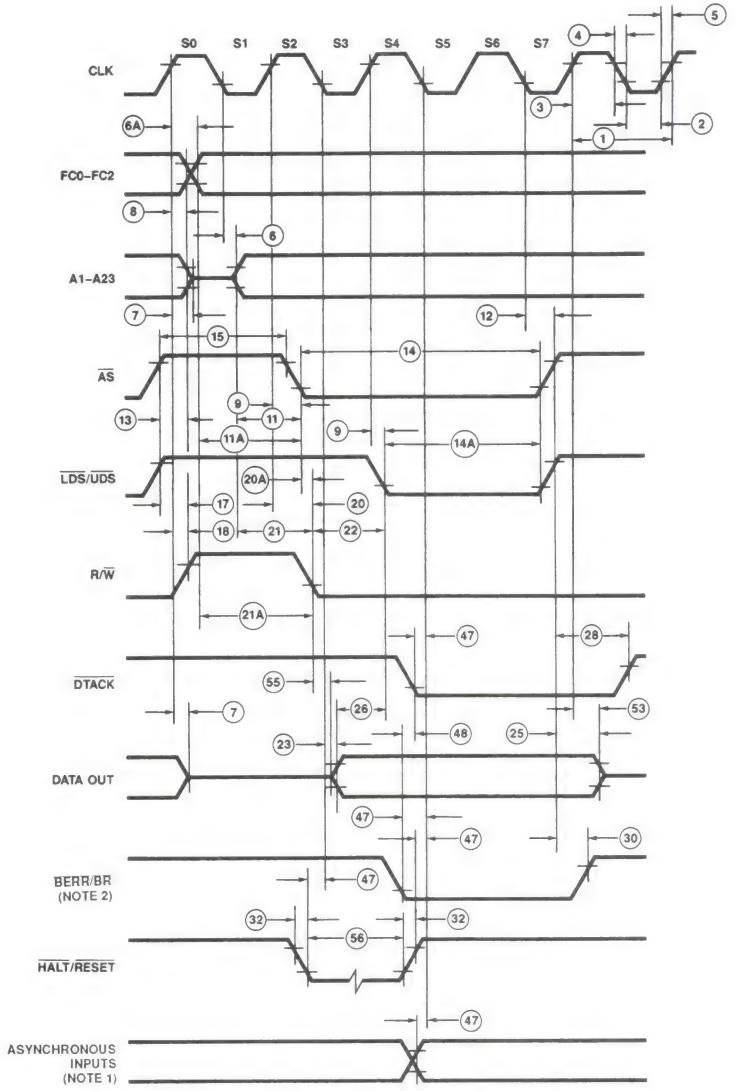



NOTES:

1. Setup time for the asynchronous inputs BGACK, IPL0–2, and VPA guarantees their recognition at the next falling edge of the clock.
2. BR need fall at this time only in order to insure being recognized at the end of this bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.

Figure 47. Write Cycle Timing Diagram

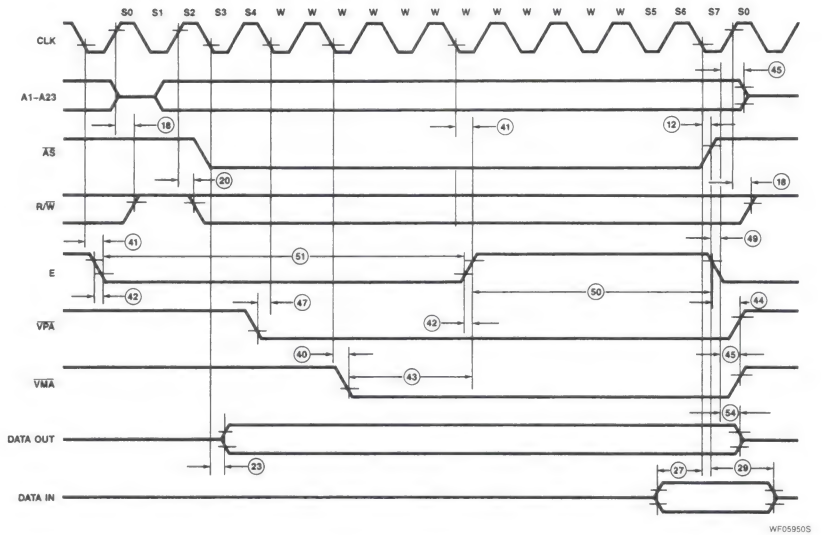
These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.




**NOTES:**

1. Timing measurements are referenced to and from a low voltage of 0.8V and a high voltage of 2.0V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8V and 2.0V.
2. Because of loading variations, R/W may be valid after AS even though both are initiated by the rising edge of S2 (Specification 20A).

**Figure 48. Write Cycle Timing Diagram (Continued)**




**NOTE:**

**This timing diagram is included for those who wish to design their own circuit to generate VMA. It shows the best case possible attainable.**

Figure 49. 68000 to M6800 Peripheral Timing Diagram — Best Case

Figures 50, 51, and 52 depict the three bus arbitration cases that can arise. Figure 50 shows the timing where $\overline{AS}$ is negated when the processor asserts $\overline{BG}$ (idle bus case). Figure 51 shown the timing where $\overline{AS}$ is asserted when the processor asserts $\overline{BG}$ (active bus case). Figure 52 shows the timing where more than one bus master are requesting the bus. Refer to **Bus Arbitration** for a complete discussion of bus arbitration.

The waveforms shown in Figures 50, 51, and 52 should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

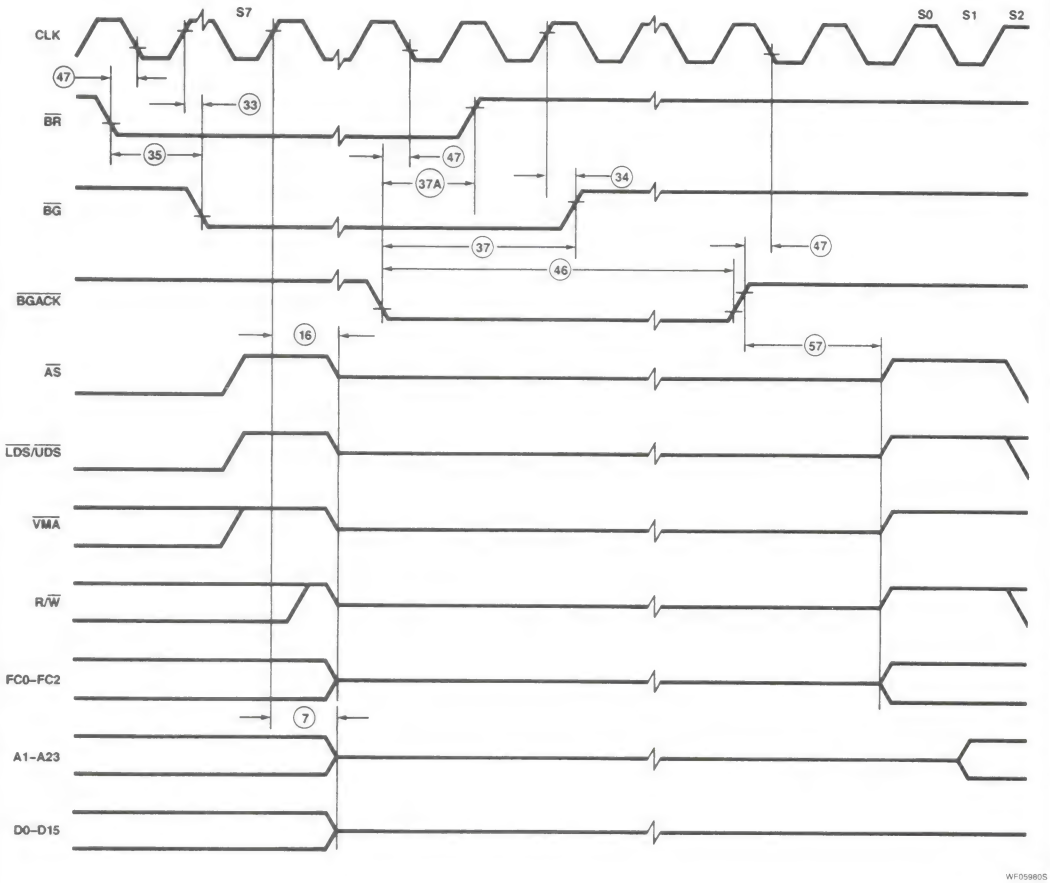



**Figure 50. Bus Arbitration Timing Diagram — Active Bus Case**

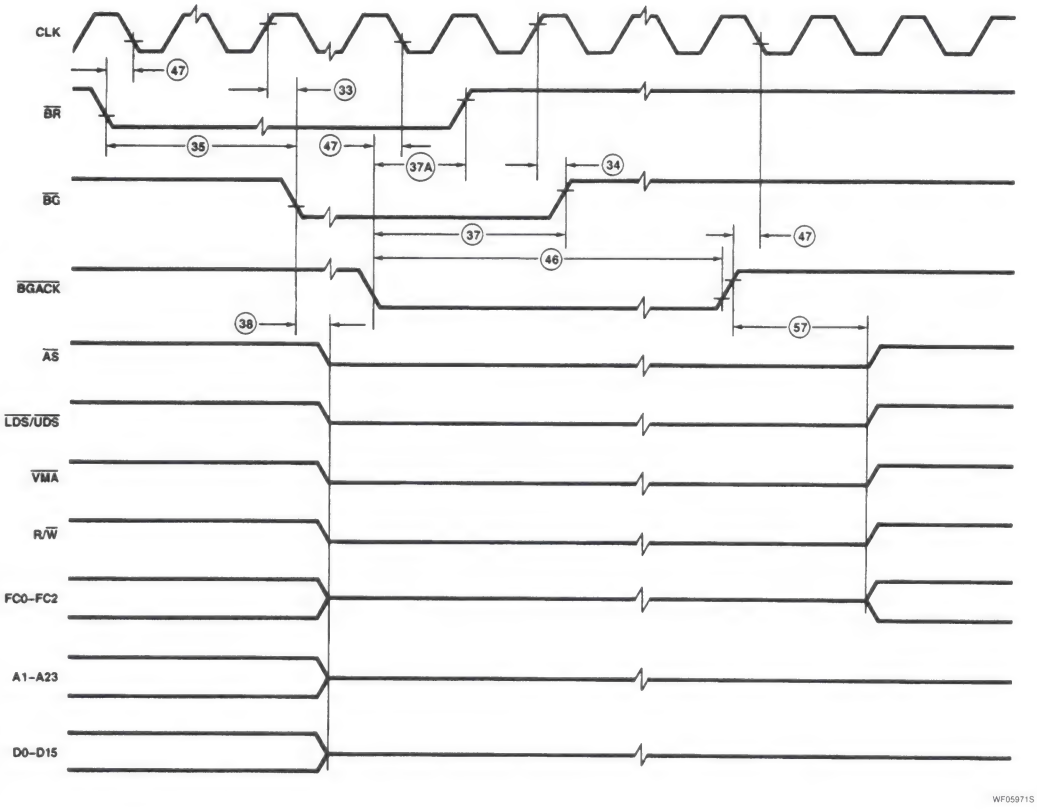



Figure 51. Bus Arbitration Timing Diagram — Idle Bus Case

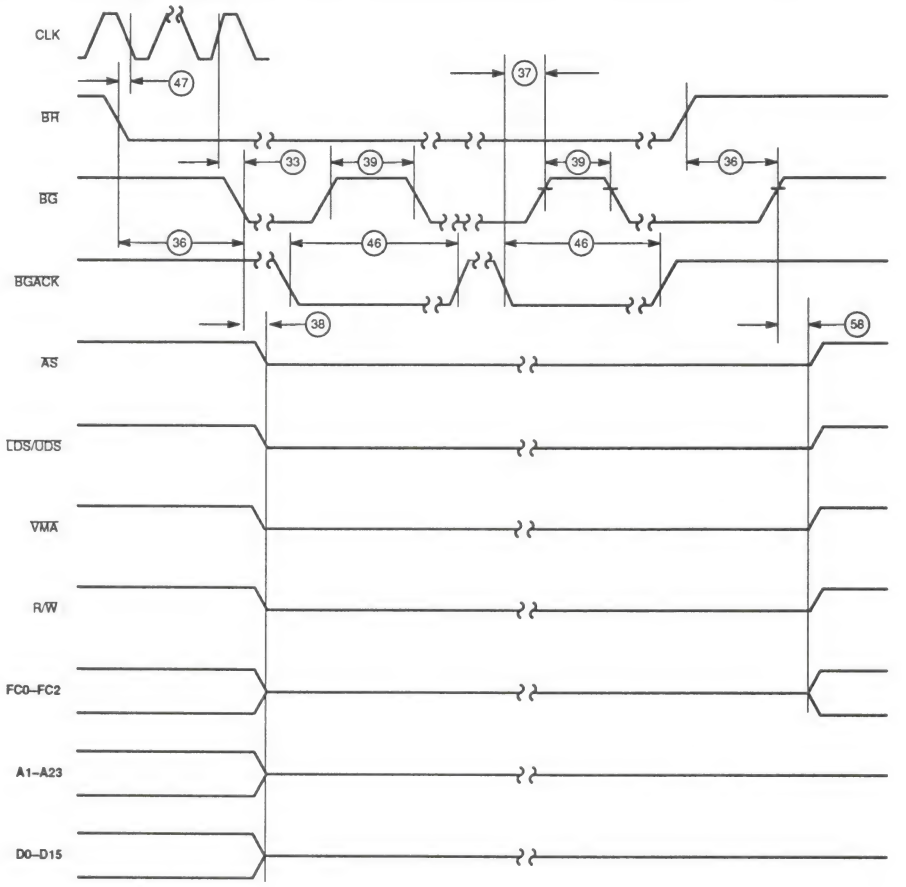



Figure 52. Bus Arbitration Timing Diagram — Multiple Bus Requests

Signetics

# 68154
## Interrupt Generator

*Product Specification*

**Military**
**Customer Specific Products**

### DESCRIPTION

The Signetics 68154 Interrupt Generator provides an interface between an interrupting device and a system bus such as the VMEbus or VERSAbus™. Figure 1 shows a typical configuration of the 68154. The 68154 has three primary functions:

1. Generates bus interrupt requests.
2. Resides in the interrupt acknowledge daisy chain.
3. Allows a status/ID byte (interrupt vector) to be supplied to the system if needed.

The 68154 has seven interrupt request levels, IRQ7N – IRQ1N, which are selected by using the interrupt request register. The local master writes to the interrupt request register to generate an interrupt request on any interrupt request level. The interrupt request register may be read to determine if an interrupt has been acknowledged. If a level with an interrupt request pending is acknowledged, the 68154 will allow a status/ID byte to be supplied to the system. Seven bits of the status/ID byte come from the interrupt vector register with the user externally supplying the LSB. If the 68154 does not have an interrupt acknowledge on the level acknowledged, the 68154 will pass the interrupt acknowledge on via the daisy-chain output. The user can enable or clear all interrupt request levels by setting specific bits in the interrupt vector register.

The 68154 was designed primarily for interface to the VMEbus. For more information regarding the protocol definitions, proper use, and application of this device, refer to the VMEbus Specification Manual.

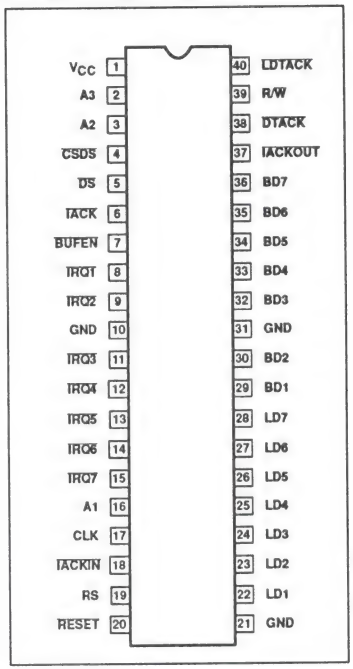
### FEATURES

- Interrupts generator for VMEbus and VERSAbus systems
- Generates 7 bus interrupt requests
- Two internal registers for system control
- Interrupt enable and interrupt clear bits
- Allows status/ID byte to be supplied during interrupt acknowledge
- High-speed bipolar technology
- Single +5V supply

### ORDERING INFORMATION

| PACKAGE | ORDERING CODE |
|---|---|
| 40–Pin Ceramic DIP | 68154/BQA |

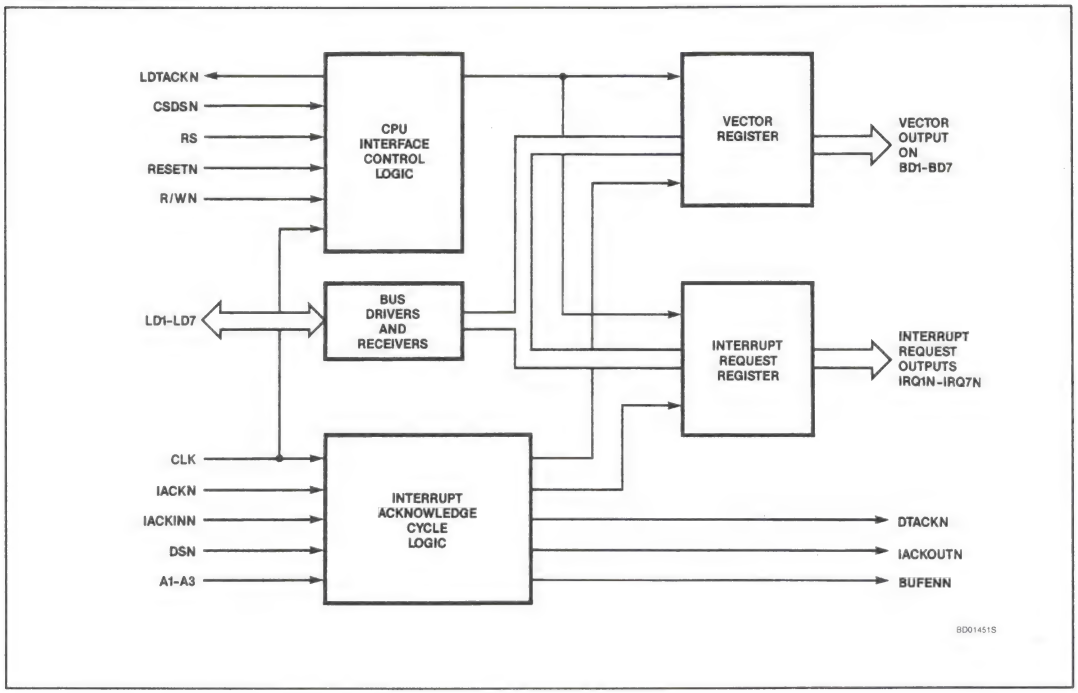
### PIN CONFIGURATION




VERSAbus is a registered trademark of Motorola, Inc.

# Interrupt Generator 68154

## BLOCK DIAGRAM



# Interrupt Generator 68154

## PIN DESCRIPTION

| SYMBOL | PIN NO. | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| $V_{CC}$ | 1 | I | **Supply Voltage:** +5V power supply. |
| A1 – A3 | 16, 3, 2 | I | **Address Lines:** Address inputs from system bus. The internal level being acknowledged is encoded on these inputs. A1 is LSB (least significant bit). |
| CSDSN | 4 | I | **Chip Select:** Active–Low chip select input for register I/O. This input must be qualified by the local master's data strobe prior to input (See Figure 1). |
| DSN | 5 | I | **Data Strobe:** Active–Low data strobe input from the system used to enable interrupt vector output. |
| IACKN | 6 | I | **Interrupt Acknowledge:** Active–Low interrupt acknowledge input from the system bus. |
| BUFENN | 7 | O | **Buffer Enable:** Active–Low totem pole output to enable the data buffer required to drive the outputs of the bus data pins (BD1 – BD7). |
| IRQ1N – IRQ7N | 8, 9, 11 – 15 | O | **Interrupt Request:** Active–Low totem pole system interrupt request output. |
| GND | 10, 21, 31 | I | **Ground** |
| CLK | 17 | I | **Clock:** Clock input (typically CPU clock). |
| IACKINN | 18 | I | **Interrupt Acknowledge In:** Active–Low interrupt acknowledge daisy–chain input. |
| RS | 19 | I | **Register Select:** Register select input. |
| RESETN | 20 | I | **Reset:** Active–Low input resets all internal registers, IACKOUTN, and RQnN. |
| LD1 – LD7 | 22 – 28 | I/O | **Local Data:** 3–State local data bus. |
| BD1 – BD7 | 29, 30, 32 – 36 | O | **Bus Data:** 3–State data pins used for vector output. |
| IACKOUTN | 37 | O | **Interrupt Acknowledge Out:** Acitve–Low totem pole interrupt acknowledge daisy–chain output. |
| DTACKN | 38 | O | **Data Transfer Acknowledge:** Acitive–Low totem pole output. This signal indicates that valid data is available on the bus during interrupt acknowledge cycle. |
| R/WN | 39 | I | **Read/Write:** Register read/write input. This signal specifies the data transfer cycle in process is to be either read or write. |
| LDTACKN | 40 | O | **Local Data Transfer Acknowledge:** Active–Low, open collector, data transfer acknowledge output to the local bus. |

## FUNCTIONAL DESCRIPTION

### Typical Configuration

The 68154 provides a vehicle for interprocessor communications on an intelligent peripheral controller board, or a CPU board as shown in Figure 1. The local data pins (LD1 – LD7) serve as a local data bus. This allows the local master to access the Interrupt Generator's two internal registers. During an interrupt acknowledge, the 68154 will allow for a status/ID byte to be supplied to the system. The 68154 supplies seven of the eight needed status/ID bits. The user is allowed to externally supply the least significant bit (LSB), typically the system address line A1 of the status/ID byte. The IRQ1N – IRQ7N, DTACKN, and BD1 – BD7 outputs require external buffers to provide adequate drive to the system bus. BUFENN provides the output enable control for the data buffer that is required for BD1 – BD7.

### Register Selection

The 68154 has two internal registers which can be programmed for system control. They are the interrupt vector register and the interrupt request register. Figure 2 shows the programming model. Both registers can be read from as well as written to. The interrupt vector register (register RO) is selected by the register select (RS) input equal to 0. Setting bit 1 of register RO enables all interrupt levels for the 68154. Writing a 1 to bit 2 of register RO resets all interrupt levels in the interrupt request register as well as the IRQnN outputs. Subsequent interrupt request will be honored. Bit 2 of RO will always be read as 0. The high order bits, bits 7 – 3, of register RO are the high order bits of the status/ID byte. The seven bit output of the status/ID byte are formed by concatenating the high order bits (bits 7 – 3) of register RO with system bus address lines A3 and A2. Bus address lines A3 and A2 are output on BD2 and BD1 respectively.

The interrupt request register (R1) is selected by RS input equal to 1. Setting bit "n" in R1 will generate an interrupt on interrupt request level IRQnN. Any number (up to the maximum of seven) interrupt requests can be generated in a single access of R1.

The state of only those levels, which a 1 has been written to, is affected. Writing a 0 to any level does not change the current state of that level. For example, if IRQ1N is currently asserted, writing a 0 bit to 1 of R1 does not de–assert IRQ1N, nor clear bit 1 in R1.

Note that interrupt requests on the same level are not stackable. To generate another interrupt request on a level currently asserted, the user must wait until that level has been acknowledged, before generating another interrupt request on that level.

Since interrupts are acknowledged independently of the local CPU, the interrupt vector register should not be modified while interrupts are pending. Any attempt to modify the interrupt vector register, while interrupts are pending, could cause the status/ID byte to change while the interrupted master is reading it. This could cause the interrupted master to acquire an in-

determinate vector. Therefore, the interrupt request should be examined to make certain there are no interrupts pending before attempting to modify the interrupt vector register.

All data transfers between the local CPU and the 68154 are done using local data lines (LD1 – LD7), register select (RS), read/write (R/WN) and a chip select input (CSDSN). The 68154 supplies a local data transfer acknowledge (LDTACKN) to complete the transfer of data between the local CPU and itself.

## Interrupt/Interrupt Acknowledge

The 68154 generates the maximum defined seven bus interrupts, on the IRQ1N – IRQ7N outputs, in a VMEbus or VERSAbus system. An interrupted master will acknowledge only a single level of the seven interrupt levels. To allow for multiple interrupters on the level acknowledged, VMEbus and VERSAbus systems use an interrupt acknowledge daisy–chain. The 68154 resides in this interrupt acknowledge daisy–chain.

When the system interrupt acknowledge (IACKN) is asserted, the interrupt acknowledge daisy–chain starts at the first slot in the system bus. The level being acknowledged is specified by the interrupted master on address lines A1 – A3. The system bus interface on the 68154 is initiated only if IACKN, interrupt acknowledge daisy chain in (IACK – INN), and data strobe 0 (DSON) are all received asserted. If the system bus interface is initiated and 68154 has an interrupt request on the level specified, it will not pass the daisy–chain signal on. It will, instead, clear the interrupt request level acknowledge, IRQnN, as well as the appropriate bit in the interrupt request register. It will also assert buffer enable (BUFENN), place seven bits of the status/ID byte on the bus data outputs (BD1 – BD7) and assert data transfer acknowledge (DTACKN).

If the system bus interface is initiated, but the 68154 has no interrupt request on the level being acknowledged, it will pass the daisy–chain input (IACKINN) on via the interrupt acknowledge out (IACKOUTN).

## Arbitration

The system bus interface, as well as the local master interface, are independent processes. Either can be initiated at any time without respect to the other. The 68154 will arbitrate between the processes, allowing proper system operation without any degradation in performance.

## Reset

When RESETN is asserted, 68154 drives the outputs IRQnN and IACKOUTN high. It also resets the interrupt request and the interrupt vector registers.

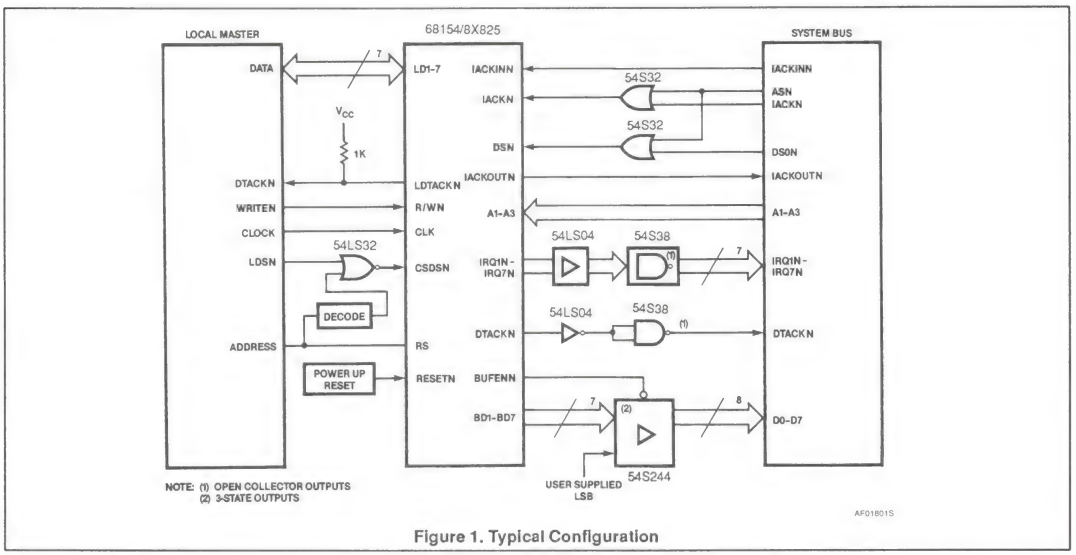



Figure 1. Typical Configuration

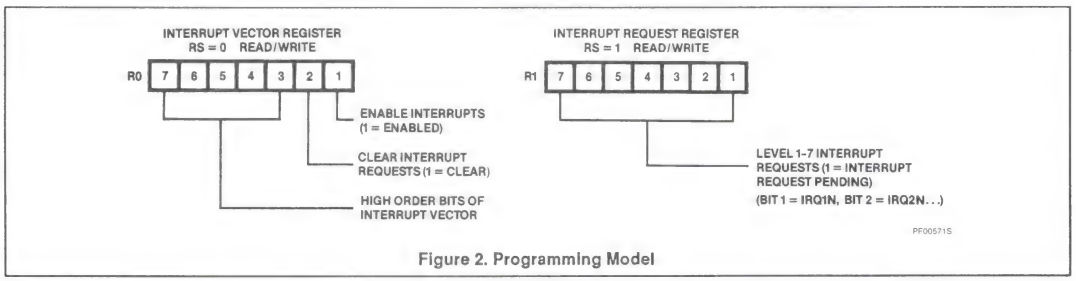

INTERRUPT VECTOR REGISTER
RS = 0 READ/WRITE
R0
7 6 5 4 3 2 1
ENABLE INTERRUPTS (1 = ENABLED)
CLEAR INTERRUPT REQUESTS (1 = CLEAR)
HIGH ORDER BITS OF INTERRUPT VECTOR
INTERRUPT REQUEST REGISTER
RS = 1 READ/WRITE
R1
7 6 5 4 3 2 1
LEVEL 1-7 INTERRUPT REQUESTS (1 = INTERRUPT REQUEST PENDING)
(BIT 1 = IRQ1N, BIT 2 = IRQ2N...)
PF00571S

Figure 2. Programming Model

# Interrupt Generator 68154

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_{CC}$ | Supply voltage range[3] | –0.5 to +7.0 | V |
| $V_I$ | Input voltage range[3] | –0.5 to +5.5 | V |
| $V_O$ | Voltage applied to output in OFF–State[3] | –0.5 to +5.5 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | RATINGS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage range | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High level input voltage | 2.0 | | | V |
| $V_{IL}$ | Low level input voltage | | | 0.8 | V |
| $I_{OL}$ | Low level output current | | | 8.0 | mA |
| $I_{OL}$ | ($\overline{LDTACK}$) Low level output current | | | 20 | mA |
| $I_{OH}$ | High level output current | | | –400 | µA |
| $T_A$ | Operating free air temperature range[2] | –55 to +125 | | | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C^2$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS[4] | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | V |
| $V_{IL}$ | Input Low voltage | | | 0.8 | V |
| $V_{IH}$ | Input High voltage | | 2.0 | | V |
| $I_{IL}$ | Input Low current | $V_{CC} = 5.5V$, $V_{IL} = 0.4V$ | | –400 | µA |
| $I_{IH}$ | Input High current | $V_{CC} = 5.5V$, $V_{IH} = 2.7V$ | | 100 | µA |
| $I_{OS}$ | Short circuit output current[16] | $V_{CC} = 5.5V$, $V_{OUT} = 0V$ | –15 | –100 | µA |
| $I_{OZL}$ | Hi–Z Low output current, BD1 – BD7 | $V_{CC} = 5.5V$, $V_{OZL} = 0.5V$ | | –20 | µA |
| $I_{OZH}$ | Hi–Z High output current, BD1 – BD7 | $V_{CC} = 5.5V$, $V_{OZH} = 2.5V$ | | 20 | µA |
| $V_{OL}$ | Output Low voltage range, LDTACKN | $V_{CC} = 4.5V$, $I_{OL} = 20mA$ | | 0.5 | V |
| | All other outputs | $V_{CC} = 4.5V$, $I_{OL} = 8mA$ | | 0.5 | V |
| $V_{OH}$ | Output High voltage range (except open collector) | $V_{CC} = 4.5V$, $I_{OH} = –400µA$ | 2.5 | | V |
| $I_{OH}$ | Open collector leakage current range, LDTACKN | $V_{CC} = 4.5V$, $V_{OUT} = 5.5V$ | | 100 | µA |
| $I_I$ | Input leakage current | $V_{CC} = 5.5V$, $V_I = 5.5V$ | | 200 | µA |
| $V_{IK}$ | Input clamp voltage | $V_{CC} = 4.5V$, $I_I = 10mA$ | | –1.2 | V |
| $I_{CC}$ | Supply voltage | $V_{CC} = 5.5V$, $V_I = 0V$ | | 210 | mA |

## AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | NUMBER | FIGURE | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $t_{RSS}$ | 1 | 3 & 4 | RS valid to CSDSN Low set up time | 0 | | ns |
| $t_{RWS}$ | 2 | 3 & 4 | R/WN to CSDSN Low set up time | 0 | | ns |
| $t_{DTV}$ | 3 | 3 | LDTACKN Low to LD1 – 7 valid | 6 | 30 | ns |
| $t_{DTCS}$ | 4 | 3 | LDTACKN Low to CSDSN High – Register read | 0 | | ns |
| | | 4 | LDTACKN Low to CSDSN High – Register write | 40 | | ns |
| $t_{RSH}$ | 5 | 3 & 4 | CSDSN High to RS valid hold time | 18 | | ns |
| $t_{RWH}$ | 6 | 3 | CSDSN High to R/WN High hold time | 9 | | ns |
| $t_{DTH}$ | 7 | 3 | CSDSN High to LD1 – 7 valid hold time[14] | 10 | | ns |
| $t_{TST}$ | 8 | 3 | CSDSN High to LD1 – 7 3–State[14,15] | | 34.5 | ns |
| $t_{CSDT}$ | 9 | 3 & 4 | CSDSN High to LDTACKN High[15] | 13 | 38 | ns |
| $t_{CSH}$ | 10 | 3 & 4 | CSDSN High time | 30 | | ns |
| $t_{ACCR}$ | 11 | 3 | CSDSN Low to LDTACKN Low read access time | 0.5CLK + 21 | 1.5CLK + 62 | ns |
| $t_{DS}$ | 12 | 4 | LD1 – LD7 valid to CSDSN Low set up time | 0 | | ns |
| $t_{RWH2}$ | 13 | 4 | CSDSN High to R/WN Low hold time | 9 | | ns |
| $t_{DH}$ | 14 | 4 | CSDSN High to LD1 – LD7 valid | 15 | | ns |
| $t_{IRQ}$ | 15 | 4 | LDTACKN Low to IRQnN Low | –10 | 30 | ns |
| $t_{ACCW}$ | 16 | 4 | CSDSN Low to LDTACKN Low write access time | 0.5CLK + 13 | 1.5CLK + 62 | ns |
| $t_{IKDS}$ | 17 | 5 | IACKN Low to DSN Low | 0 | | ns |
| $t_{ADDS}$ | 18 | 5 | A1 – A3 valid to DSN Low set up | 0 | | ns |
| $t_{ADIK}$ | 19 | 5 | A1 – A3 valid to IACKINN Low set up | 0 | | ns |
| $t_{IKBF}$ | 20 | 5 | IACKINN Low to BUFENN Low[15] | CLK + 13 | 1.5CLK + 50 | ns |
| $t_{DSBF}$ | 21 | 5 | DSN Low to BUFENN Low[15] | CLK + 29 | 1.5CLK + 79 | ns |
| $t_{IRA1}$ | 22 | 5 | IACKINN Low to IRQnN High[15] | CLK + 34 | 1.5CLK + 92 | ns |
| $t_{IRA2}$ | 23 | 5 | DSN Low to IRQnN High[15] | CLK + 50 | 1.5CLK + 120 | ns |
| $t_{DYO1}$ | 24 | 5 | IACKINN Low to IACKOUTN[15] | CLK + 7 | 1.5CLK + 79 | ns |
| $t_{DYO2}$ | 25 | 5 | DSN Low to IACKOUTN Low[15] | CLK + 25 | 1.5CLK + 79 | ns |
| $t_{BFBD}$ | 26 | 5 | BUFENN Low to BS1 – BD7 valid | 0 | | ns |
| $t_{BFDT}$ | 27 | 5 | BUFENN Low to DTACKN Low | 0.5CLK – 30 | 0.5CLK + 6 | ns |
| $t_{IAD}$ | 28 | 5 | IACKN High to A1 – A3 valid hold time | 49 | | ns |
| $t_{DSAD}$ | 29 | 5 | DSN High to A1 – A3 valid hold time | 49 | | ns |
| $t_{DTDS}$ | 30 | 5 | DTACKN Low to DSN High | 0 | | ns |
| $t_{DTIK}$ | 31 | 5 | DTACKN Low to IACKN High | 0 | | ns |
| $t_{IDT}$ | 32 | 5 | IACKN High to BD1 – BD7 valid hold time[15] | 13 | 49 | ns |
| $t_{DSDT}$ | 33 | 5 | DSN High to BD1 – BD7 valid hold time[15] | 13 | 49 | ns |
| $t_{ITST}$ | 34 | 5 | IACKN High to BD1 – BD7 3–State[15] | | 49 | ns |
| $t_{DTST}$ | 35 | 5 | DSN High to BD17 – BD7 3–State[15] | | 49 | ns |
| $t_{DBF}$ | 36 | 5 | DSN High to BUFENN High[15] | 17 | 55 | ns |
| $t_{IBF}$ | 37 | 5 | IACKN High to BUFENN High[15] | 17 | 55 | ns |
| $t_{DDTK}$ | 38 | 5 | DSN High to DTACKN High[15] | 14 | 44 | ns |
| $t_{IDTK}$ | 39 | 5 | IACKN High to DTACKN High[15] | 14 | 44 | ns |
| $t_{IOUT}$ | 40 | 5 | IACKN High to IACKNOUTN High[15] | 19 | 57 | ns |
| $t_{DOUT}$ | 41 | 5 | DSN High to IACKOUTN High[15] | 12 | 57 | ns |
| $t_{IAKH}$ | 42 | 5 | IACKN High time | 58 | | ns |
| $t_{IINH}$ | 43 | 5 | IACKN High to IACKINN High | 18 | | ns |

## AC ELECTRICAL CHARACTERISTICS (Continued) $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | NUMBER | FIGURE | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $t_{IKIN}$ | 44 | 5 | IACKN Low to IACKINN Low | 0 | | ns |
| $t_{RST}$ | 45 | 6 | RESETn Low time | 28 | | ns |
| $t_{CKH}$ | 46 | 7 | Clock High | 36 | | ns |
| $t_{CKL}$ | 47 | 7 | Clock Low | 48 | | ns |
| $t_{CKPD}$ | 48 | 7 | Clock period | 100 | | ns |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 45°C/W junction to ambient for ceramic package.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. If the falling edge of IACKINN occurs last, then (19) is valid. If the falling edge of DSN occurs last, then (18) is valid. If the falling edges of IACKINN and DSN occur simultaneously, then either (19) or (18) is valid.
6. If the falling edge of IACKINN occurs last, then (17) is valid. If the falling edge of DSN occurs last, then (21) is valid. If the falling edges of IACKINN and DSN occur simultaneously, then either (17) or (21) is valid.
7. True only if no request pending on levels being acknowledged. If the falling edge of IACKINN and DSN occur simultaneously, then either (22) or (23) is valid.
8. If the rising edge of IACKNN occurs first, then (24) is valid. If the rising edge of DSN occurs first, then (25) is valid. If the rising edges of both IACKNN and DSN occur simultaneously, then either (24) or (25) is valid.
9. If the rising edge of IACKN occurs first, then (33) is valid. If the rising edge of DSN occurs first, then (34) is valid. If the rising edge of both IACKN and DSN occur simultaneously, then either (33) or (34) is valid.
10. If the rising edge of IACKN occurs first, then (35) is valid. If the rising edge of DSN occurs first, then (36) is valid. If the rising edges of both IACKN and DSN occurs simultaneously, then either (35) or (36) is valid.
11. If the rising edge of IACKN occurs first, then (38) is valid. If the rising edge of DSN occurs first, then (37) is valid. If the rising edges of both IACKN and DSN occur simultaneously, then either (38) or (37) is valid.
12. If the rising edge of IACKN occurs first, then (40) is valid. If the rising edge of DSN occurs first, then (39) is valid. If the rising edges of both IACKN and DSN occur simultaneously, then either (40) or (39) is valid.
13. True only if no request pending on level being acknowledged. If the rising edges of both IACKN and DSN occur simultaneously, then either (41) or (42) is valid.
14. (8) is always greater than (7).
15. Guaranteed, but not tested.
16. Not more than one output should be shorted at one time and the duration of the short circuit should not exceed one second.

## REGISTER READ

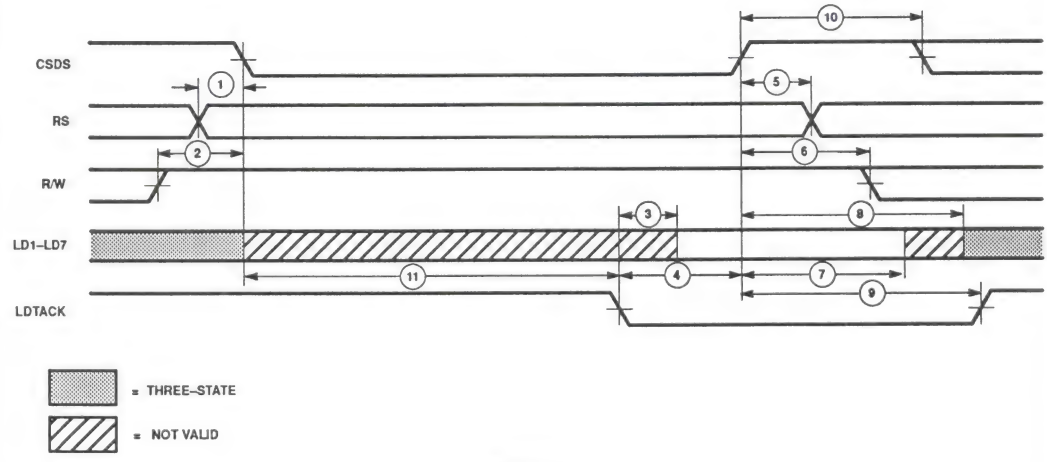



Figure 3

## REGISTER WRITE

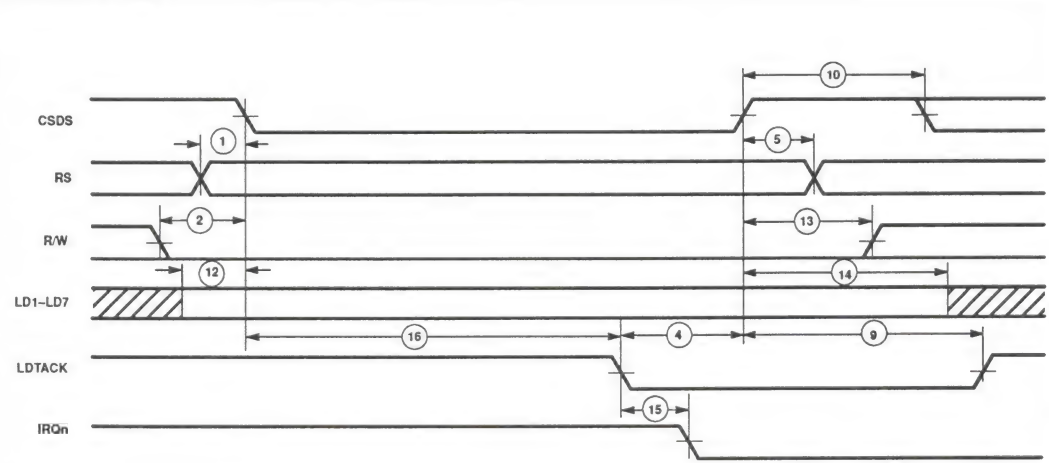



Figure 4

## INTERRUPT ACKNOWLEDGE

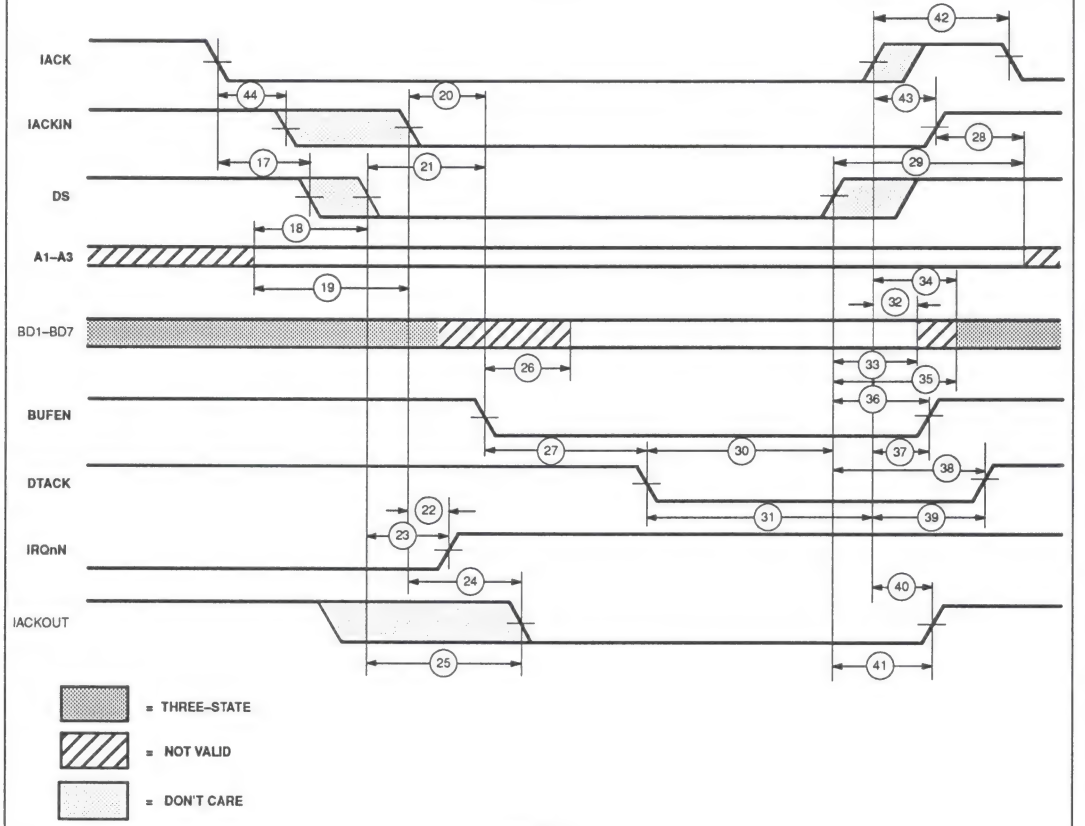



Figure 5

## RESET TIMING

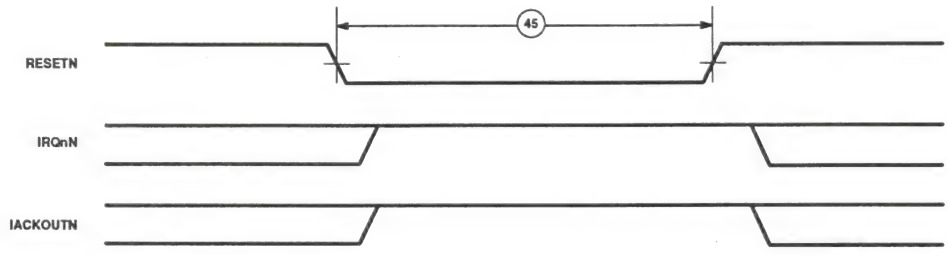



Figure 6. Reset Timing

## RESET TIMING

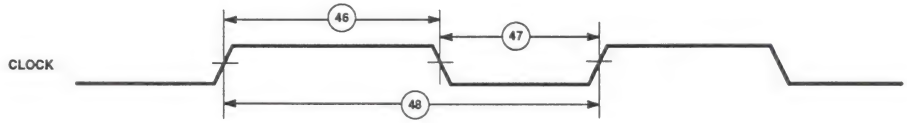



Figure 7. Clock Timing

Signetics

# 68155
## Interrupt Handler

*Product Specification*

**Military Microprocessor Products**

## DESCRIPTION

The Signetics 68155 is an asynchronous interrupt handler for VMEbus and VERSAbus® systems. Up to 14 interrupts are prioritized by the 68155 to one of seven levels and are output on the interrupt priority level lines (IPLON-IPL2N). The 68155 prioritizes the interrupts in the following manner: local bus requests over system bus requests with the non-maskable interrupt (NMIN) considered the highest priority local interrupt (NMIN over IRQ7N, then LRQ6N-LRQ1N over IRQ6N-IRQ1N).

The local interrupt requests can be programmed to be either active high or low, and either edge of level sensitive. The system bus interrupt requests are always active low and level sensitive. The non-maskable interrupt is always negative edge-triggered.

During a local interrupt acknowledge sequence, two modes of response are available: vectored mode or device-supplies-the vector mode.

For system bus responses, the 68155 works with a bus requester (for example, the 68172 VMEbus Controller), to acquire a status/ID byte (interrupt vector) for the system.

The 68155 was designed primarily for interface to the VMEbus. For more information regarding the protocol definitions, proper use, and application of this device, refer to the VMEbus Specification Manual.

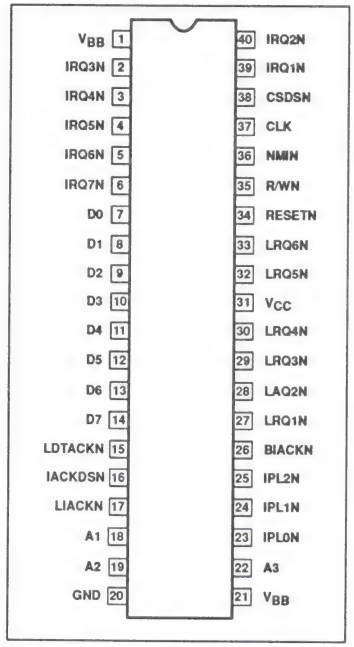
## FEATURES

- **Asynchronous interrupt handler for VMEbus and VERSAbus® systems**
- **Receives and prioritizes non-maskable, six local and seven system bus interrupts**
- **Interrupts may be polled in lieu of real-time operation**
- **Programmable local interrupt response**
- **Complete device status, including last interrupt acknowledged**
- **High-speed bipolar technology**

## ORDERING INFORMATION

| PACKAGE | ORDERING CODE |
|---|---|
| 40–Pin Ceramic DIP | 68155/BQA |

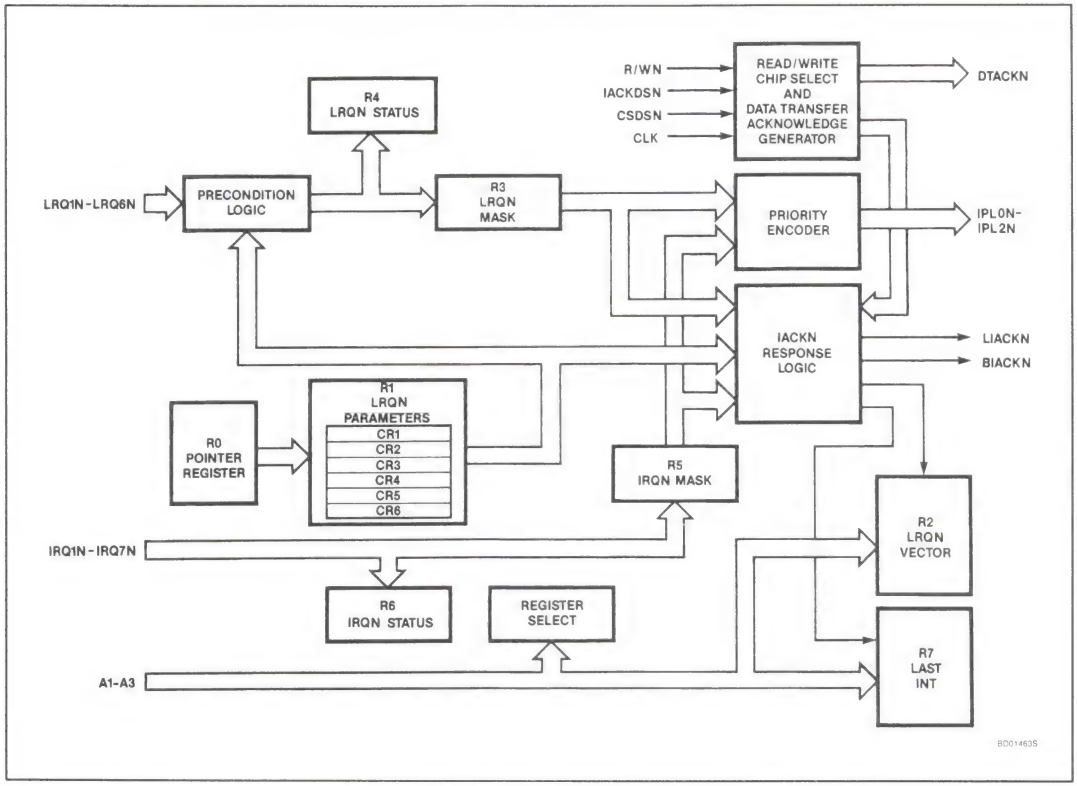
## PIN CONFIGURATION




VERSAbus is a registered trademark of Motorola, Inc.

# Interrupt Handler | 68155

## BLOCK DIAGRAM



# Interrupt Handler | 68155

## PIN DESCRIPTION

| MNEMONIC | PIN NO. | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| $V_{BB}$ | 1, 21 | I | **Supply Voltage:** Supply voltage for internal gates. |
| IRQ1N – IRQ7N | 39, 40, 2 – 6 | I | **Bus Interrupt Request:** Active–Low inputs for bus–generated interrupts. |
| D0 – D7 | 7 –14 | I/O | **Bus Data:** 3–State local data bus. |
| LDTACKN | 15 | O | **Local Data Transfer Acknowledge:** Acitive–Low, open–collector output. Indicates that valid data is available on the local data bus during interrupt acknowledge cycle or data transfer cycle. |
| IACKDSN | 16 | I | **Interrupt Acknowledge:** Active–Low interrupt acknowledge input from the local master. This signal must be qualified by the local master's data strobe prior to input. |
| LIACKN | 17 | O | **Local Interrupt Acknowledge:** Active–Low interrupt acknowledge totem–pole output to the local interrupting devices. |
| A1 – A3 | 18, 19, 22 | I | **Address Lines:** Address inputs from local master. |
| GND | 20 | I | **Ground** |
| IPL0N – IPL2N | 23 – 25 | O | **Interrupt Priority Level:** Active–Low totem–pole outputs to the local master. The priority level of the interrupt request is encoded on these outputs. |
| BIACKN | 26 | O | **Bus Interrupt Acknowledge:** Acitve–Low interrupt acknowledge totem–pole output to the system bus. |
| LRQ1N – LRQ6N | 27 – 30, 32, 33 | I | **Local Interrupt Request:** User can define the active state of these inputs. |
| $V_{CC}$ | 31 | I | **Supply Voltage:** +5V power supply. |
| RESETN | 34 | I | **Reset:** Active–Low input reset. |
| R/WN | 35 | I | **Read/Write:** This signal specifies the data transfer cycle to be either read or write. |
| NMIN | 36 | I | **Non–Maskable Interrupt:** Active–Low highest priority interrupt. |
| CLK | 37 | I | **Clock:** Clock input (typically CPU clock). |
| CSDSN | 38 | I | **Chip Select:** Active–Low chip select input for register I/O. This input must be qualified by the local master's data strobe prior to input. |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_{CC}$ | Supply voltage range[3] | –0.5 to +7.0 | V |
| $V_I$ | Input voltage range[3] | –0.5 to +5.5 | V |
| $V_O$ | Voltage applied to output in OFF–State[3] | –0.5 to +5.5 | V |

# Interrupt Handler 68155

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | RATINGS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{BB}$ | Supply voltage range | 1.35 | 1.5 | 1.65 | V |
| $V_{CC}$ | Supply voltage range | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High level input voltage range | 2.0 | | | V |
| $V_{IL}$ | Low level input voltage range | | | 0.8 | V |
| $I_{OL}$ | Low level output current range | | | 8.0 | mA |
| $I_{OH}$ | High level output current range | | | –3.0 | µA |
| $T_A$ | Operating free–air temperature range[2] | –55 to +125 | | | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C^2$, $4.5V \leq V_{CC} \leq 5.5V^5$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS[4] | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{CC}$ | Supply voltage range | | 4.5 | 5.5 | V |
| $V_{BB}$ | Supply voltage range | | 1.35 | 1.65 | V |
| $I_{CC}$ | $V_{CC}$ supply current range | $V_{CC}$ = 5.5V | | 100 | mA |
| $I_{BB}$ | $V_{BB}$ supply current range | $V_{BB}$ = 1.65V | | 200 | mA |
| $I_{IL}$ | Input Low current range | $V_{CC}$ = 5.5V, $V_{BB}$ = 1.65V, $V_{IL}$ = 0.4V | | –20 | µA |
| $I_{IH}$ | Input High current range | $V_{CC}$ = 5.5V, $V_{BB}$ = 1.65V, $V_{IH}$ = 2.7V | | 20 | µA |
| $I_{OS}$ | Short circuit output current except LDTACKN | $V_{CC}$ = 5.5V, $V_{OUT}$ = 0V[6] | –15 | –100 | mA |
| $V_{OL}$ | Output Low voltage range | $V_{CC}$ = 4.5V, $V_{BB}$ = 1.35V, $I_{OL}$ = 8mA | | 0.6 | V |
| $V_{OH}$ | Output High voltage except LDTACKN (open collector) | $V_{CC}$ = 4.5V, $V_{BB}$ = 1.35V, $I_{OH}$ = –3mA | 2.5 | | V |
| $I_I$ | Input leakage current | $V_{CC}$ = 5.5V, $V_I$ = 5.5V | | 100 | µA |
| $I_{CEX}$ | Open–Collector leakage current LDTACKN | $V_{CC}$ = 4.5V, $V_O$ = 4.5V | | 100 | µA |
| $V_{IC}$ | Input clamp voltage | $V_{CC}$ = 4.5V, $I_{IK}$ = –10mA | –1.5 | | V |
| $V_{IL}$ | Input Low voltage | | | 0.8 | V |
| $V_{IH}$ | Input High voltage | | 2.0 | | V |

## AC ELECTRICAL CHARICTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | FIGURE | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{RWS}$ | 3 & 4 | R/WN TO CSDSN Low set up time | 5 | | ns |
| $t_{IAKS}$ | 3 & 4 | IACKDSN High to CSDSN Low set up time | 42 | | ns |
| $t_{ADRS}$ | 3 & 4 | A1 – A3 valid to CSDSN Low set up time | 29 | | ns |
| $t_{DTV}$ | 3 | CSDSN Low to D0 – D7 set up time | | 164 | ns |
| $t_{ACCR}$ | 3 | CSDSN Low to LDTACKN Low read access time | CLK + 33 | 2CLK + 175 | ns |
| $t_{RWH}$ | 3 & 4 | CSDSN High to R/WN High hold time | 16 | | ns |
| $t_{ADRH}$ | 3 & 4 | CSDSN High to A1 – A3 valid hold time | 6 | | ns |
| $t_{DTH}$ | 3 & 4 | CSDSN High to D0 – D7 valid hold time | 34 | 104 | ns |
| $t_{TST}$ | 3 | CSDSN High to D0 – D7 3–State | 34 | 104 | ns |
| $t_{ACK}$ | 3 & 4 | CSDSN High to LDTACKN High time | 15 | 56 | ns |
| $t_{CSH}$ | 3 & 4 | CSDSN High time | 42 | | ns |
| $t_{DTCS}$ | 3 & 4 | LDTACKN Low to CSDSN High | 18 | | ns |
| $t_{DS}$ | 4 | D0 – D7 valid to CSDSN Low set up time | 0 | | ns |
| $t_{ACCW}$ | 4 | CSDSN Low to LDTACKN Low write access time | CLK + 33 | 2CLK + 175 | ns |
| $t_{CSS}$ | 5, 6 & 7 | CSDSN High to IACKDSN Low set up time | 42 | | ns |
| $t_{PDL}$ | 5 & 6 | IACKDSN Low to LIACKN Low propagation time | CLK + 33 | 2CLK + 175 | ns |
| $t_{DAV}$ | 5 | IACKDSN Low to D0 – D7 vector valid | | 189 | ns |
| $t_{ACCV}$ | 5 | IACKDSN Low to LDTACKN Low (vector access time) | CLK + 33 | 2CLK + 175 | ns |
| $t_{IKH}$ | 5, 6 & 7 | IACKDSN High time | 42 | | ns |
| $t_{DAH}$ | 5 | IACKDSN High to D0 – D7 valid hold time | 34 | 104 | ns |
| $t_{TRST}$ | 5 | IACKDSN High to D0 – D7 3–State | 34 | 104 | ns |
| $t_{IKDT}$ | 5 | IACKDSN High to LDTACKN High | 15 | 56 | ns |
| $t_{PDH}$ | 5 & 6 | IACKDSN High to LIACKN High propagation delay | 15 | 56 | ns |
| $t_{DTIK}$ | 5 | LDTACKN Low to IACKDSN High time | 18 | | ns |
| $t_{ADRS}$ | 5, 6 & 7 | A1 – A3 valid to IACKDSN Low set up time | 29 | | ns |
| $t_{ADH}$ | 5, 6 & 7 | IACKDSN High to A1 – A3 valid hold time | 6 | | ns |
| $t_{PDL2}$ | 7 | IACKDSN Low to BIACK Low propagation delay | CLK + 33 | 2CLK + 175 | ns |
| $t_{PDH2}$ | 7 | IACKDSN High to BIACK High propagation delay | 15 | 56 | ns |
| $t_{RST}$ | 8 | RESET Low time | 31 | | ns |
| $t_{CKPD}$ | 9 | Clock period | 100 | | ns |
| $t_{CKH}$ | 9 | Clock High | 45 | | ns |
| $t_{CKL}$ | 9 | Clock Low | 35 | | ns |
| $t_S$ | 9 | CSDSN Low to clock High set up time | 45 | | ns |

**NOTES:**

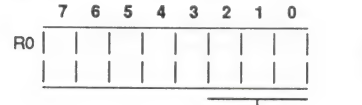
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient for ceramic package.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of ≤3ns maximum and output voltages are checked at 1.5V.
6. At any time, no more than one output should be connected to ground.
7. $t_{TST}$ is always greater than or equal to $t_{DTH}$.
8. Signal number $t_{TRST}$ is always greater than or equal to signal number $t_{DAH}$.

## REGISTERS

The 68155 contains eight internal registers (R0 – R7) accessible to the local master. There are also six sub–registers contained in register R1. Register R0 specifies which sub–register is to be accessed in R1. Register R2 stores the interrupt vector for vectored mode responses. Register R3 and R5 are the interrupt mask registers for the local and system bus interrupts, respectively. Registers R4 and R6 are the status registers for local and bus interrupts, respectively, allowing all interrupts to be polled. Register R7 can be read by the local master to determine the last interrupt acknowledged.

All data transfers between the 68155 and the local master are done using the local data bus (D0 – D7), address bus (A1 – A3), a chip select (CSDSN) and a read/write (R/WN) input.

**Register R0 — A3A2A1 = 000**

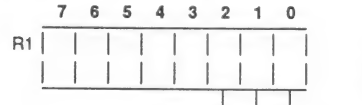



Pointer register (write only).
Bit 0 – 2 of R0 specify which control sub–register CR1 – CR6 during an access of R1.
During register I/O, bits 7 – 3 will read as 0.

B2 – B1 – B0

| | |
|---|---|
| 000 – none | 100 – CR4 |
| 001 – CR1 | 101 – CR5 |
| 010 – CR2 | 110 – CR6 |
| 011 – CR3 | 111 none |

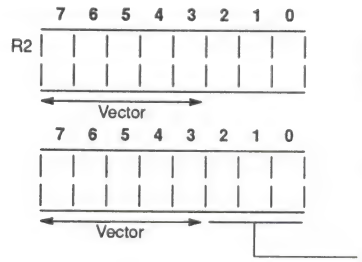
**Register R1 — A3A2A1 = 001**




Control registers CR1 – CR6 (read or write).
These six registers program the function of the local interrupt requests (LRQ1N – LRQ6N).
(CR1 programs LRQ1N, CR2 programs LRQ2N, etc.).
During register I/O, bits 7 – 3 will be read as 0.

| | |
|---|---|
| LRQnN active state (High/Low) | (1 = active High) |
| LRQnN edge/level sensitive | (1 = edge sensitive) |
| LRQnN vector enable | (1 = enabled) |

**Register R2 — A3A2A1 = 010**

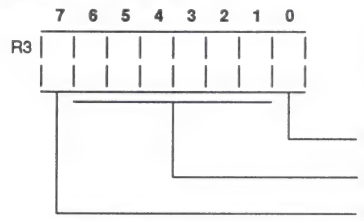



LRQ vector (read or write).
Bits 7 – 3 of this register are the top five bits of the local interrupt vector.
During register I/O, bits 2 – 0 will be read as zeros.

LRQ vector output during local interrupt acknowledge (if vector enable = 1).

| | |
|---|---|
| 001 – LRQ1N | 100 – LRQ4N |
| 010 – LRQ2N | 101 – LRQ5N |
| 011 – LRQ3N | 110 – LRQ6N |
| | 111 – NMIN |

**Register R3 — A3A2A1 = 011**




LRQ mask (read or write).
This register allows the user to mask local interrupts. It also enables vectored response for NMIN.

NMIN Vector enable (1 = enabled)

LRQN 1 – 6 mask (1 = interrupt enabled)

NMIN mask (1 = NMIN enabled)

Bit 1 = LRQ1N
Bit 2 = LRQ2N
Bit 3 = LRQ3N
Bit 4 = LRQ4N
Bit 5 = LRQ5N
Bit 6 = LRQ6N
Bit 7 = NMIN

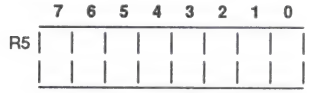
**Register R4 — A3A2A1 = 100**

LRQ status (read only).
Local interrupts can be polled through this register.
During register I/O, bit 0 will be read as a 0.

Bit 1 = LRQ1N
Bit 2 = LRQ2N
Bit 3 = LRQ3N
Bit 4 = LRQ4N
Bit 5 = LRQ5N
Bit 6 = LRQ6N
Bit 7 = NMIN

LRQN status (1 = interrupt pending)
NMIN stauts (1 = interrupt pending)

**Register R5 — A3A2A1 = 101**




IRQ mask (read or write).
This register allows the user to mask system bus interrupts.
During register I/O, bit 0 will be read as a 0.

Bit 1 = IRQ1N
Bit 2 = IRQ2N
Bit 3 = IRQ3N
Bit 4 = IRQ4N
Bit 5 = IRQ5N
Bit 6 = IRQ6N
Bit 7 = IRQ7N

(1 = interrupt enabled)

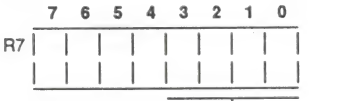
**Register R6 — A3A2A1 = 110**

IRQ status (read only).
System bus interrupts can be polled through this register.
During register I/O, bit 0 will be read as 0.

Bit 1 = IRQ1N
Bit 2 = IRQ2N
Bit 3 = IRQ3N
Bit 4 = IRQ4N
Bit 5 = IRQ5N
Bit 6 = IRQ6N
Bit 7 = IRQ7N

IRQN status (1 = interrupt pending)

**Register R7 — A3A2A1 = 111**




Last interrupt acknowledged (read only).
This register can be read by the local CPU to determine the last interrupt acknowledged.
During register I/O, bits 7 – 4 will be read as 0.

| | |
|---|---|
| 0000 – none | 1000 – none |
| 0001 – IRQ1N | 1001 – LRQ1N |
| 0010 – IRQ2N | 1010 – LRQ2N |
| 0011 – IRQ3N | 1011 – LRQ3N |
| 0100 – IRQ4N | 1100 – LRQ4N |
| 0101 – IRQ5N | 1101 – LRQ5N |
| 0110 – IRQ6N | 1110 – LRQ6N |
| 0111 – IRQ7N | 1111 – NMIN |

## FUNCTIONAL OPERATION

### Typical Configuration

The 68155 can handle interrupts from 14 sources: seven bus interrupt requests generated on the IRQ1N – IRQ7N inputs, six local interrupt sources generated on the LRQ1N – LRQ6N inputs, and one non–maskable interrupt which may originate locally or from the system (such as the system's AC fail signal). All interrupts are encoded to one of seven levels and output on the IPL0N – IPL2N lines. Table 1 shows how the 68155 encodes the interrupts.

BIACKN is the bus interrupt acknowledge signal which is asserted during a bus interrupt acknowledge sequence. BIACKN can be used to get the associated bus requester (for example, the Signetics 68172), to acquire an interrupt vector from the system bus. Figure 1 shows a typical 68155 – 68172 system configuration.

LIACKN is the local interrupt acknowledge signal which is asserted during a local interrupt acknowledge sequence. Figure 2 shows a typical configuration for the 68155.

### Non–Maskable Interrupt (NMI)

The highest priority interrupt request is the non–maskable interrupt (NMIN). It is an Active–Low, negative edge–triggered interrupt. NMIN is considered by the 68155 to be the highest priority local interrupt, however, the user is not restricted to having it represent a local device. When the local master responds to an NMIN, bit 7 in the LRQ status register R4 is cleared to 0.

Both vectored and device–supplies–the–vector modes are available with NMIN. However, it is recommended that the 68155 response to an NMIN be a vectored mode interrupt acknowledge.

### Local Interrupts

The 68155 can handle interrupts generated by local devices through its six local interrupt request lines (LRQ1N – LRQ6N). The local interrupt requests are prioritized with LRQ6N being the highest priority, and LRQ1N the lowest priority.

The response of the 68155 to an acknowledge of a local interrupt can be selected by means of the 68155 R1 register. Pointer register R0 points to one of the six control sub–registers when accessing register R1. The six control registers (CR1 – CR6) in register R1 define the functions of the six local interrupt requests (LRQ1N – LRQ6N).

**Control Register 'n' Bit 0**
Selects local interrupt requests 'n' (LRQnN), to be either Low or High. Bit 0 = 1 defines active state to be High.

**Control Register 'n' Bit 1**
Selects local interrupt request 'n', to be either edge or level sensitive. Bit 1 = 1 defines LRQnN to be edge sensitive.

**Control Register 'n' Bit 2**
Selects either vectored mode or device–supplies–the–vector mode response. Bit 2 = 1 enables vectored mode operation for LRQnN.

Two modes of operation for a local interrupt response are possible; vectored mode and device–supplies–the–vector mode. In vectored mode, the 68155 supplies the interrupt vector to the local CPU and asserts LDTACKN to complete the transfer. In the device–supplies–the–vector mode, the local interrupting device supplies its own interrupt vector and asserts LDTACKN to complete the transfer.

The vector register R2 allows the user to program the five most significant bits (bits 7 – 3) of the interrupt vector supplied in vectored mode. During a vectored local interrupt acknowledge cycle, the upper five bits of the vector register are concatenated with a 3–bit interrupt level (address lines A3 = B2 of the vector, A2 = B1 and A1 = B0). This forms the unique vector for the local interrupt request level being acknowledged.

The local interrupt request mask register R3 allows the user to selectively enable local interrupt requests by setting appropriate bits in the register.

The current state of the local interrupt requests can be determined by the local master by reading the local interrupt status register R4.

### Local Interrupt Acknowledge

An interrupt acknowledge, by the local CPU, is signified by the assertion of the interrupt acknowledge input (IACKDSN). The 68155 responds by reading the three address lines (A1 – A3) to determine what level is being acknowledged. If a local interrupt is the highest priority interrupt pending on the level acknowledged, the 68155 will respond as though it is programmed for that level.

If vectored mode is programmed, the 68155 will assert the local interrupt acknowledge (LIACKN) and place the interrupt vector on the local data bus. To complete the transfer of the vector to the local CPU, the 68155 asserts the local data transfer acknowledge signal (LDTACKN).

If device–supplies–the–vector mode is programmed, the 68155 asserts the local interrupt acknowledge signal (LIACKN). The interrupting device is then allowed to place its own vector on the local data bus and assert LDTACKN.

When a local interrupt is acknowledged by the local master, the appropriate bit in the LRQ status register R4 is cleared to 0.

### Bus Interrupts

The VMEbus specification defines a maximum of seven interrupt levels. The 68155 can handle seven system bus interrupts through its IRQ1N – IRQ7N lines. Bus interrupt requests are Active–Low level sensitive, and prioritized with IRQ7N being the highest priority and IRQ1N the lowest priority. The bus mask control register R5 allows the user to selectively enable bus interrupt requests by setting appropriate bits in

the register. The local CPU can read the bus interrupt status register R6 to determine the current state of the bus interrupt requests.

## Bus Interrupt Acknowledge

The local CPU asserts the interrupt acknowledge signal (IACKDSN) to signify an interrupt acknowledge. The 68155 responds by reading the interrupt level on A1 – A3 to determine what level is being acknowledged. If a local interrupt is not pending on the level acknowledged, and that bus level is not masked, the 68155 will assert bus interrupt acknowledge (BIACKN). If that bus level is masked, the 68155 will not respond to the interrupt acknowledge by the local master.

Part of the interrupt acknowledge sequence for a bus interrupt consists of acquiring a vector (status/ID byte) from the system bus.

The bus signals required to acquire this vector are available with a bus controller. The Signetics 68172 bus controller can be used by the 68155 to acquire the vector (status/ID byte), thereby eliminating the need for the 68155 to duplicate this bus control functions. Because most interrupts are serviced by boards that already have the 68172, a one–chip addition of the 68155 gives that board complete interrupt handling capability.

Since the 68155 is an asynchronous device, it is possible for a local interrupt request to be asserted during acknowledgement of a bus interrupt on the same level. The 68155 passes all local interrupt requests through transparent latches which close during each interrupt acknowledge cycle. All possibility of contention is therefore eliminated.

## Reset

When RESETN is asserted, the 68155 drives LDTACKN, LIACKN, BIACKN and IPL0N – IPL2N all High. The D0 – D7 I/O pins go to 3–State and all internal registers are cleared.

**Table 1. 68155 Interrupt Level Encoding**

| INTERRUPT REQUEST LEVEL | INTERRUPT PRIORITY LEVEL OUTPUTS | | |
|---|---|---|---|
| | IPL2N | IPL1N | IPL0N |
| NMIN, IRQ7N | 0 | 0 | 0 |
| LRQ6N, IRQ6N | 0 | 0 | 1 |
| LRQ5N, IRQ5N | 0 | 1 | 0 |
| LRQ4N, IRQ4N | 0 | 1 | 1 |
| LRQ3N, IRQ3N | 1 | 0 | 0 |
| LRQ2N, IRQ2N | 1 | 0 | 1 |
| LRQ1N, IRQ1N | 1 | 1 | 0 |
| None | 1 | 1 | 1 |

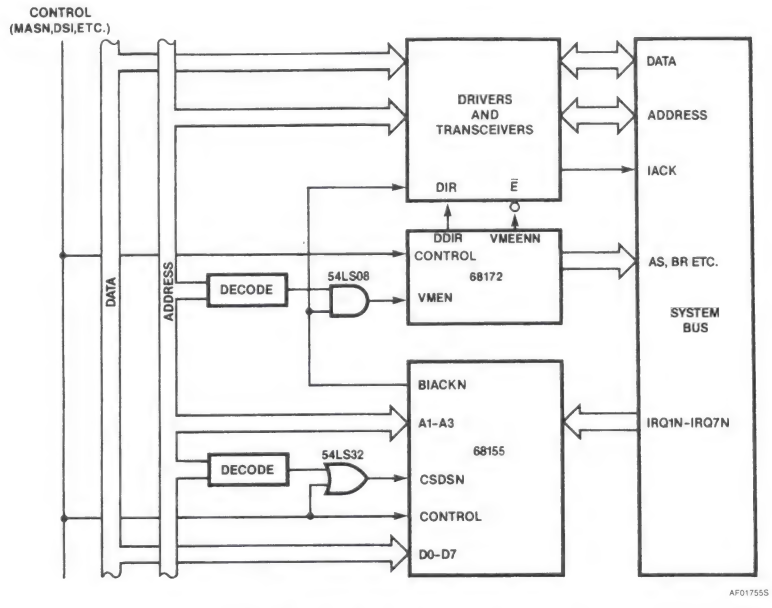



**Figure 1. Typical System Configuration**

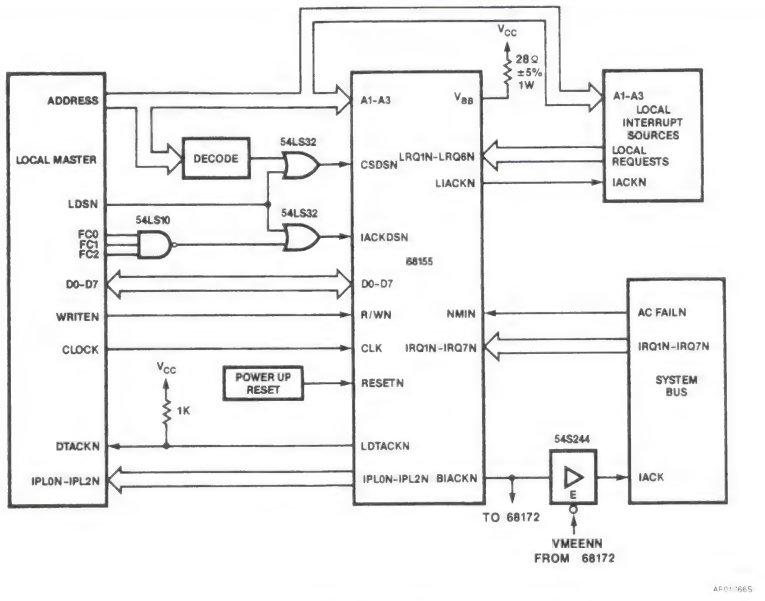
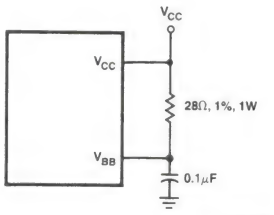
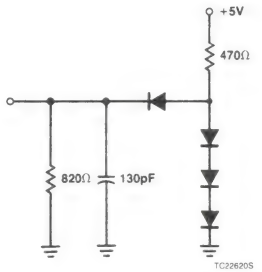



**Figure 2. Local Master Configuration Using 68155**

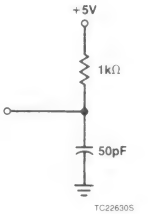
## $V_{BB}$ TEST CIRCUIT




## LOAD CONDITIONS




Signals: D0 – D7, LTACKN
IPL0N – IPL2N, BIACKN




Signals: LDTACKN

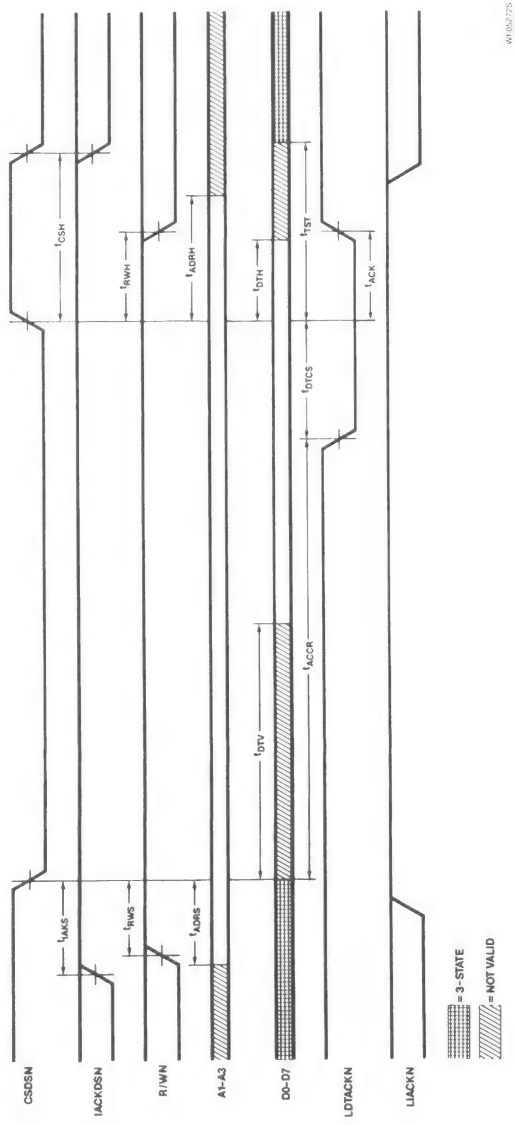



Figure 3. Register Read[5]

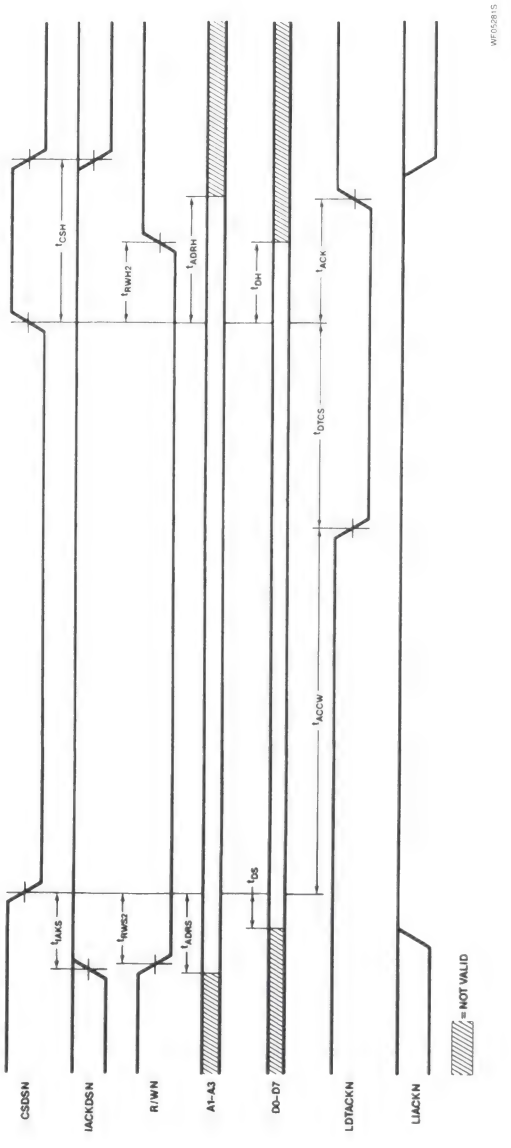



Figure 4. Register Write[5]

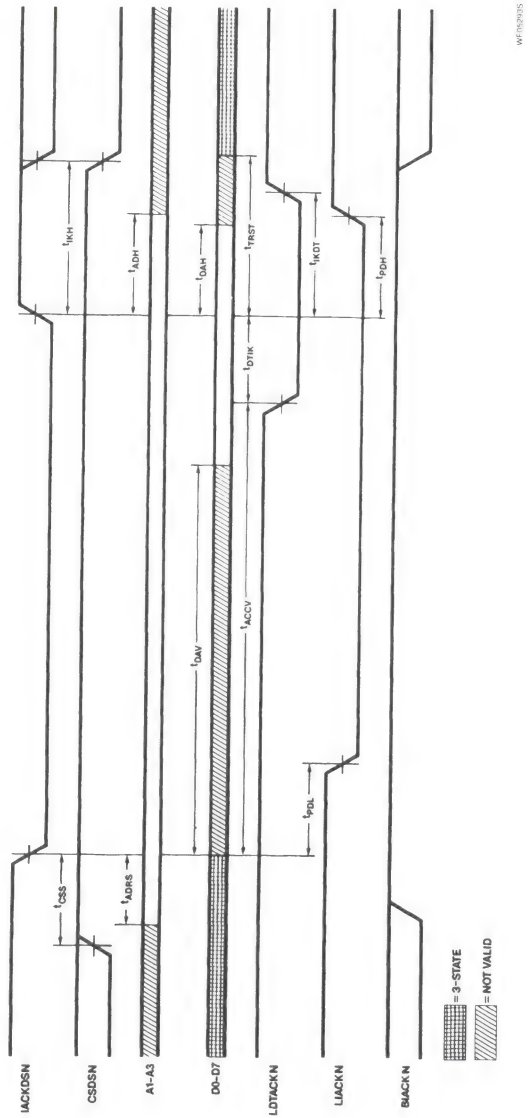



Figure 5. Local Interrupt Acknowledge (Vector Mode)[5]

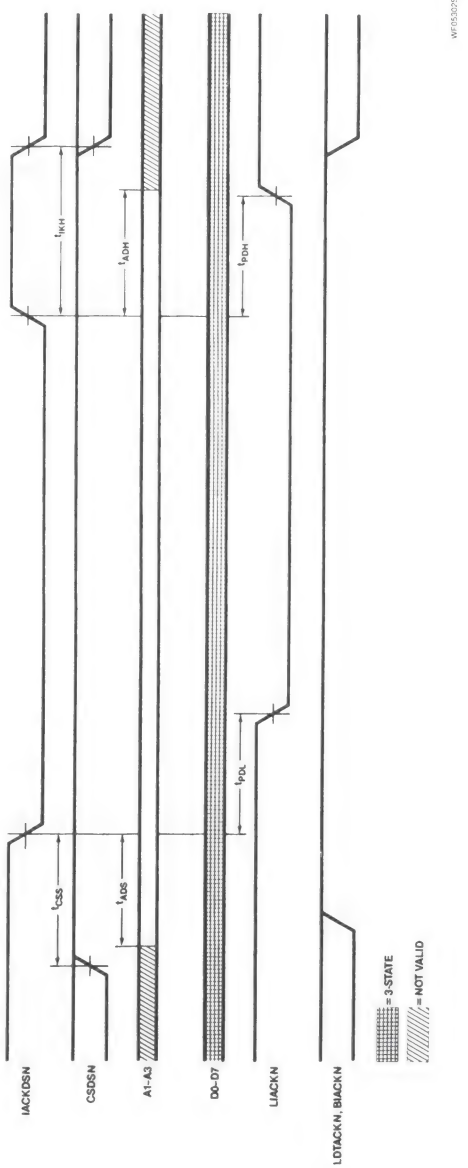



Figure 6. Local Interrupt Acknowledge (Non-Vectored Mode)[5]

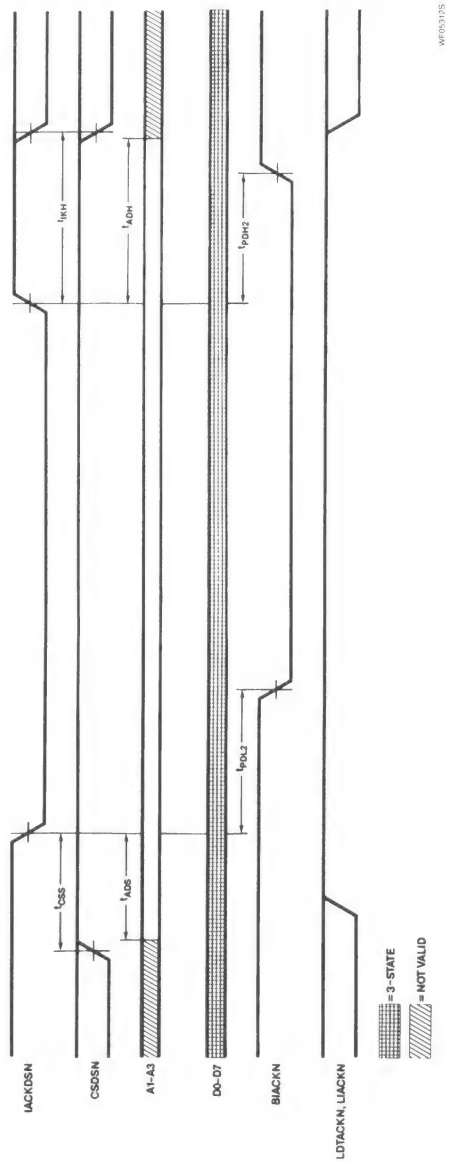



Figure 7. Bus Interrupt Acknowledge[5]

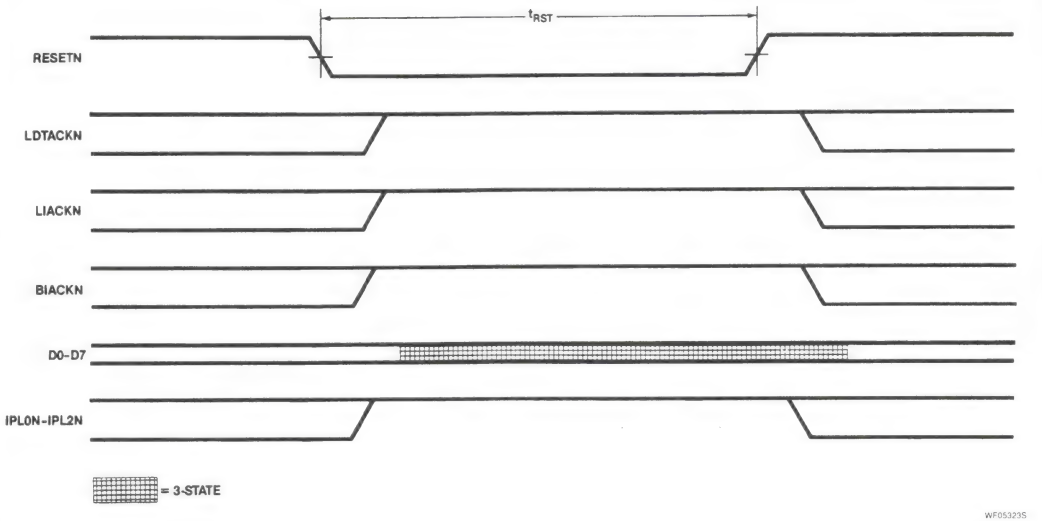



Figure 8. Reset[5]

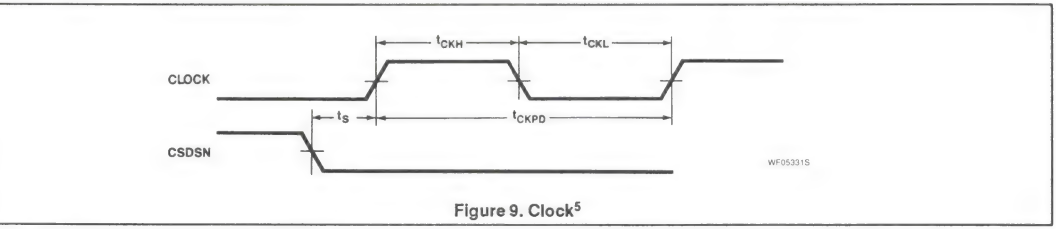



Figure 9. Clock[5]

Signetics

# 68172

## VMEbus Controller (BUSCON)

*Product Specification*

**Military Customer Specific Products**

### DESCRIPTION

The Signetics 68172 VMEbus Controller (BUSCON) is an interface device for the VMEbus. It can be used in three different configurations: master-only, slave-only, and master/slave. The 68172 can be used with a processor-type interface or with a DMA controller-type interface. In all configurations, it handles the VMEbus signaling protocol in compliance with revisions B and C of the VMEbus Specification.

### CONFIGURATION/VERSION

Applications of the BUSCON are identified as follows (see Figures 1 through 4):

| VERSION | APPLICATION |
|---|---|
| PMS | Processor-type master/slave |
| DMAC | DMA controller/type master/slave |
| MS | Either PMS or (DMAC) |
| M | Master-only |
| S | Slave-only |

All of these applications are handled by the 68172, with unused pins tied to stated logic levels in some of the applications.

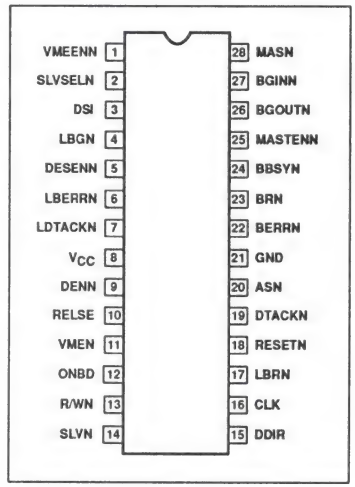
Figure 5 shows a functional model of the 68172 logic. The ASN, MASN, LBRN, BGINN, and RELSE inputs are internally synchronized to CLK before being presented to the state machine which determines the major functions of the device. The SLVN, ONBD, and VMEN signals are used directly in the state machine, although they are highly qualified to prevent metastable conditions on the state machine outputs. the BRN, BBSYN and LBGN signals are direct state machine outputs, while ASN, MASTENN, VMEENN, SLVSELN, and BGOUTN are derived from the state machine outputs plus some combinatorial qualification.

The DSI, R/WN, DTACKN, BERRN, LDTACKN, and LBERRN inputs function largely as direct combinatorial inputs. The DDIR, DTACKN, BERRN, LDTACKN, LBERRN, and (when applicable) MASN outputs are largely derived directly from these direct inputs, with some qualification from the state machine outputs. The DENN and DSENN outputs have complex multi-case logic which uses both the direct inputs and the state machine outputs.

### FEATURES

- **Master, slave, or master/slave (dual ported) applications**
- **Helps assure VMEbus compatibility**
- **Allows for address decoding time**
- **Processor or DMA controller interface for master/requester**
- **Master/requester logic allows release on request (ROR) or release when done (RWD) operation, early or intercycle release**
- **Supports and exploits address lookahead**

### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDERING CODE |
|---|---|
| 28–Pin CERDIP | 68172/BXA |

## PIN DESCRIPTION

| MNEMONIC | PIN NO. | TYPE | CONFIG | NAME AND FUNCTION |
|---|---|---|---|---|
| CLK | 16 | I | All | **Clock:** User-supplied clock signal. |
| SLVN | 14 | I | S,MS | **Slave:** Active-low decode of the VMEbus address and address modifier lines indicating that the current cycle is for this board. SLVN should not be qualified with ASN nor VMEENN. It is first sampled on the rising clock edge after the rising edge on which ASN is first detected. It must remain valid until after the next low-going edge on DTACKN or BERRN. In a master-only application, SLVN should be pulled up to $V_{CC}$. |
| ASN | 20 | I/O<br>I | M,MS<br>S | **Address Strobe:** Direct connect to VMEbus ASN. |
| VMEN | 11 | I | M,MS | **VME Decode:** Active-low decode of the master's address lines, indicating that the master's current cycle is for a slave on the VMEbus. VMEN should not be qualified with MASN nor MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until MASN goes false (high). In a slave-only configuration, VMEN should be pulled up to $V_{CC}$. |
| LBRN | 17 | I | M,MS | **Local Bus Request:** Connected to the low-active bus request output of a DMA controller. Typically tied to a high logic level in processor-type interfaces. |
| ONBD | 12 | I | MS | **Onboard:** Active-high decode of the master's address lines, indicating that the master's current cycle is for an onboard slave that is dual-ported with the VMEbus. ONBD should not be qualified with MASN or MASTENN. It is first sampled on the rising clock edge after the one on which MASN is first detected. Thereafter, it must remain valid until after MASN goes false (high). In a master-only or slave-only application, ONBD should be grounded. If a master/slave configuration does not contain "local slaves" as shown in Figure 3, VMEN and ONBD should both be connected to an active-low "VME decode". A cycle between the onboard master and a local slave (VMEN high, ONBD low) is ignored by BUSCON, and can proceed concurrently with a cycle between another VMEbus master and an onboard dual-ported slave. |
| MASN | 28 | I | M,PMS<br>DMAC | **Master's Address Strobe:** RMW and Sequential VMEbus master cycles are accomplished by holding MASN low across several data strobes. If LBGN is high at the end of the RESETN low time, the state of ASN is driven onto MASN whenever BUSCON does not have control of the VMEbus. In a slave-only application, MASN should be pulled up to $V_{CC}$. |
| MASTENN | 25 | O | MS | **Master Enable:** In a master/slave application, the low state of this signal enables the master onto the shared bus and enables shared-bus responses back t the master. MASTENN also provides the direction control for the VMEbus address transceivers. |
| VMEENN | 1 | O | M,MS | **VME Enable:** Active-low enable for the VMEbus address drivers (master-only) or transceivers (master/slave). |
| SLVSELN | 2 | O | S,MS | **Slave Select:** Active-low select for the onboard slave resources (the shared/dual ported slaves in a master/slave application). Derived from MASN and ONBD, or from ASN and SLVN. If necessary, MASTENN and VMEENN are cycled to provide address setup time before SLVSELN is asserted. |
| BRN | 23 | O | M,MS | **Bus Request:** Active-low, open-collector VMEbus request. Direct connect to the selected level among VMEbus BR0* - BR3*. |
| BGINN | 27 | I | M,MS | **Bus Grant In:** Direct connect to the selected level among VMEbus BG0IN* - BG3IN*. |
| BGOUTN | 26 | O | M,MS | **Bus Grant Out:** Direct connect to the selected level among VMEbus BG0OUT* - BG3OUT*. |
| BBSYN | 24 | O | M,MS | **Bus Busy:** Active-low, open-collector direct connect to VMEbus BBSY*. |
| LBGN | 4 | I/O | M,MS | **Local Bus Grant:** Active-low, open-collector. Can be connected to the bus grant input of a DMA controller. Asserted when LBRN is low and the BUSCON has control of the VMEbus. Grounded, or driven low during RESET, to prevent the ASN state being driven onto MASN when the BUSCON is not in control of the VMEbus. |
| RELSE | 10 | I | M,MS | **Release:** Active-high signal indicating that the onboard logic wants to release control of the VMEbus. In DMA controller applications, the BGACKN output of the DMAC should be connected to (or positive-logic ANDed into) this signal. |
| DTACKN | 19 | I/O<br>O | M,MS<br>S | **Data Transfer Acknowledge:** Active-low, open-collector. Direct connect to VMEbus DTACK*. |
| BERRN | 22 | I/O<br>O | M,MS<br>S | **Bus Error:** Active-low, open-collector. Direct connect to VMEbus BERR*. |
| LDTACKN | 7 | O, I/O<br>I | M,MS<br>S | **Local DTACK:** Active-low, open-collector. Output to onboard master and/or input from onboard slave. |

## PIN DESCRIPTION (Continued)

| MNEMONIC | PIN NO. | TYPE | CONFIG | NAME AND FUNCTION |
|---|---|---|---|---|
| LBERRN | 6 | O, I/O I | M,MS S | **Local Bus Error:** Onboard active-low, open-collector. Output to onboard master and/or input from onboard slave. |
| DSI | 3 | I | All | **Data Strobe:** The high-active or of the onboard data strobes, which may be from the on board master or VMEbus master. |
| DSENN | 5 | O | M,MS | **Data Strobe Enable:** Low-active, used to enable the onboard data strobes onto the VME bus. |
| R/WN | 13 | I | All | **Read/Write:** Onboard R/W signal from the onboard master or VMEbus master. |
| DDIR | 15 | O | All | **Data Direction Control:** Direction control for VMEbus data transceivers. A high level indicates the "onboard-to-VMEbus" direction. |
| DENN | 9 | O | All | **Data Enable:** Low-active enable for VMEbus data transceivers. |
| RESETN | 18 | I | All | **RESET:** Low-active reset. Clears BUSCON logic. |
| $V_{CC}$ | 8 | I | All | **Power Supply:** +5 volts. |
| GND | 21 | I | All | **Ground:** 0V reference. |

## ADDRESS DECODING

Both the VMEbus and current high-speed processors provide short address-to-strobe setup times, such that with all but the most simple decode schemes, designers must provide for delaying the strobe until decoder outputs have become valid. However, BUSCON operates as a finite-state machine and must synchronize address strobes and other inputs before it can act on them. The BUSCON design allows this synchronization time to be overlapped with address decoding.

In general, most BUSCON inputs do not have critical timing parameters. Exceptions are the three address decode signals. Figure 6 shows a somewhat simplified model of the VMEbus slave selection logic in the 68172. The ASN signal is qualified and sampled by flip-flops A and B on each rising edge of CLK. Flip-flop C is set when ASN is high between cycles, and cleared by a falling edge on DTACKN or BERRN.

On the rising edge of CLK after flip-flop B samples ASN low, if C is still set and SLVN is low, flip-flop D is set, indicating slave selection. (In reality, there are more terms in the logic to set D.) Once D is set, it remains set until flip-flop A samples ASN high and a similar circuit (not shown) samples DSI low.

Since SLVN is a direct input to flip-flop D, it must meet a setup time to the clock after ASN is sampled low. Viewed asynchronously, SLVN should be valid slightly less than one clock period after ASN goes low, through shortly after DTACKN goes low.

The onboard logic driven by MASN, VMEN, and ONBD is similar, but not as complex. Neither flip-flop C nor a data-strobe-related signal are used, and there are separate flip-flops corresponding to D for each of the VMEN and ONBD signals. VMEN and ONBD should be valid slightly less than one clock period after MASN goes low, through shortly after MASN goes high.

Because ASN and MASN are used directly to clear the corresponding "flip-flop B", their minimum high times are relatively short. However, for consecutive cycles, the inactive time of "flip-flop D" (and signals derived from it) will be at least two clock periods because of the feedback path from "D" to "B".

## VMEbus ARBITRATION

BUSCON begins VMEbus arbitration by driving BRN low if MASN, VMEN and ONBD indicate a VMEbus cycle (or if LBRN goes low) and the BUSCON does not have control of the bus.

After driving BRN, BUSCON waits for the BGINN input which is connected to the selected one among the four VMEbus arbitration levels. (During this time it can of course respond t cycles from other VMEbus masters.) When it receives BGINN low while holding BRN low, it drives BBSYN low and thereafter releases BRN. (If it receives BGINN low at any other time, it drives BGOUTN low and continues to do so until BGINN goes high.)

Once BUSCON has driven BBSYN low, it waits for any current VMEbus cycle to complete as evidenced by ASN high. Then it begins to drive ASN (initially high) and drives VMEENN low to enable the address out onto the VMEbus.

If the BRN was initiated by MASN, BUSCON then waits two clock periods for address setup time before driving ASN low. If the bus acquisition was initiated by LBRN, it waits for MASN.

BUSCON will release the BBSYN signal on a rising clock edge at which all of the following conditions are met:

1. It is at least three clock periods after the edge on which BBSYN was asserted, and
2. Any prior master's cycle has completed and VMEENN has been driven low, and
3. The BGINN input was high on the last rising clock edge, and
4. The RELSE input was high on the last rising clock edge, and
5. It is not the clock edge at which BUSCON asserts ASN, and
6. It is not the clock edge at which BUSCON withdraws ASN, and
7. LBRN was high on the last rising clock edge.

If BBSYN is released while BUSCON is not driving ASN low, then VMEENN goes high when BBSYN is released, to release the VMEbus. Otherwise, VMEENN goes high shortly before ASN goes high.

RELSE is provided to allow user determination of the method of VMEbus release. The BGACKN output of a DMA controller can be connected to (or included in) this signal to allow the device to control how long it keeps the bus. The OR of the VMEbus requests can be connected to (or included in) this signal for release on request (ROR) operation. If RELSE is connected to a constant logic high, BUSCON will release the bus as soon as possible, i.e. during the first bus cycle.

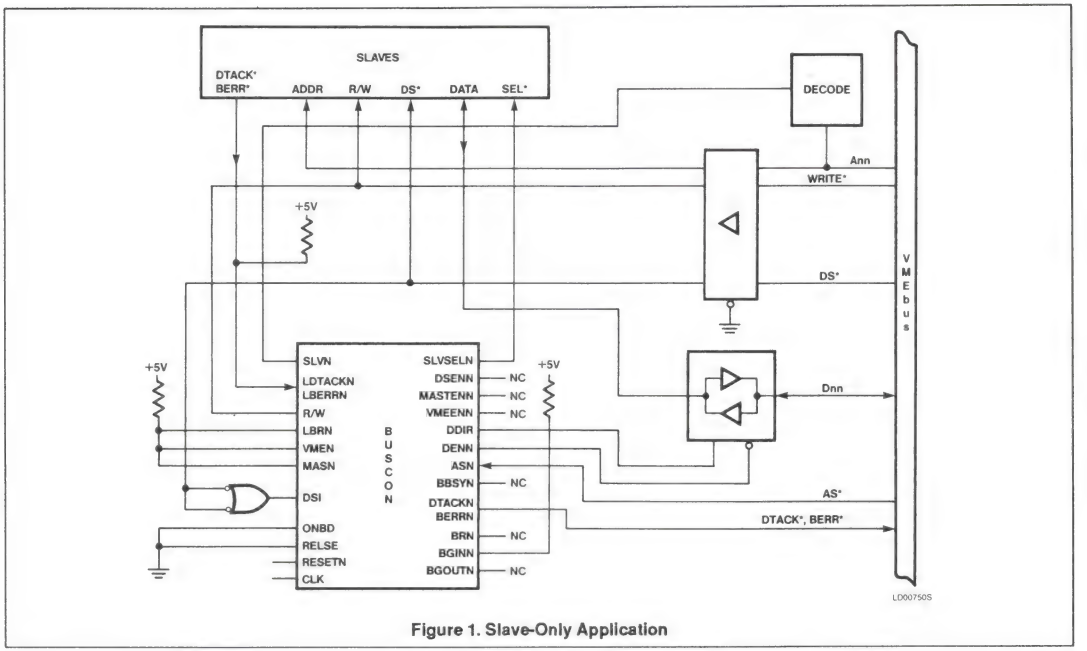



Figure 1. Slave-Only Application

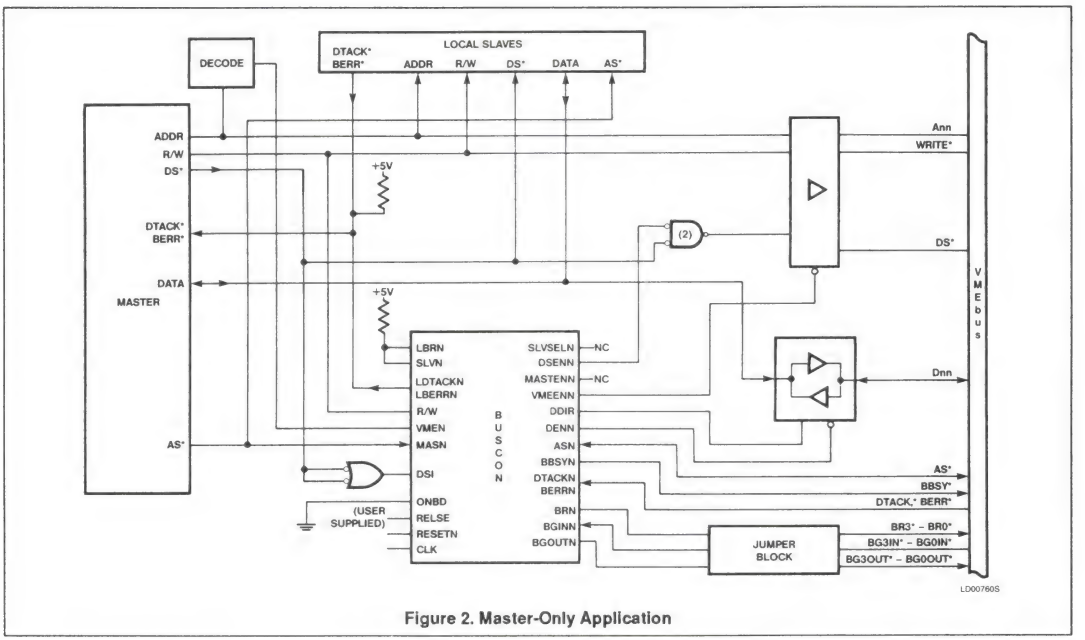



Figure 2. Master-Only Application

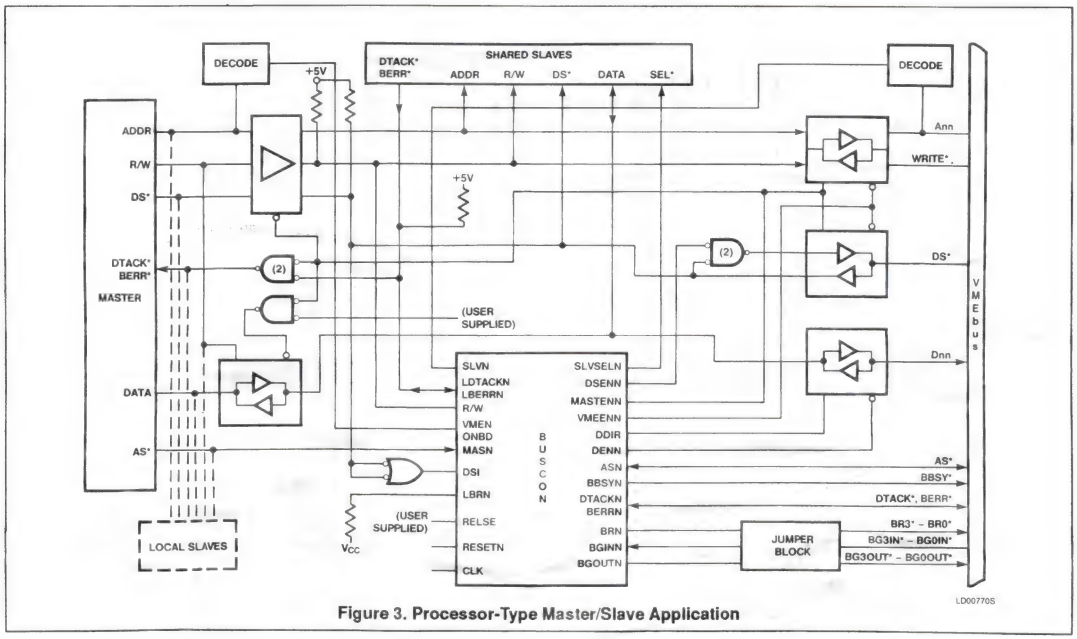



Figure 3. Processor-Type Master/Slave Application

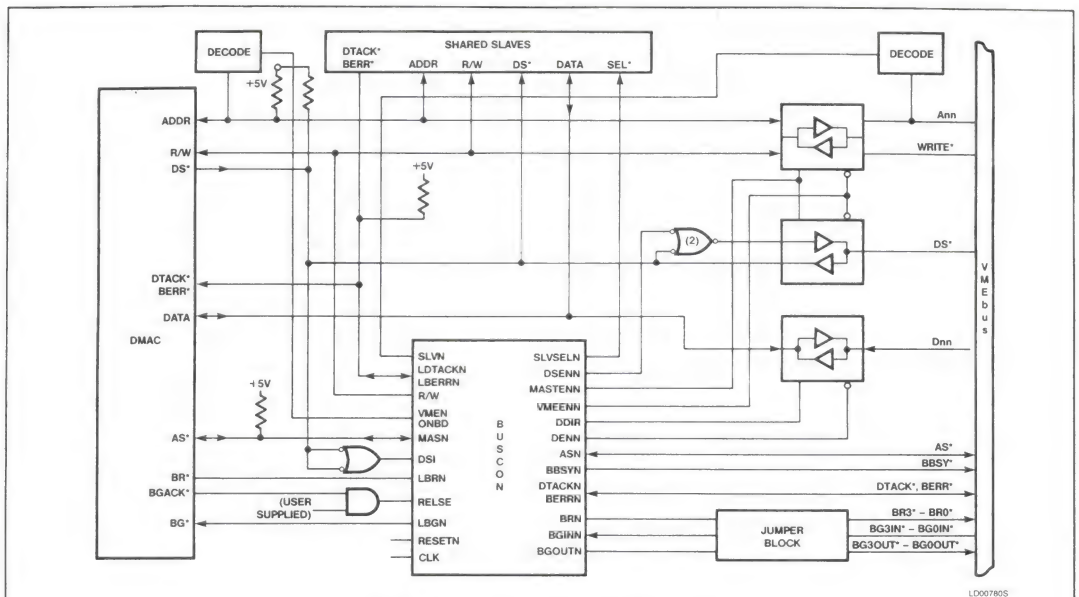



Figure 4. DMAC-Type Master/Slave Application

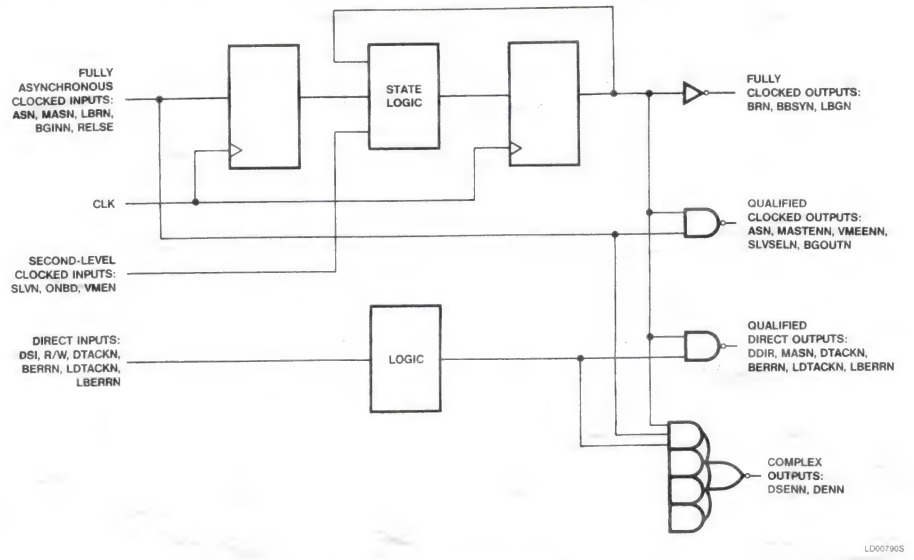



Figure 5. Functional Model

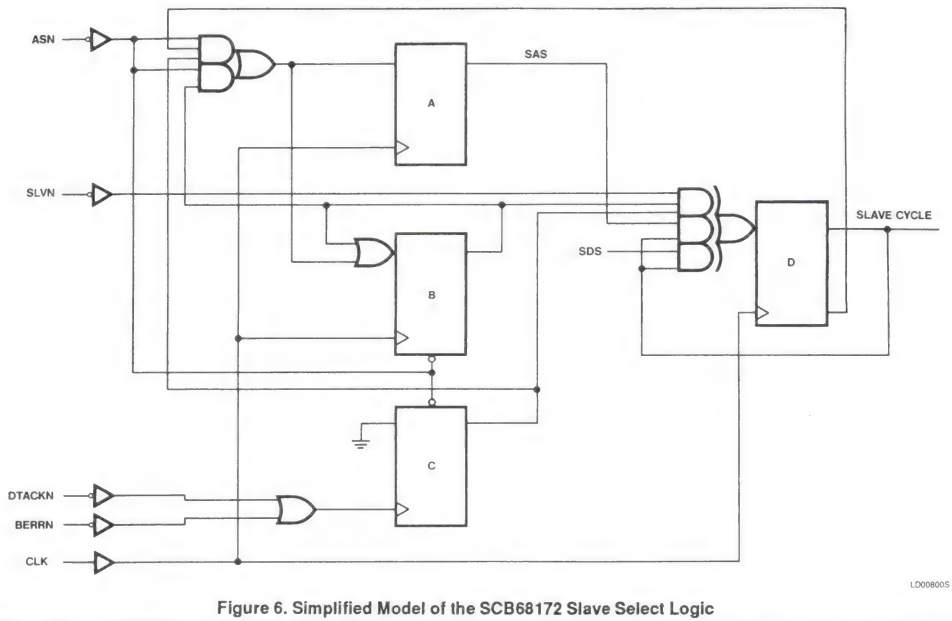



Figure 6. Simplified Model of the SCB68172 Slave Select Logic

## VMEbus MASTER OPERATION

When the BUSCON has VMEbus control, VMEbus cycles indicated on MASN and VMEN produce ASN low on the VMEbus. DDIR and DENN control the VMEbus data transceivers. DDIR reflects the R/WN line.

In a write operation, DENN is driven low to drive data onto the VMEbus whenever the BUSCON has control of the VMEbus, R/WN is low, and the previous VMEbus slave has released DTACKN and BERRN to high. (The DTACKN/BERRN requirement does not apply to subsequent cycles among consecutive writes, if R/WN is maintained continuously low.) DSENN is then driven low when DENN has been low for more than a clock period, and DTACKN and BERRN are high, but not before ASN is driven low. DSENN goes high after DSI goes low or MASN goes high, whichever occurs first. DENN goes high after R/WN goes high, or with VMEENN going high, whichever occurs first.

In a read operation (R/WN is high), DENN goes low to drive data in from the VMEbus after ONBD and VMEN have been sampled, DSI is high, and MASTENN is low. DSENN goes low after DSI, DTACKN, and BERRN are all high, but not before ASN goes low. DSENN and DENN go high after DSI goes low or MASN goes high, whichever occurs first.

DTACKN and BERRN are inputs and drive LDTACKN and LBERRN as outputs. LDTACKN and LBERRN are released when the onboard master makes DSI low. If the VMEbus slave continues to hold DTACKN or BERRN low thereafter, DSENN, LDTACKN and LBERRN are inhibited for the next cycle until the response is released.

MASTENN and VMEENN are kept low while the BUSCON has VMEbus control. The MAS-to-AS delay thus provides automatic address-setup time for subsequent VMEbus cycles.

The need to transceive the data strobes in a master/slave application, plus qualify the on-board master's strobes with DSENN for output, can be accomplished in several ways as shown in Figure 7.

## MASTER/SLAVE SWITCHING

BUSCON includes arbitration and switching logic between VMEbus slave cycles and onboard master cycles (to a shared onboard slave or the VMEbus). The logic remains in its previous direction until forced to switch by another cycle. This provides minimum overhead for slave-only or master-only operation, and for consecutive cycles from the same master.

If a master cycle to a shared slave occurs, or BGINN arrives when requesting the VMEbus, after a slave cycle with another VMEbus master, VMEENN goes high to disable the address from the VMEbus. On the next clock edge, MASTENN goes low to enable the master's address back out onto the onboard bus.

For a VMEbus master cycle, if the current VMEbus cycle is also over, VMEENN then goes low to enable the address out onto the VMEbus.

For a master cycle to a shared slave, SLVSELN goes low one clock period after MASTENN goes low, or if the master direction is continuing, after ONBD is sampled high. SLVSELN goes high shortly after MASN goes high. DTACKN and BERRN are isolated from LDTACKN and LBERRN. DSENN is kept high. DENN is kept high except in a write cycle when BUSCON has VMEbus control.

If an onboard master cycle and VMEbus slave cycle both arrive for the shared slaves within the same clock period, the previous direction of the master/slave switch is retained.

## VMEbus SLAVE OPERATION

If a VMEbus slave cycle occurs after a master cycle, or while BUSCON is requesting the VMEbus, MASTENN goes high, and on the subsequent clock VMEENN goes low to enable the VMEbus address and control signals onto the board.

SLVSELN goes low one clock period after VMEENN goes low, to signal the shard slave(s) that a cycle is occurring. If the slave mode is continuing, SLVSELN goes low after SLVN is sampled low. SLVSELN goes high shortly after ASN goes high.

DDIR reflects R/WN (in the opposite sense from master operation). LDTACKN and LBERRN are inputs and drive DTACKN and BERRN as outputs.

In write operations, DENN is driven low (to enable data in) whenever R/WN is low and LDTACKN and LBERRN are high. When switching between master and slave operation with R/WN low, DENN sequences line VMEENN.

In read operations, DENN is driven low (to enable data out) after SLVN has been sampled low, and while R/WN and DSI are both high.

## SLAVE-ONLY USE

This is the simplest application of the BUSCON. However, handling of board-selection logic from a simple VMEbus address decode, plus driving and sequencing of DTACKN and BERRN, can save VMEbus designers cost and board space even in this application.

## SLAVE DESIGN

In the MS and S configurations, slaves operate off the data strobes and SLVSELN rather than address and data strobes. It should be noted that SLVSELN will typically go low after the data strobes go low. Data should not be written nor placed on the data lines until SLVSELN goes low.

## 68000 DUAL-PORTED OPERATION

BUSCON is ideal for use on a VMEbus board containing a 68000 processor. The obvious approach to dual-porting memory and other slaves, on a board with a 68000, is to use the BRN input of the 68000 to suspend processor operation while another master accesses the onboard slave. This works fine except when the processor has already started a cycle for the VMEbus. This latter coincidence threatens a "deadlock" situation and requires that the processor be "rolled back" off the board's shared bus so that the other master's cycle can occur first. The 68000 has a feature which can be used for this; assertion of both its BERRN and HALTN inputs cause it to suspend operation and retry the cycle when the inputs are released.

The BUSCON does not use these features because there is a flaw in the retry logic. The retry logic does not function during an indivisible RMW sequence (TAS instruction), even in the read cycle. Instead, the assertion of BERRN and HALTN causes an actual bus error exception. It is believed that there is no reliable and general programming solution to the problem of finding the start of the TAS instruction for restart. With 6801x processors, the situation is better because the TAS can be restarted. In any case BUSCON elects to isolate the processor with a few more packages rather than adding complexity tot he error-handling software because of dual-ported design.

## DMA USE

The BUSCON can be used for VMEbus boards which contain a DMA controller but no processor. Such DMA applications are always master/slave due to the need to program the DMA controller from the VMEbus. There are two operational features of the 68172 that are intended for use with DMA controllers. First, the LBRN input can be used to request control of the VMEbus directly, rather than waiting for MASN low and VMEN low as in a processor application. Second, the SCB68172 samples the state of the LBGN pin when RESTN is low. If LBGN is low at the end of RESETN, MASN is used as an input only. If LBGN is high (at the end of the RESETN pulse), the BUSCON thereafter drives the state of VMEbus ASN onto MASN whenever it does not have control of the VMEbus.

For 68000 family DMA controllers, MASN is connected directly to the controller's address strobe pin. The VMEbus ASN-to-MASN feature satisfies the requirement of some DMA controllers that ASN be low on cycles which program

them, and also serves to delay the activity of a controller which gets an LBGN response during the last VMEbus cycle by another master.

When LBRN is sampled low, the BUSCON has retained VMEbus control from previous DMA activity, it continues to retain control for the duration of LBRN being low, and drives LBGN low on the next clock.

Otherwise, it drives VMEbus BRN low on the next clock. When BGINN is sampled low, BBSYN is driven low on the next clock. LBGN is driven low on the same clock as BBSYN if VMEbus ASN is high. If ASN is low, LBGN is driven low one clock after BBSYN, except when ASN low and BGINN are both sampled low for the first time in the same clock period and the VMEbus cycle addresses this board — in this last case, LBGN is driven low two clocks after BBSYN. In either of the last two cases, VMEbus ASN low makes MASN low before LBGN goes low, which keeps the DMA controller from starting until the current VMEbus cycle is over.

Note that the local bus request/grant logic and ASN-to-MASN drive feature are separate capabilities, either or both of which can be used in applications not involving a DMA controller. However, note also that when the state of the ASN is driven onto MASN, this is done without conditioning by the state of the master-slave switch. This means MASN can go low before MASTENN and VMEENN have been cycled to bring the VMEbus address onto the board. (The low state of SLVSELN indicates that the VMEbus address is valid on the board.)

DMA applications are always considered master/slave due to the need to program the DMA controller. The BUSCON assumes that it must always have VMEbus control before answering an LBRN with LBGN. If this is not desired, i.e., if the DMA controller will sometimes be programmed to do onboard transfers solely and the designer wishes to optimize for this case, then a processor-type interface should be used, and isolation devices and additional onboard logic are required.

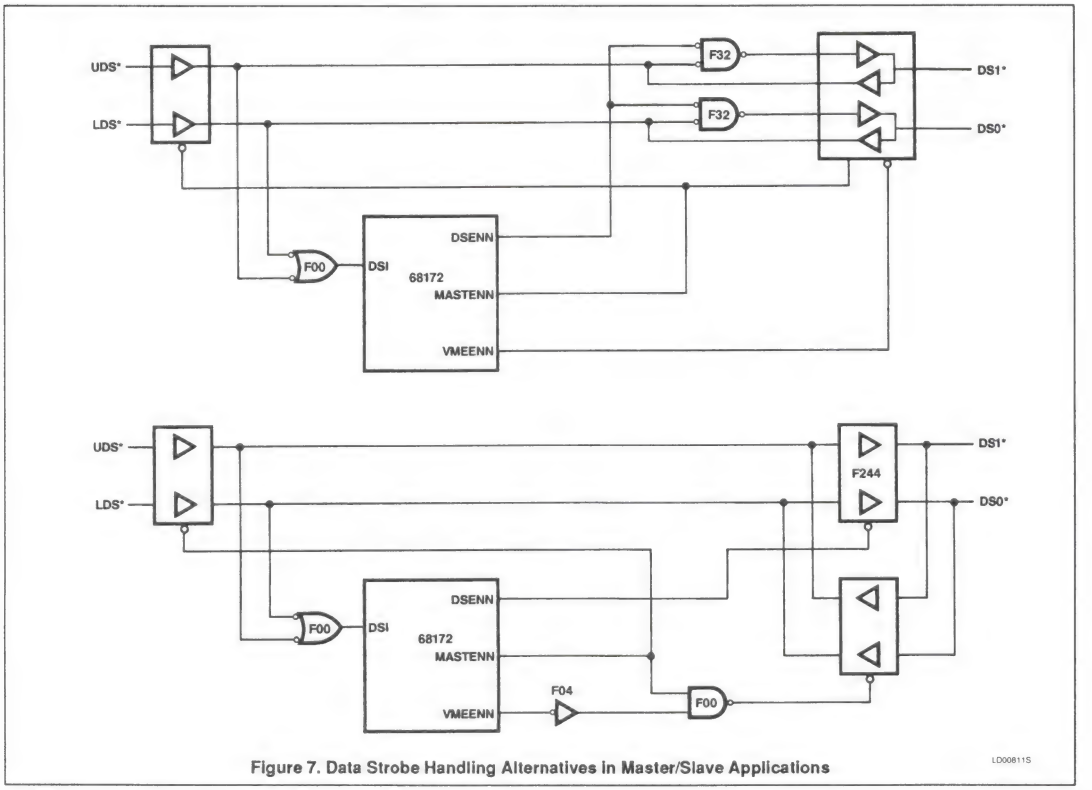



**Figure 7. Data Strobe Handling Alternatives in Master/Slave Applications**

## INTERRUPT HANDLING

When a processor handles interrupts from onboard sources and from the VMEbus, the design must include logic to decide whether an interrupt acknowledge cycle is an onboard or offboard cycle. This logic is quite different from the address decoding logic used to make this decision on other cycles.

Performance can be maximized if the interrupt logic can provide ONBD and VMEN within the specified time after MASN goes low, or if the signals can be made to meet their specified set-up and hold times for CLK. In this case ONBD and VMEN need be selected between the IACK and non-IACK sources. Otherwise (i.e., if the interrupt logic presents these signals slowly and asynchronously), MASN must also be selected between the IACK and non-IACK sources.

## MASTER BLOCK TRANSFER

The block transfer feature of the VMEbus allows considerable performance improvement for transferring a block of consecutive memory

locations. The BUSCON can be used for block transfer operations in the master role.

Master block transfers are applicable to cache subsystems or block transfer on processor boards, and to DMAC-type designs. The only requirements for master block transfers operation with the BUSCON are that external logic must place a block transfer address modifier (AM) code on the VMEbus, and then hold MASN low across a number of data strobes.(Note that a long block transfer can compromise the operation of other VMEbus masters. One strategy to avoid such problems could be to do a minimum of 4 or 8 transfers without interruption, and then switch to release on request (ROR) operation.)

A sample circuit for master block transfers is shown in Figure 8. Here, a block transfer is triggered whenever the DMAC accesses a certain range of addresses. The SEQ signal could of course be generated in other ways.

## SLAVE BLOCK TRANSFERS

VMEbus slaves that are capable of block transfers latch the bus address into a set of counters on the leading edge of ASN, and then increment the address for each data transfer. The 68172 can be used on such slave boards in accordance with revision C of the VMEbus specification.

The revision C specification introduces a limitation on block transfers, namely that a master is not allowed to continue a block transfer across a 256-byte boundary. This limitation has a number of advantages, including reducing the number of counter devices needed on slave boards, allowing straightforward use of page or static column modes on dynamic memories, providing periodic windows in a long block transfer in which higher-priority masters can gain bus control, and (effectively) preventing a block transfer from crossing from one slave board to another.

It is this last advantage that is of particular importance for the 68172. It means that VMEbus slaves can make a positive selection-decision after ASN goes low, and this decision will remain valid for the duration of the cycle even if it is a block transfer cycle.

In a block transfer which selects an 68172-bused slave board, SLVSELN remains low through the block, until ASN goes high. The onboard slave logic then uses the data strobes to define each data transfer.

The data strobe and acknowledge signals are handled in a high-speed combinatorial fashion by the 68172 in both the master and slave roles. Block transfers are inherently faster on the VMEbus because the address need be passed and decoded only once, and because the slave can look ahead (pipeline) subsequent transfers in a block read cycle. With the 68172, this inherent speed advantage is augmented by the advantage of combinatorial over sequential (arbitrated) logic.

## 3-STATE ENABLE SWITCHING (MASTENN, VMEENN, DENN)

As a result of speed optimization of master/slave switching, some parts used in PMS applications may exhibit short high-going transients on MASTENN, VMEENN, and/or DENN, if requests for access to the shared slave(s) arrive closely in time from both the onboard master and the VMEbus master. These transients should pose no problem as long as the signals are used as intended (i.e., as 3-State enables). The following points apply:

1. A transient will occur only when SLVSELN has been high for at least one clock period, and at least one clock period before a subsequent low on SLVSELN.
2. A transient will occur only if the current master/slave direction is maintained.
3. Low-going transients (which could cause 3-State conflicts) do not occur.
4. Commonly such transients will be eliminated by external capacitance, and/or rejected by receivers on other parts. In any case the logic levels on signals controlled by these enable signals should not be affected.
5. Edge-sensitive use of these signals is inadvisable in a PMS application.

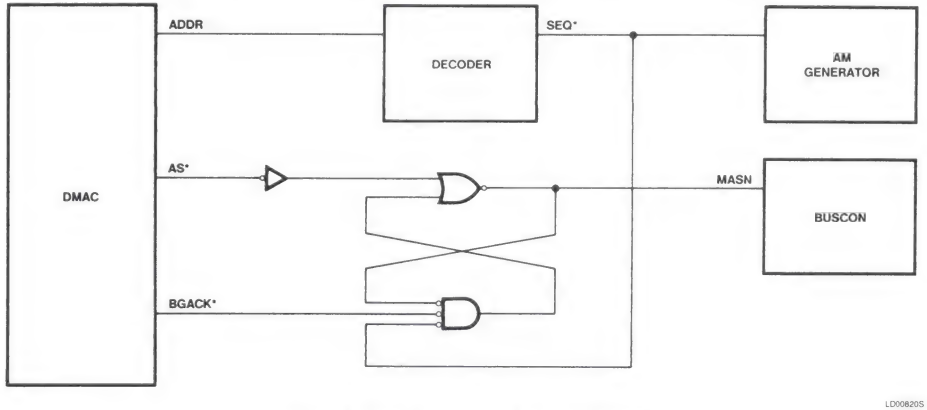
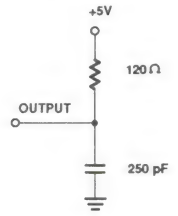


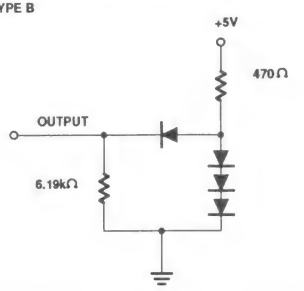

**Figure 8. Master Sequential Mode with DMAC**

**TEST CONDITIONS** unless otherwise noted, the timing parameters are based on loading as follows:

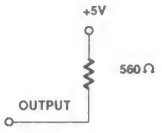
LOAD TYPE A



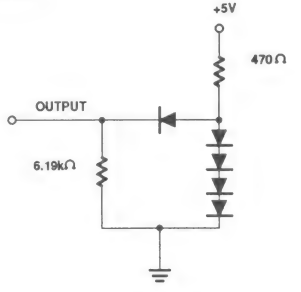

LOAD TYPE B



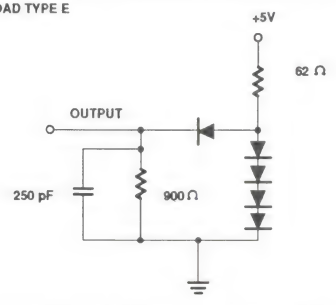

LOAD TYPE C



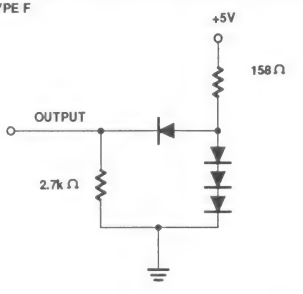

LOAD TYPE D




LOAD TYPE E




LOAD TYPE F




| SIGNALS | LOAD TYPE |
|---|---|
| BBSYN,BERRN,BRN,DTACKN | A |
| BGOUTN,DDIR,DENN,DSENN,SLVSELN,VMEENN | B |
| LBERRN,LBGN,LDTACKN | C |
| MASN | D |
| ASH | E |
| MASTENN | F |

**NOTE:** All capacitive loads calculated with 50pf board capacitance.

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage range | -0.5 to +7.0 | V |
| $V_I$ | Input voltage range | -0.5 to +5.5 | V |
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = 5.0V ± 5%, $T_A$ = -55°C to +125°C[2, 3, 4]

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| **DSI, ONBD, SLVN, VMEN, LBRN, RELSE, RESETN** | | | | | |
| $I_{IL}$ | Input low current | $V_I$ = 0.4V | | -400 | µA |
| $I_{IH}$ | Input high current | $V_I$ = 2.7V | | 20 | µA |
| $V_{IL}$ | Input low voltage | | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | V |
| **ASN, MASN, BGINN, DTACKN, BERRN, LDTACKN, LBERRN** | | | | | |
| $I_{IL}$ | Input low current | $V_I$ = 0.4V | | -400 | µA |
| $I_{IH}$ | Input high current | $V_I$ = 2.7V | | 20 | µA |
| $V_{IL}$ | Input low voltage | | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | V |
| **R/WN, CLK** | | | | | |
| $I_{IL}$ | Input low current | $V_I$ = 0.4V | | -800 | µA |
| $I_{IH}$ | Input high current | $V_I$ = 2.7V | | 40 | µA |
| $V_{IL}$ | Input low voltage | | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | 2.0 | | V |
| **BGOUTN, VMEENN, SLVSELN, DSENN, DENN, DDIR (low current totem pole)** | | | | | |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 8mA, $V_{CC}$ = 4.75V | | 0.5 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -0.4mA, $V_{CC}$ = 4.75V | 2.7 | | V |
| **MASTENN (high current totem pole)** | | | | | |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 24mA, $V_{CC}$ = 4.75V | | 0.5 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -1mA, $V_{CC}$ = 4.75V | 2.7 | | V |
| **MASN (low current 3-State)** | | | | | |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 8mA, $V_{CC}$ = 4.75V | | 0.5 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -0.4mA, $V_{CC}$ = 4.75V | 2.7 | | |
| **ASN (high current 3-State)** | | | | | |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 64mA, $V_{CC}$ = 4.75V | | 0.5 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -3mA, $V_{CC}$ = 4.75V | 2.7 | | |
| **LDTACKN, LBERRN, LBGN (low current open-collector)** | | | | | |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 8mA, $V_{CC}$ = 4.75V | | 0.5 | V |
| $I_{OH}$ | Output leakage current | V = 5.25V | | 100 | µA |
| **DTACKN, BERRN, BRN, BBSYN (high current open-collector)** | | | | | |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 48mA, $V_{CC}$ = 4.75V | | 0.6 | V |
| $I_{OH}$ | Output leakage current | V = 5.5V | | 250 | µA |
| $I_{CC}$ | $V_{CC}$ Supply current | $V_{CC}$ = 5.25V | | 250 | mA |

## AC ELECTRICAL CHARACTERISTICS $V_{CC}$ = 5.0V ± 5%, $T_A$ = -55°C to +125°C.

| NO. | FIGURE | CHARACTERISTIC | LIMITS | | UNIT | NOTES |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| **Clock and general parameters** | | | | | | |
| 1 | 9 - 18, 20 | CLK cycle time (CLK) | 40 | | ns | |
| 2 | 9 - 18, 20 | CLK low time | 15 | | ns | |
| 3 | 9 - 18, 20 | CLK high time | 15 | | ns | |
| **Asynchronous input setup time to CLK high** | | | | | | |
| 4 | 9, 10, 11, 12, 13, 18, 20 | ASN, MASN low | 30 | | ns | 5 |
| 5 | 9, 10, 11, 13 | ASN, MASN high | 25 | | ns | 5 |
| 6 | 9, 10, 11, 12, 13, 20 | SLVN, VMEN low | 20 | | ns | 6 |
| 7 | 11, 17, 18 | SLVN, VMEN high | 33 | | ns | 6 |
| 8 | 9, 10, 13 | ONBD low | 25 | | ns | 6 |
| 9 | 18 | ONBD high | 20 | | ns | 6 |
| 10 | 13, 16, 20 | LBRN, RELSE, BGINN low | 23 | | ns | 5 |
| 11 | 14, 15 | LBRN, RELSE, BGINN high | 10 | | ns | 5 |
| 12 | 11, 12, 13 | DSI low (end of slave cycle) | 30 | | ns | 5 |
| **Asynchronous input hold time from CLK high** | | | | | | |
| 13 | | ASN, MASN, DSI | 0 | | ns | 7 |
| 14 | | ONBD, VMEN | 0 | | ns | 8 |
| 15 | | LBRN, RELSE, BGINN | 2 | | ns | 7 |
| **Propagation, CLK high to:** | | | | | | |
| 16 | 16 | BGOUTN low | 20 | 55 | ns | |
| 17 | 20 | LBGN low | 20 | 70 | ns | |
| 18 | | LBGN high | 11 | 46 | ns | |
| 19 | 13, 16, 20 | BBSYN, BRN low | 17 | 53 | ns | |
| 20 | 13, 20 | BBSYN, BRN high | 14 | 34 | ns | |
| 21 | 9, 10, 13 | ASN low | 12 | 41 | ns | |
| 22 | 9, 10 | ASN high | | 40 | ns | |
| 23 | 11, 12, 13, 18, 20 | SLVSELN, VMEENN low | 14 | 60 | ns | |
| 24 | 13, 18, 20 | MASTENN low | 19 | 42 | ns | |
| **Miscellaneous** | | | | | | |
| 25 | | RESETN width low | 6clk | | ns | 9 |
| 27 | 16 | BGINN high to BGOUTN high | 5 | 17 | ns | |
| 28 | 9, 11 | R/WN high to DSI high (start of read cycle) | 10 | | ns | 39 |
| 29 | 9, 12 | DSI low to RWN low (end of ready cycle) | 10 | | ns | 39 |
| **Address decoding** | | | | | | |
| 33 | 17 | SLVN high after DTACKN low | 22 | | ns | |
| 34 | 9, 10 | VMEN, ONBD valid after MASN high | 10 | | ns | 39 |
| 35 | 9, 10 | MASN high | 15 | | ns | 10 |
| 36 | 9, 10, 11 | DSI low | 20 | | ns | |
| 37 | 11 | ASN high | 20 | | ns | 10 |
| **VMEbus acquisition** | | | | | | |
| 38A | 13, 20 | ASN low to BGINN low (early release by other master) | 10 | | ns | 39 |
| 40 | 13, 20 | BBSYN low to BRN high | | 15 | ns | |
| 42 | 13 | ASN high to VMEENN low, DENN low (write) | 20 | 57 | ns | 12, 13 |
| 43A | 13, 16, 20 | BBSYN or BGOUTN low to BGINN high | 0 | | ns | 39 |

## AC ELECTRICAL CHARACTERISTICS (Continued)

| NO. | FIGURE | CHARACTERISTIC | LIMITS | | UNIT | NOTES |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| **VMEbus master cycles** | | | | | | |
| 46 | 9, 10 | ASN low to DSEN low | -1 | 14 | ns | 17, 18 |
| 47 | 10, 13 | R/WN low to DDIR high | | 36 | ns | |
| 48 | 10, 13 | DDIR high to DENN low (write) | 2 | 11 | ns | 15 |
| 49 | 10 | DTACKN and BERRN high to DENN low (write, 1st bus cycle or preceded by read) | 14 | 41 | ns | 15 |
| 50 | 10 | DENN low to DSENN low (write) | clk+13 | 2clk+53 | ns | 17 |
| 51 | 9, 11, 13 | R/WN high to DDIR low | 13 | 40 | ns | |
| 52 | 9 | DDIR low to DENN low (read) | 7 | 26 | ns | 16 |
| 53 | 9 | DSI high to DENN low (read) | 10 | 30 | ns | 16 |
| 54 | 9 | DSI high to DSENN low (read) | 14 | 45 | ns | 18 |
| 55 | 9, 10 | DTACKN and BERRN high to DSENN low | 15 | 51 | ns | 17, 18 |
| 56 | 9, 10 | DTACKN or BERRN low to LDTACKN or LBERRN low | | 66 | ns | |
| 57 | 9, 10 | LDTACKN or LBERRN low to DSI low or MASN high | 0 | | ns | 39 |
| 58 | 9, 10 | DSI low to DSENN high | | 37 | ns | 19 |
| 59 | 9, 10 | MASN high to DSENN high | | 50 | ns | |
| 60 | 10 | R/WN high to DSENN high (after a write) | | 32 | ns | 20 |
| 62 | 9 | MASN high to DENN high (read) | | 50 | ns | 21 |
| 63 | 9 | DSI low to DENN high (read) | | 39 | ns | 21 |
| 64 | 10 | R/WN high to DENN high (write) | | 30 | ns | 22 |
| 65 | 9, 10 | DSENN high to LDTACKN and LBERRN high | | 54 | ns | 23 |
| 66 | 9, 10 | DTACKN and BERRN high to LDTACKN and LBERRN high | | 17 | ns | 23 |
| **VMEbus release** | | | | | | |
| 67 | 14 | BBSYN low | 2clk | | ns | 39 |
| 71 | 14 | MASN high to VMEENN high or DENN high (early release, write) | 7 | 46 | ns | |
| 73 | 14 | DENN (write) and VMEENN high to ASN high | -6 | 2 | ns | |
| 74 | 14 | ASN high to ASN released (early release) | 6 | 52 | ns | |
| 76 | 15 | DENN (write) and VMEENN high to BBSYN high (intercycle release) | 0 | 19 | ns | |
| 77 | 14, 15 | BBSYN high to RELSE low | 0 | | ns | 39 |
| **Master to slave switching** | | | | | | |
| 78 | | Clock high to MSTEEN high (Clock at which (External) ASN is detected low) | 13 | 30 | ns | 25 |
| 79 | 11, 13, 20 | SLVN low to MASTENN high | | 18 | ns | 25 |
| 80 | 11 | SLVSELN high to MASTENN high | 18 | 35 | ns | 25 |
| 81A | 11, 13 | VMEENN low to DDIR change | -1 | 16 | ns | |
| **VMEbus slave cycles** | | | | | | |
| 85 | 12, 13 | R/WN low to DDIR low | 16 | 45 | ns | |
| 86 | 12, 13 | DDIR low to DENN low (write) | 7 | 25 | ns | 27 |
| 87 | 12 | LDTACKN and LBERRN high to DENN low (write) | 10 | 35 | ns | 27 |
| 88 | 12, 13 | R/WN high to DDIR high | | 17 | ns | |
| 89 | 11 | DDIR high to DENN low (read) | 4 | 12 | ns | 28 |
| 91 | 11 | DSI high to DENN low (read) | | 29 | ns | 28 |
| 92 | 11, 12, 13, 18 | SLVSELN low and DSI high to LDTACKN or LBERRN low | 0 | | ns | 29, 39 |
| 93 | 11, 12, 13, 18 | LDTACKN or LBERRN low to DTACKN or BERRN low | | 48 | ns | |
| 94 | 12, 13 | LDTACKN or LBERRN low to DENN high (write) | 10 | 27 | ns | |
| 94A | 11, 12, 13, 18 | DTACKN or BERRN low to DSI low or ASN high | 0 | | ns | 39 |
| 95 | 11 | DSI low to DENN high (read) | | 22 | ns | |
| 96 | 11, 12, 18, 20 | ASN high to SLVSELN high | 14 | 35 | ns | |
| 97 | 11, 12, 13 | DSI low to DTACKN and BERRN high | 14 | 32 | ns | |
| 97A | 11 | DENN high to DTACKN and BERRN high | | 20 | ns | |
| 98 | 11, 12, 13, 20 | DSI low to DTACKN and LBERRN high | 0 | 35 | ns | 30, 32, 39 |
| 99 | 11, 12 | LDTACKN and LBERRN high to (next) DSI high | 0 | | ns | 30, 39 |

## AC ELECTRICAL CHARACTERISTICS (Continued)

| NO. | FIGURE | CHARACTERISTIC | LIMITS | | UNIT | NOTES |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| **Slave to master switching** | | | | | | |
| 100 | | Clock high to VMEENN, DENN (VMEbus slave write high) (Clock which MASN is detected low) | | clk+40 | ns | 31 |
| 101 | 18 | ONBD high to VMEENN, DENN (VMEbus slave write) high | 10 | 40 | ns | 31 |
| 102 | | VMEN low to VMEENN, DENN (VMEbus slave write) high | 9 | 26 | ns | 31 |
| 103 | 13, 18, 20 | SLVSELN high to VMEENN, DENN (VMEbus slave write) high | 0 | | ns | 31 |
| 104 | | Clock high to VMEENN, DENN (VMEbus slave write) high (Clock at which DSI (selected) is detected low) | 10 | 40 | ns | 31 |
| **Onboard cycles** | | | | | | |
| 111 | 18 | MASN high to SLVSELN high | 10 | 40 | ns | |
| **DMAC-Type operation** | | | | | | |
| 112 | 19 | Clock high to MASN active (Clock from which BBSYN is driven high) | 22 | 60 | ns | 34 |
| 113 | 19 | ASN high to MASN active | | 20 | ns | 34 |
| 114 | 19 | ASN low to MASN low | 20 | 49 | ns | |
| 115 | 19 | ASN high to MASN high | 5 | 25 | ns | |
| 116 | 19 | ASN high to MASN released | | 48 | ns | 35 |
| 117 | 19 | LBGN low to MASN released | | 50 | ns | 35 |
| 122 | 20 | LBGN low to LBRN high | 0 | | ns | 39 |

Notes on following page.

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other conditions other than those indicated in the Electrical Characteristics section of this data sheet is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. Parameters are valid over specified temperature range.
4. All voltage measurements are referenced to ground ($V_{SS}$). For testing, all signals swing between 0.4V and 2.4V with a transition time of 10ns maximum. All time measurements are referenced at input voltages of 1.5V.
5. These setup times guarantee recognition at a rising edge of CLK, but the device will operate correctly if they are not met. If the asynchronous input is changed between the setup and hold times, the new state of the input may be recognized at this clock or the following clock.
6. These setup times are required on the rising edge of CLK following the one on which ASN or MASN is first recognized low. If parameters 30, 31, and 32 are met, these parameters are automatically guaranteed.
7. These hold times guarantee (continued) recognition of the signal state at a rising edge of CLK, but the device will operate correctly if they are not met.
8. These hold times are required on the rising edge of CLK preceding the one on which MASN is first recognized high. Parameter 34 provides a more straightforward requirement which guarantees these times.
9. This parameter applies after $V_{CC}$ and the clock signal are both within the specified limits.
10. These minimum times are to guarantee recognition. Operation will be limited by 44, 83, and 109 if the strobe is high for less than 2clk.
11. BRN is driven low, and this acquisition sequence applies, only if BBSYN is high.
12. VMEENN is driven low only when 41, 42, and 107 have been met.
13. Applies to ASN or VMEbus cycle which does not select this board as a slave.
14. ASN goes low when 43, 44, and 45 are met. 44 is not applicable on the first cycle after acquiring the VMEbus.
15. In a write operation, DENN goes low when 41, 42, 48, 49, and 107 are met. 49 does not apply for subsequent cycles in a series of writes if R/WN is held low throughout.
16. In a read operation, DENN goes low when all of 52, 53, 53A and (as applicable) 41A and 107A are set.
17. In a write operation, DSENN goes low when 46, 50, and 55 are met. 55 is significant only for subsequent cycles in a series of writes with R/WN held low throughout.
18. In a read operation, DSENN goes low when 46, 54, and 55 are met.
19. DSENN goes high when either 58 or 59 is met.
20. Applies only if R/WN remains low after a write cycle, so that DSENN goes low again.
21. In a read operation, DENN goes high when either 63 or 64 is met.
22. In a write operation, DENN goes high when either 64 or 71 is met
23. LDTACKN and LBERRN go high when either 65 or 66 is met.
24. BBSYN is always released in response to BGINN, RELSE, and LBRN all high. However, if this condition is detected during a clock period in which the decision to change ASN is made, the release of BBSYN is delayed one clock period so that 70 or 75 is met.
25. MASTENN goes high when 78, 79, and 80 are all met.
26. SLVSELN goes low when 82, 83, and 84 (as applicable) are met.
27. In a write operation, DENN goes low when 86 and 87 are met.
28. In a read operation, DENN goes low when 89, 90, and 91 are met.
29. The onboard slave(s) should wait for both SLVSELN and DSI before driving a response.
30. Since BUSCON itself terminates DTACKN and BERRN when DSI goes low, the onboard slaves must meet this requirement to assure that a "lingering" LDTACKN or LBERRN is not presented as DTACKN or BERRN when the next DSI occurs. 99 is the real requirement - 98 max is derived from it, plus the 40ns minimum high time of VMEbus data strobes and an allowance for receiver skew.
31. VMEENN goes high only when 100, (101 or 102), 103, and 104 are met. 104 applies only if a VMEbus slave cycle (with this board) is ending.
32. The onboard slave(s) must meet this requirement so that the local response is not inadvertently presented to the onboard master.
33. SLVSELN goes low when 108, 109, and 110 (as applicable) are met.
34. MASN is driven out of Hi-Z state only when 112 and 113 are met.
35. MASN is released to Hi-Z state only when 116 and 117 are met.
36. The max figure applies only if BUSCON has keep VMEbus control (i.e., if BBSYN is low).
37. LBGN goes high only when 123, 125, and 126 are met, but 125 and 126 apply only if a VMEbus slave cycle (with this board) is in progress.
38. These parameters guarantee parameters 6 through 10, but are not absolute requirements. If these parameters are not met, parameters 6 through 10, and 14 must be met for each clock edge from the one following the edge on which MASN or ASN is recognized low, until MASN or ASN goes high.
39. Guaranteed, but not tested.

**DERIVED AC CHARACTERISTICS** The following parameters can be derived directly from the AC Electrical Characteristics. These will not be tested or characterized separately.

| NO. | FIGURE | CHARACTERISTIC | LIMITS | | UNIT | NOTES |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| **Miscellaneous** | | | | | | |
| 26 | 16 | BGINN low to BGOUTN low | clk+18 | 2clk+78 | ns | |
| **Address decoding** | | | | | | |
| 30 | 11, 12, 13, 20 | ASN low to SLVN valid | | clk-30 | ns | 38 |
| 31 | 9, 10, 13, 18 | MASN low to VMEN valid | | clk-30 | ns | 38 |
| 32 | 9, 10, 13, 18 | MASN low to ONBD valid | | clk-22 | ns | 38 |
| **VMEbus acquisition** | | | | | | |
| 38 | 13 | MASN low to BRN low | clk+20 | 2clk+83 | ns | 11 |
| 39 | 13, 20 | BGINN low to BBSYN low | clk+15 | 2clk+76 | ns | |
| 41 | 13 | BGINN low to VMEENN low, DENN low (write) | clk+3 | 2clk+38 | ns | 12 |
| 41A | 13 | BGINN low to DENN low (read) | clk+5 | 2clk+60 | ns | 16 |
| 43 | 13 | VMEENN low to ASN low | clk-11 | 2clk | ns | 14 |
| **VMEbus master cycles** | | | | | | |
| 44 | 9, 10 | ASN high (successive VMEbus master cycles) | 2clk | | ns | 14 |
| 45 | 9, 10 | MASN low to ASN low (subsequent cycle retaining VMEbus control) | clk+18 | 2clk+70 | ns | 14 |
| 53A | 9 | MASN low to DENN low (read) | clk+5 | 2clk+60 | ns | 16 |
| 61 | 9, 10 | MASN high to ASN high (unless early release) | clk+8 | 2clk+75 | ns | |
| **VMEbus release** | | | | | | |
| 68 | 14, 15 | BGINN high to BBSYN high | clk+12 | 2clk+35 | ns | 23 |
| 69 | 14, 15 | RELSE high to BBSYN high | clk+12 | 2clk+42 | ns | 24 |
| 70 | 14 | ASN low to BBSYN high (early release) | clk-8 | | ns | |
| 75 | 15 | ASN high to BBSYN high (intercycle release) | clk-6 | | ns | |
| **Master to slave switching** | | | | | | |
| 81 | 11, 20 | MASTENN high to VMEENN low | 8 | clk+13 | ns | |
| 82 | 11, 13, 20 | VMEENN low to SLVSELN low | clk-20 | clk | ns | 26 |
| **VMEbus slave cycles** | | | | | | |
| 83 | 12 | SLVSELN high (successive slave cycles) | 3clk+56 | | ns | 26 |
| 84 | 12 | ASN low to SLVSELN low (already in slave state) | clk+13 | 2clk+74 | ns | 26 |
| 90 | 11 | ASN low to DENN low (read) | clk+22 | 2clk+80 | ns | 28 |
| **Slave to master switching** | | | | | | |
| 105 | 13, 18, 20 | VMEENN high to MASTENN low | -17 | | ns | |
| 107 | 13, 20 | MASTENN low to VMEENN low, DENN low (write, if next cycle on VMEbus) | | 0 | ns | 12, 15 |
| 107A | 13 | MASTENN low to DENN low (read, next cycle on VMEbus) | -5 | 20 | ns | 16 |
| 108 | 18 | MASTENN low to SLVSELN low (if next cycle on board) | clk-28 | clk+17 | ns | 33 |
| **Onboard cycles** | | | | | | |
| 109 | 18 | SLVSELN high (successive onboard cycles) | 3clk+22 | | ns | 33 |
| 110 | 18 | MASN low to SLVSELN low (MASTENN already low) | clk+11 | 2clk+63 | ns | 33 |
| **DMAC-Type operation** | | | | | | |
| 118 | 20 | LBRN low to BRN low (if BBSYN released) | clk+15 | 2clk+76 | ns | |
| 119 | | LBRN low to LBGN low | clk+18 | 2clk+69 | ns | 36 |
| 120 | 20 | BGINN low to LBGN low (ASN high) | clk+18 | 2clk+69 | ns | |
| | | BGINN low to LBGN low (ASN low) | 2clk+18 | 3clk+69 | ns | |
| 121 | 20 | MASN low (output) to LBGN low | clk+38 | | ns | |
| 123 | 20 | LBRN high to LBGN high | clk+10 | 2clk+69 | ns | 37 |
| 124 | 14, 15 | LBRN high to BBSYN high | clk+12 | 2clk+56 | ns | 24 |
| 125 | 20 | ASN high to LBGN high (selected) | 2clk+15 | 3clk+71 | ns | 37 |
| 126 | 20 | DSI low to LBGN high (selected) | 2clk+15 | 3clk+76 | ns | 37 |

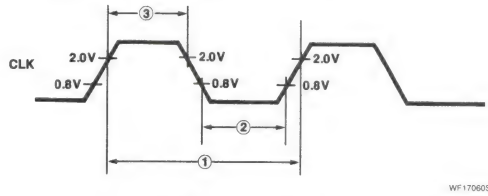



Figure 8.5 CLK Timing

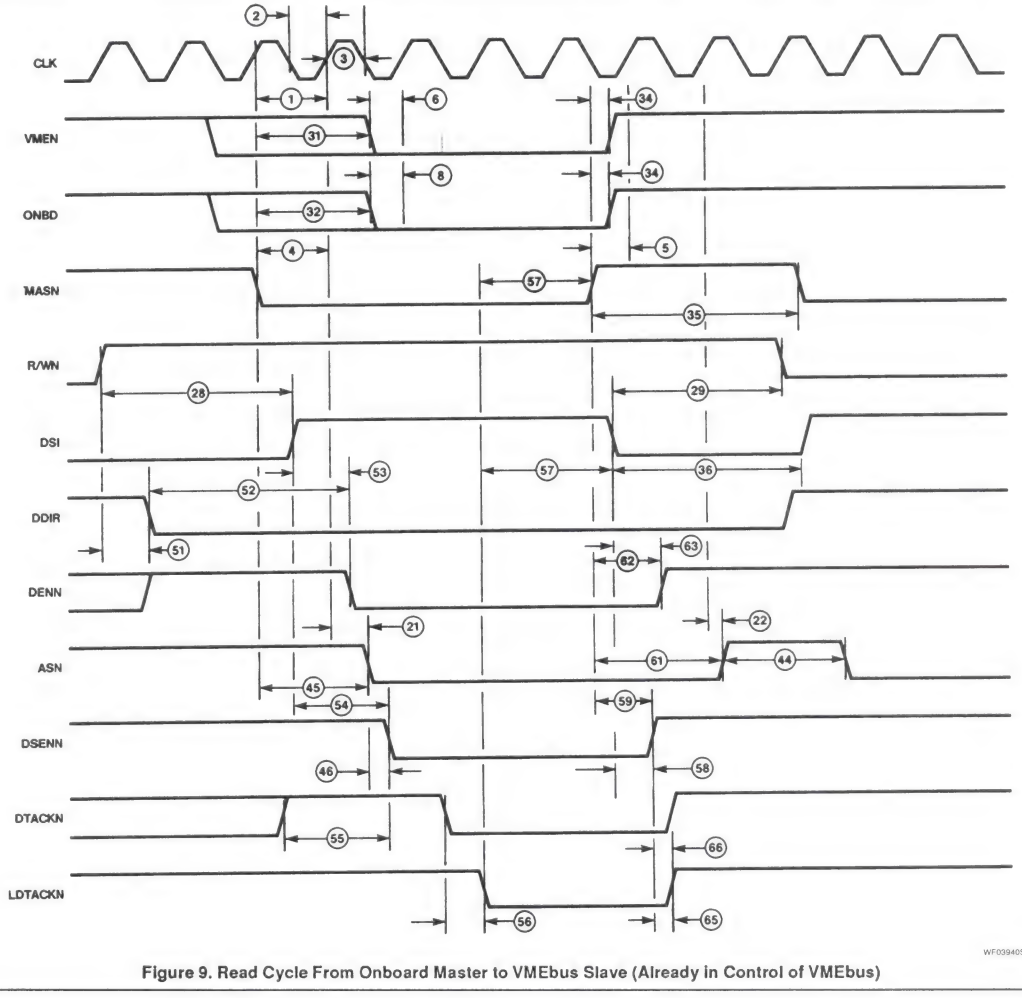



Figure 9. Read Cycle From Onboard Master to VMEbus Slave (Already in Control of VMEbus)

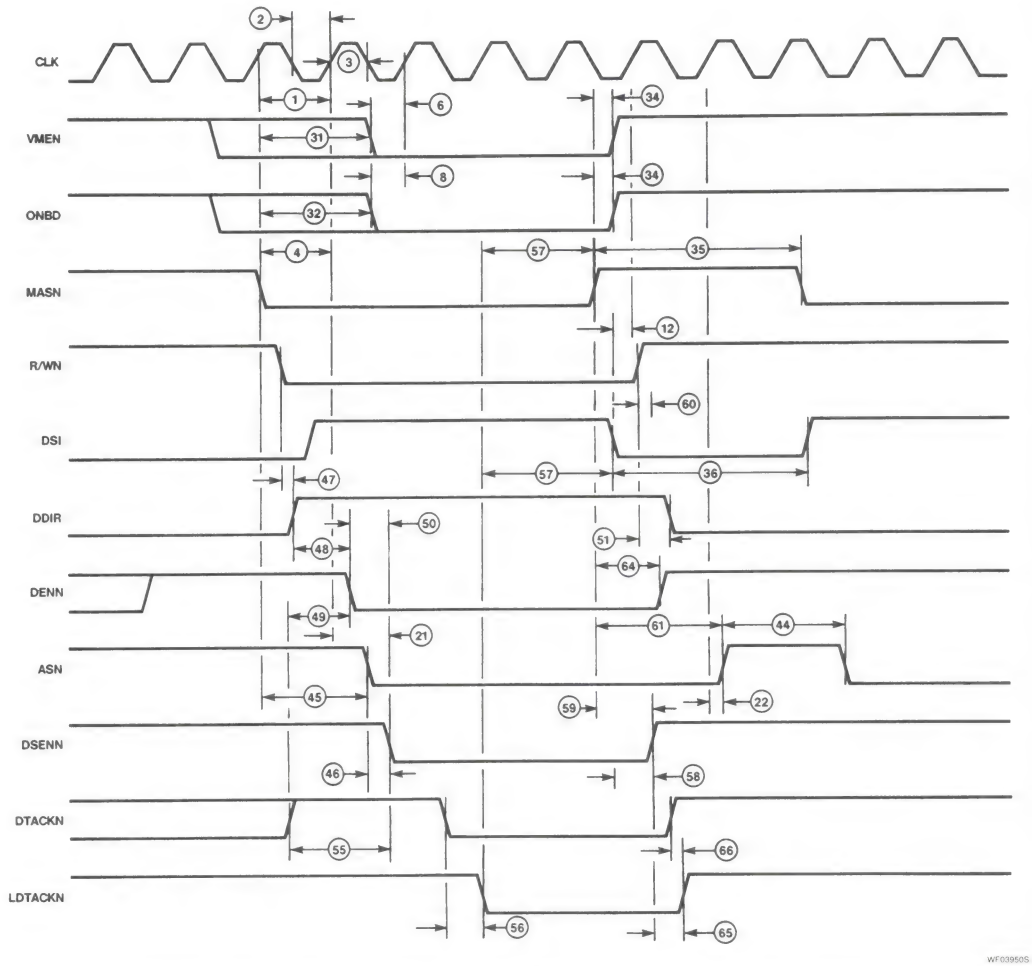



Figure 10. Write Cycle From Onboard Master to VMEbus Slave (Already in Control of VMEbus)

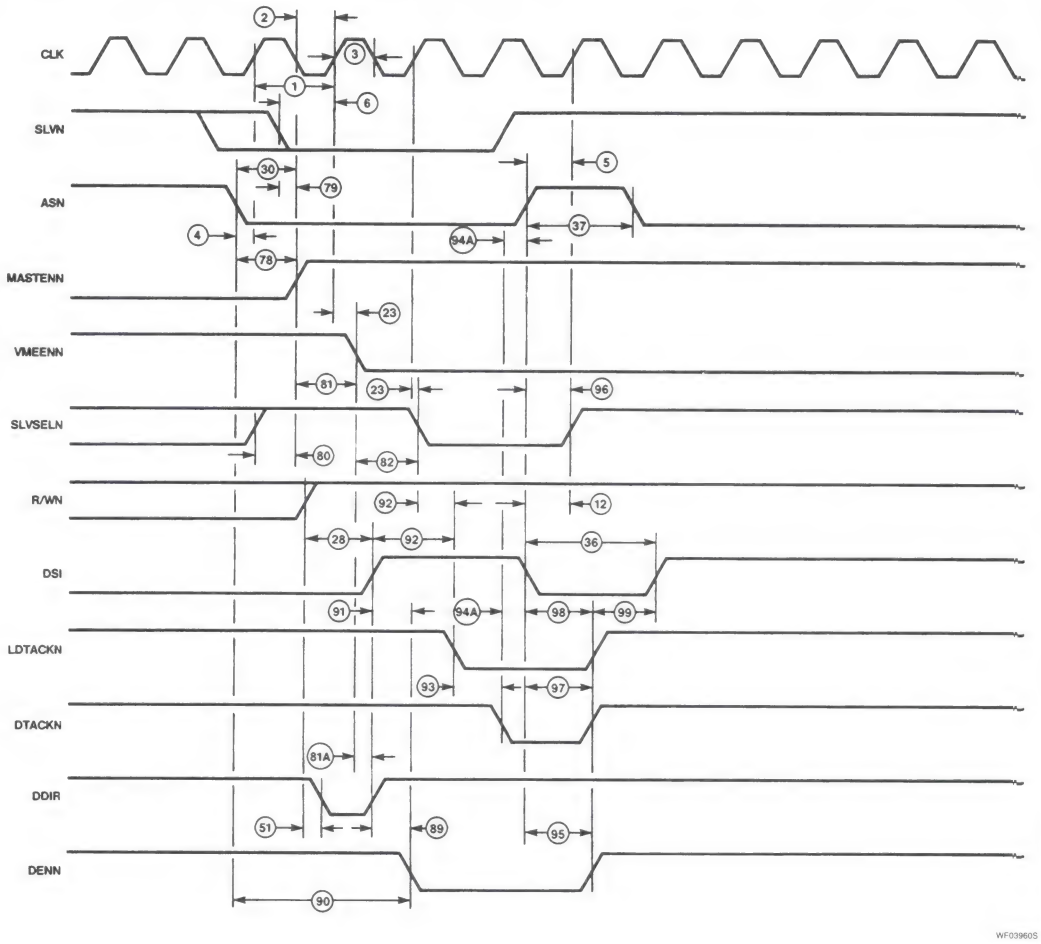



Figure 11. Slave Read Cycle (Starting in Master Mode)

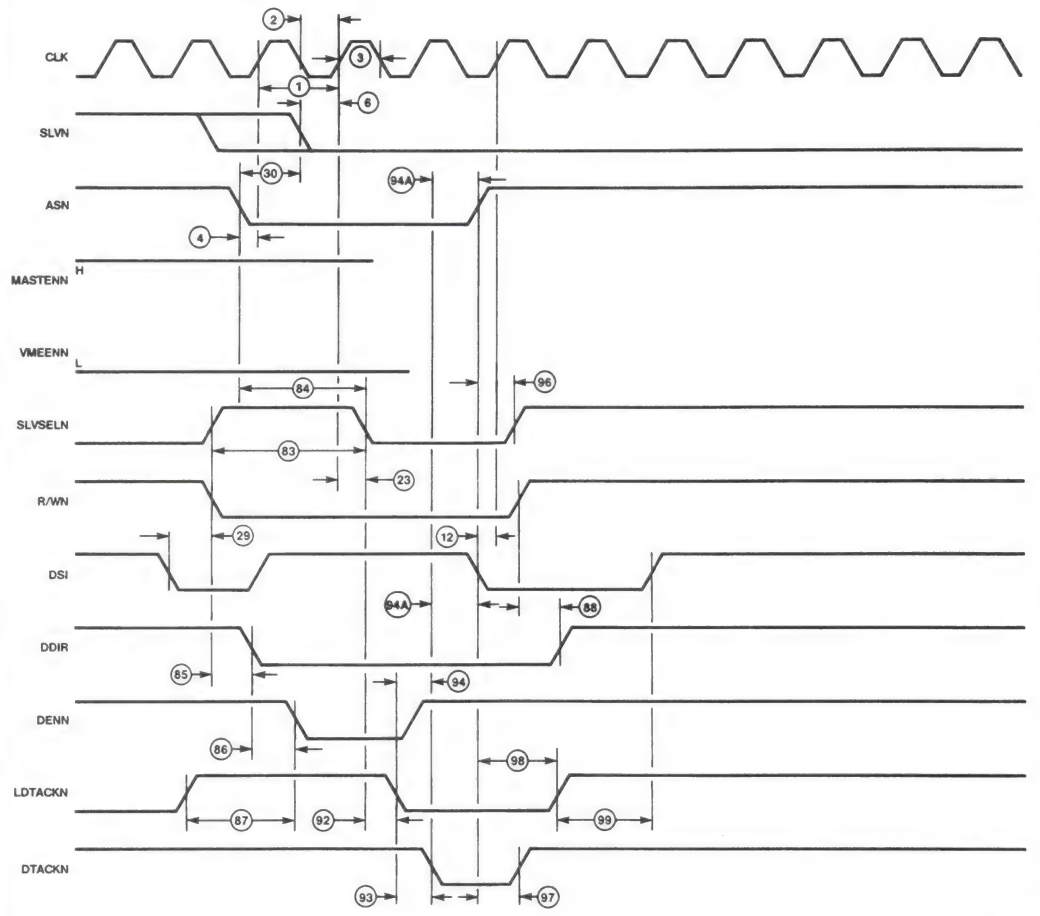



Figure 12. Slave Write Cycle (Starting in Slave Mode)

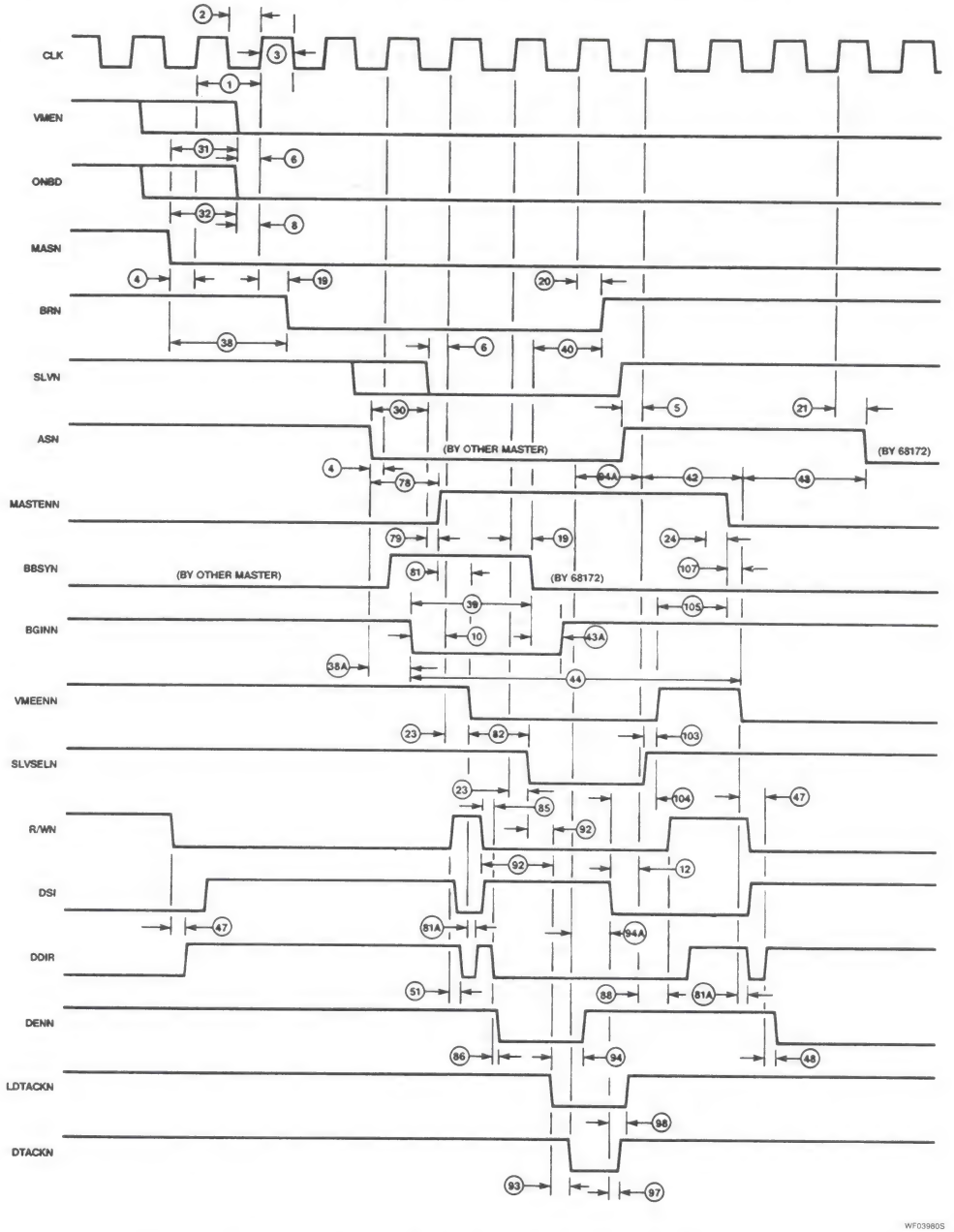



Figure 13. VMEbus Acquisition, Including Slave Write Cycle

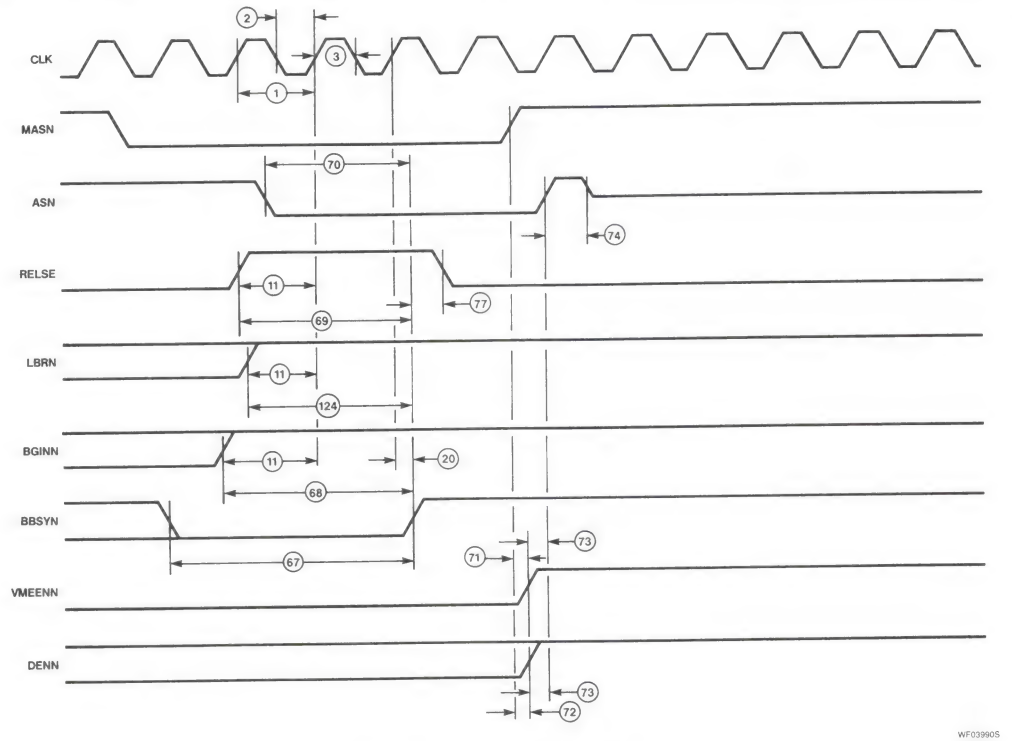



Figure 14. "Early" VMEbus Release

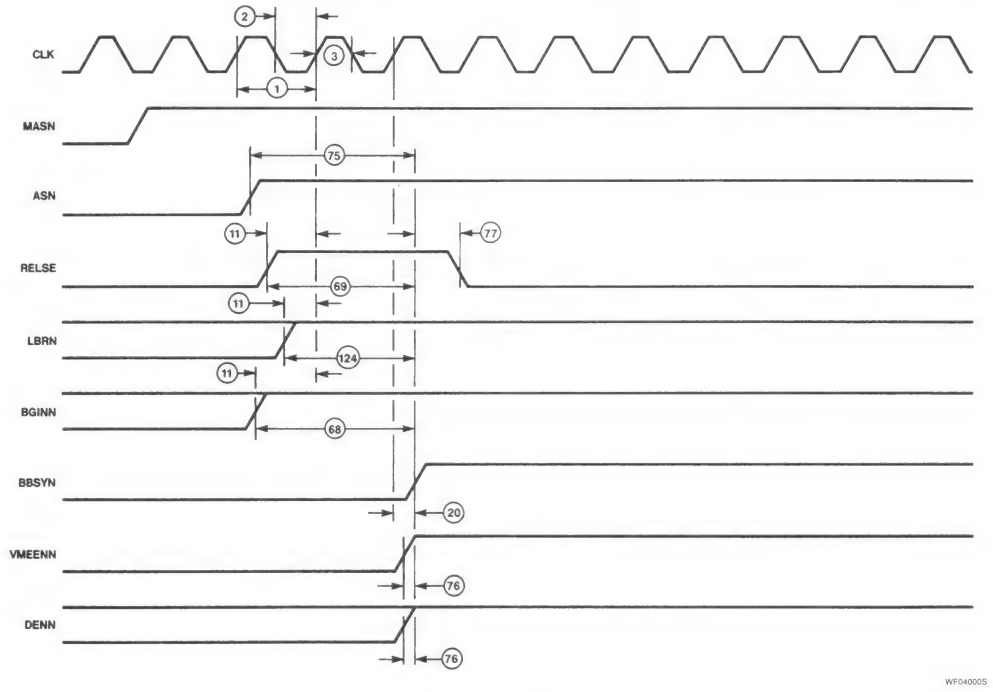



Figure 15. Intercycle VMEbus Release

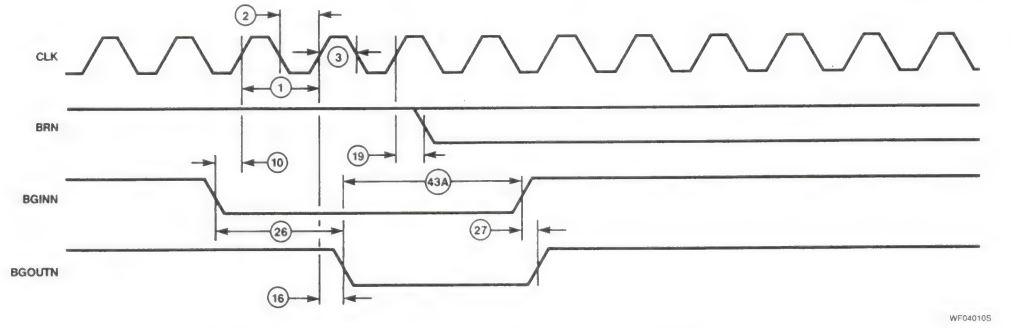



Figure 16. Passing a Bus Grant, Including Earliest Possible Bus Request Thereafter

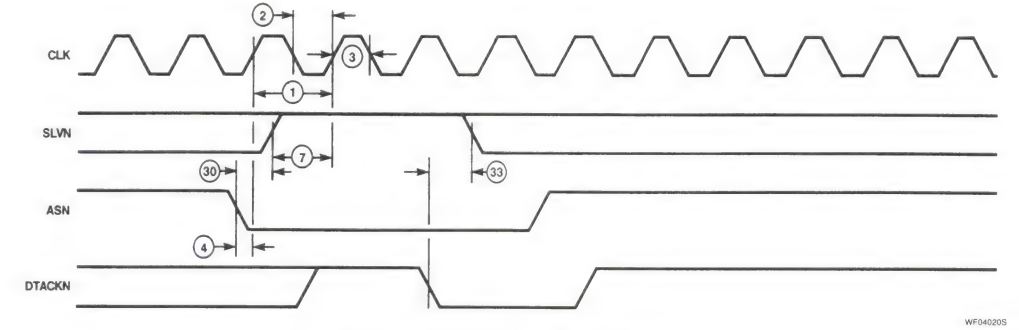



Figure 17. Non-selecting Cycle on VMEbus

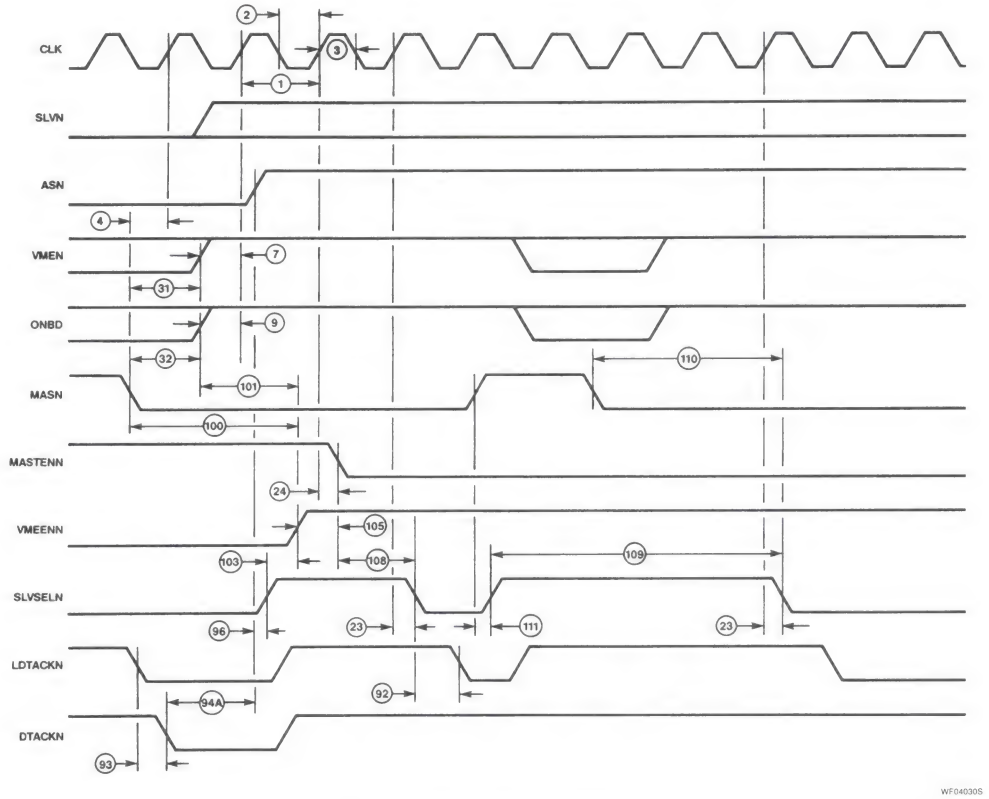



Figure 18. Two Onboard Cycles Following a Slave Cycle

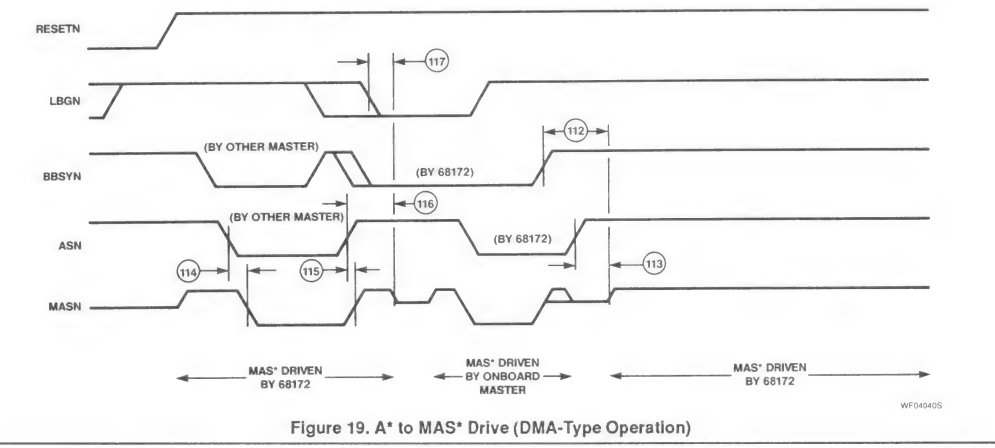



Figure 19. A* to MAS* Drive (DMA-Type Operation)

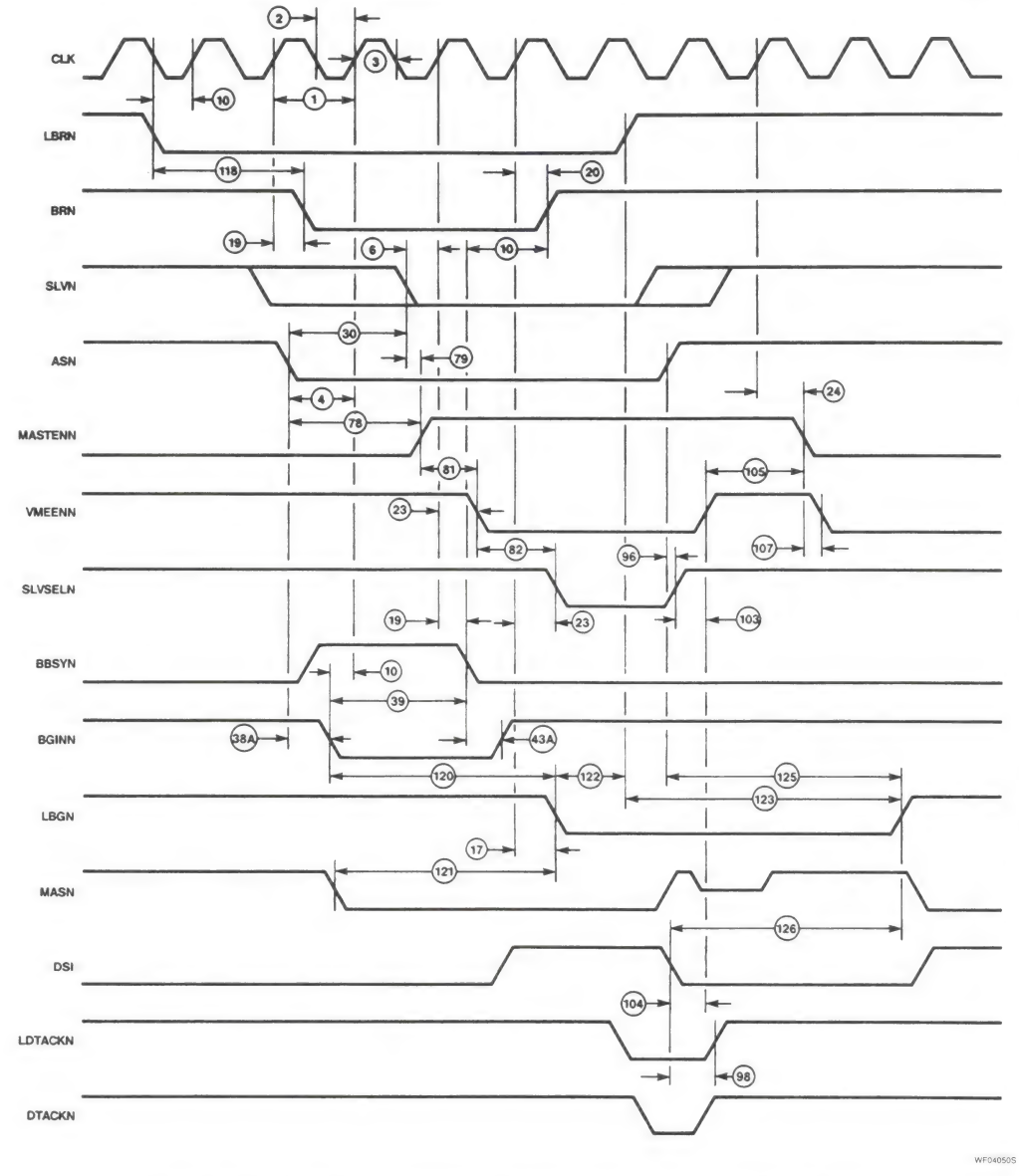



Figure 20. DMA-Type VMEbus Acquisition, With Slave Cycle From Another VMEbus Master

Signetics

# 80C31BH/80C51BH
## CMOS Single-Chip 8-Bit Microcontroller

*Product Specification*

**Military Microprocessor Products**

### DESCRIPTION

The Signetics 80C31BH/80C51BH is a high-performance microcontroller fabricated with Signetics high-density CMOS technology. The CMOS 80C31BH/80C51BH is functionally compatible with the NMOS 8031/8051 microcontroller. The Signetics CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Signetics epitaxial substrate minimizes latch-up sensitivity.

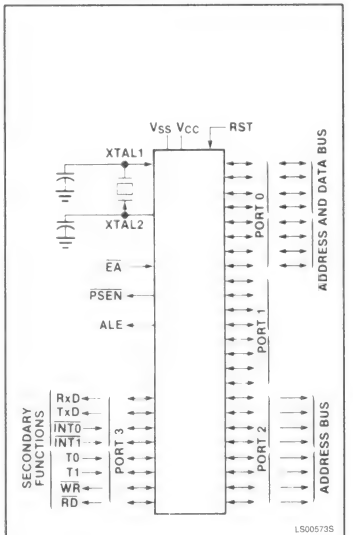
The 80C31BH/80C51BH contains a 4K x 8 ROM; a 128 x 8 RAM; 32 I/O lines; two 16-bit counter/timers; a five-source, two-priority level nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full duplex UART; an on-chip oscillator and clock circuits. In addition, the 80C31BH/80C51BH has two software selectable modes of reduction; idle mode and power-down mode.

The idle mode freezes the CPU while allowing the RAM, timer, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip function to be inoperative.

### FEATURES

- **80C31BH microcontroller without ROM**
- **80C51BH control-oriented microcontroller**
- **8031/8051 compatible**
  - **4K x 8 ROM**
  - **128 x 8 RAM**
  - **Two 16-bit counter/timers**
  - **Boolean processor**
  - **Full duplex serial channel**
- **Memory addressing capability**
  - **64K ROM and 64K RAM**
- **Power control modes:**
  - **Idle mode**
  - **Power-down mode**
- **CMOS and TTL compatible**

### LOGIC SYMBOL



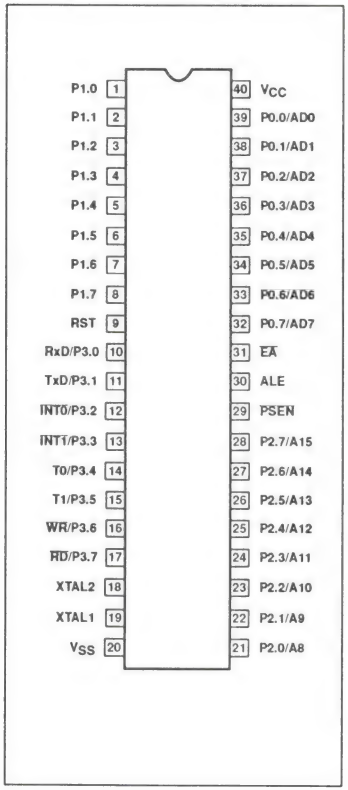

NOTE:
C1, C2 = 30pF ± 10pF for crystals
C1, C2 = 40pF ± 10pF for ceramic resonators

### ORDERING INFORMATION

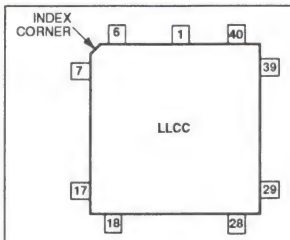
| PACKAGES | INTERNAL ROM | EXTERNAL ROM |
|---|---|---|
| 44 Pin LLCC | 80C51BH*/BUA | 80C31BH/BUA |
| 40 Pin Dual In–Line Package | 80C51BH*/BQA | 80C31BH/BQA |
| 52 Pin Flat Package | 80C51BH*/BYA | 80C31BH/BYA |

* Factory will assign unique CVXXXX part number

## CERDIP PIN CONFIGURATION

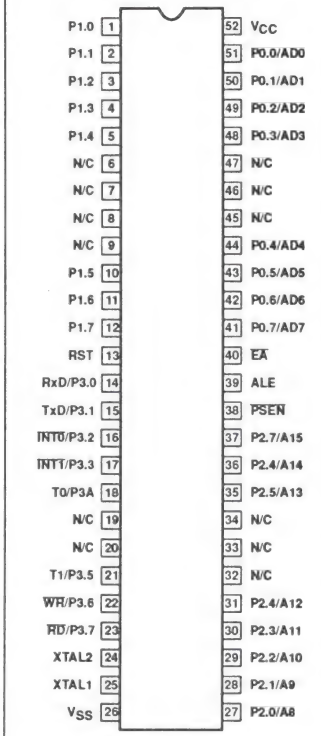



## LLCC PIN CONFIGURATION

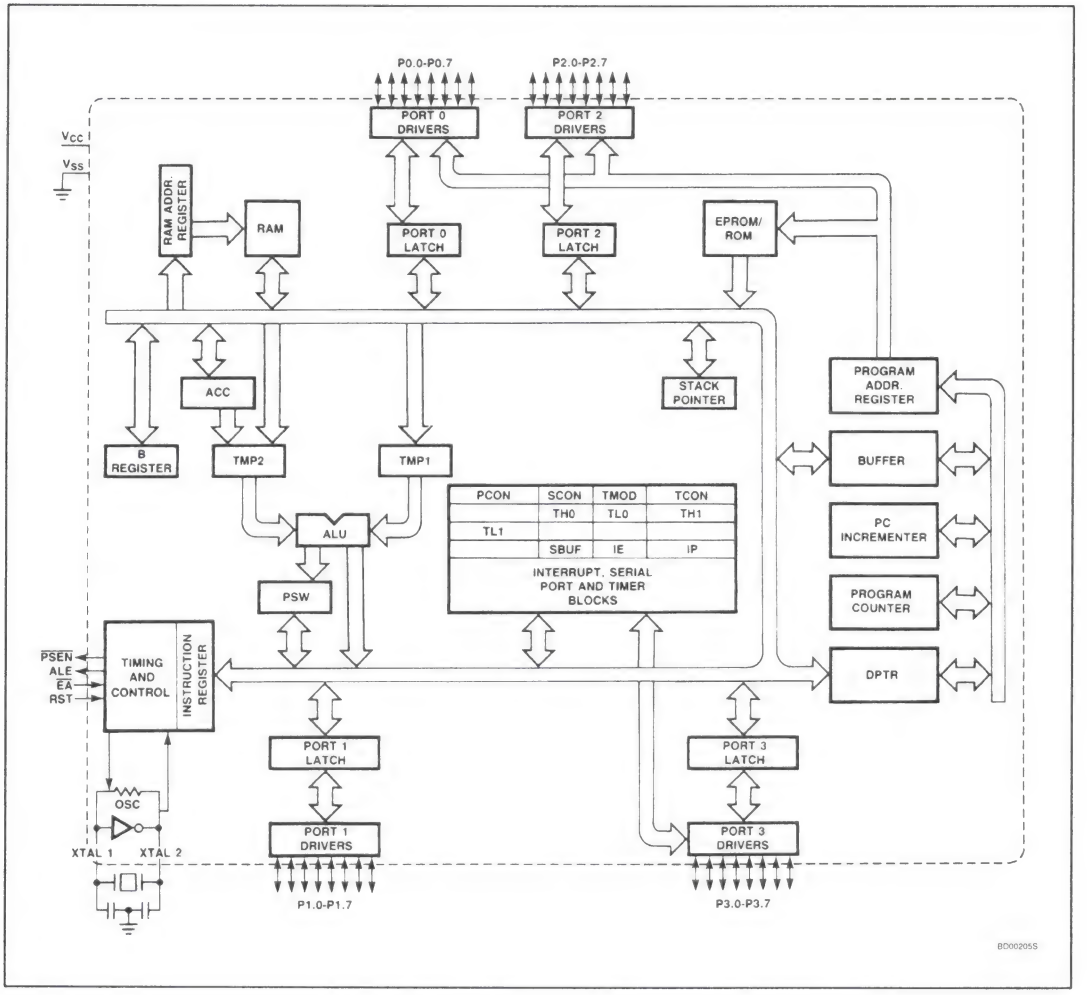



| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | P1.0 | 24 | A8/P2.0 |
| 3 | P1.1 | 25 | A9/P2.1 |
| 4 | P1.2 | 26 | A10/P2.2 |
| 5 | P1.3 | 27 | A11/P2.3 |
| 6 | P1.4 | 28 | A12/P2.4 |
| 7 | P1.5 | 29 | A13/P2.5 |
| 8 | P1.6 | 30 | A14/P2.6 |
| 9 | P1.7 | 31 | A15/P2.7 |
| 10 | RST | 32 | PSEN |
| 11 | RxD/P3.0 | 33 | ALE |
| 12 | N/C | 34 | N/C |
| 13 | TxD/P3.1 | 35 | EA |
| 14 | INT0/P3.2 | 36 | P0.7/AD7 |
| 15 | INT1/P3.3 | 37 | P0.6/AD6 |
| 16 | T0/P3.4 | 38 | P0.5/AD5 |
| 17 | T1/P3.5 | 39 | P0.4/AD4 |
| 18 | WR/P3.6 | 40 | P0.3/AD3 |
| 19 | RD/P3.7 | 41 | P0.2/AD2 |
| 20 | XTAL2 | 42 | P0.1/AD1 |
| 21 | XTAL1 | 43 | P0.0/AD0 |
| 22 | VSS | 44 | VCC |

## FLAT PACK PIN CONFIGURATION



## BLOCK DIAGRAM



## PIN DESCRIPTION

| SYMBOL | PIN NUMBER | | | NAME AND FUNCTION | TYPE |
|---|---|---|---|---|---|
| | DIP | LLCC | FLAT | | |
| $V_{SS}$ | 20 | 22 | 26 | Circuit ground potential. | I |
| $V_{CC}$ | 40 | 44 | 52 | Supply voltage during normal, idle, and power-down operation. | I |
| P0.0-P0.7 | 39-32 | 43-36 | 51-48<br>44-41 | **Port 0:** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 80C51B.<br>External pull-ups are required during program verification. | I/O |
| P1.0-P1.7 | 1-8 | 2-9 | 1-5<br>10-12 | **Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1/s written to them are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled Low will source current because of the internal pull-ups. (See DC Electrical Characteristic: $I_{IL}$) Port 1 also receives Low-order address bytes during program verification. | I/O |
| P2.0-P2.7 | 21-18 | 24-31 | 27-31<br>35-37 | **Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled Low will source current because of the internal pull-ups. (See DC electrical Characteristic: $I_{IL}$) Port 2 emits the High-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application it uses strong internal pull-ups when emitting 1's. During accesses to external data memory that use 8-bit addresses (MOVX@Ri), Port 2 emits the contents of the P2 special function register. | I/O |
| P3.0-P3.7 | 10-17 | 11,<br>13-19 | 14-18<br>21-23 | **Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled Low will source current because of the pull-ups. (See DC Electrical Characteristic: $I_{IL}$) Port 3 also serves the special feature functions of the SC80C51 family, as listed below: | |
| | 10 | 11 | 14 | RxD (P3.0): Serial input port | I |
| | 11 | 13 | 15 | TxD (P3.1): Serial output port | O |
| | 12 | 14 | 16 | $\overline{INT0}$ (P3.2): External interrupt | I |
| | 13 | 15 | 17 | $\overline{INT1}$ (P3.3): External interrupt | I |
| | 14 | 16 | 18 | T0 (P3.4): Timer 0 external input | I |
| | 15 | 17 | 21 | T1 (P3.5): Timer 1 external input | I |
| | 16 | 18 | 22 | $\overline{WR}$ (P3.6): External data memory write strobe | O |
| | 17 | 19 | 23 | $\overline{RD}$ (P3.7): External data memory read strobe | O |
| RST | 9 | 10 | 13 | **Reset:** A High on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC}$. | I |
| ALE | 30 | 33 | 39 | **Address Latch Enable:** Output pulse for latching the Low byte of the address during an access to external memory. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. | O |
| $\overline{PSEN}$ | 29 | 32 | 38 | **Program Store Enable:** The read strobe to external program memory. When the 80C51B is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. | O |
| $\overline{EA}$ | 31 | 35 | 40 | **External Access Enable:** $\overline{EA}$ must be externally held Low to enable the device to fetch code from external program memory locations 0000H to 0FFFH. If $\overline{EA}$ is held High, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH. | I |
| XTAL1 | 19 | 21 | 25 | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. | I |
| XTAL2 | 18 | 20 | 24 | **Crystal 2:** Output from the inverting oscillator amplifier. | O |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Operating temperature range | -55 to +125 | °C |
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |
| $V_{CC}$ | Voltage from $V_{CC}$ to $V_{SS}$[2] | -0.5 to +6.5 | V |
| $V_I$, $V_O$ | Voltage from any pin to $V_{SS}$[2] | -0.5 to $V_{CC}$ +0.5 | V |
| $P_{MAX}$ | Power dissipation | 200 | mW |

## MAXIMUM $I_{CC}$ (mA)

| FREQUENCY | OPERATING[7] | | | IDLE[8] | | |
|---|---|---|---|---|---|---|
| $V_{CC}$ | 4V | 5V | 6V | 4V | 5V | 6V |
| 3.5MHz | 4.3 | 5.7[10] | 7.5 | 1.1 | 1.6[10] | 2.2 |
| 8MHz[10] | 8.3 | 11 | 14 | 1.8 | 2.7 | 3.7 |
| 12MHz | 12 | 16[10] | 20 | 2.5 | 3.7[10] | 5.0 |

## DC ELECTRICAL CHARACTERISTICS -55°C ≤ $T_A$ ≤ +125°C, 4.0V ≤ $V_{CC}$ ≤ 6.0V, $V_{SS}$ = OV[3]

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IL}$ | Input Low voltage, except $\overline{EA}$ | | -0.5 | 0.2 $V_{CC}$ - 0.25 | V |
| $V_{IL1}$ | Input Low voltage, $\overline{EA}$ | | -0.5 | 0.2 $V_{CC}$ - 0.45 | V |
| $V_{IH}$ | Input High voltage, except XTAL1, RST | | 0.2 $V_{CC}$ +.1 | $V_{CC}$ +0.5 | V |
| $V_{IH1}$ | Input High voltage, XTAL1, RST | | 0.7 $V_{CC}$ + 0.2 | $V_{CC}$ +.05 | V |
| $V_{OL}$ | Output Low voltage, ports 1,2 & 3[4] | $I_{OL}$ = 1.6mA | | 0.45 | V |
| $V_{OL1}$ | Output Low voltage, port 0, ALE, $\overline{PSEN}$[4] | $I_{OL}$ = 3.2mA | | 0.45 | V |
| $V_{OH}$ | Output High voltage, ports 1, 2 & 3 | $I_{OH}$ = -60µA, $V_{CC}$ = 5V +/-10% | 2.4 | | V |
| | | $I_{OH}$ = -25µA, $V_{CC}$ = 5V +/-10% | 0.75$V_{CC}$ | | V |
| | | $I_{OH}$ = -10µA, $V_{CC}$ = 5V +/-10% | 0.9$V_{CC}$ | | |
| $V_{OH1}$ | Output High voltage, port 0 in external bus mode, ALE, $\overline{PSEN}$ | $I_{OH}$ = -400µA, $V_{CC}$ = 5V +/-10% | 2.4 | | V |
| | | $I_{OH}$ = -150µA, $V_{CC}$ = 5V +/-10% | 0.75$V_{CC}$ | | V |
| | | $I_{OH}$ = -40µA, $V_{CC}$ = 5V +/-10% | 0.9$V_{CC}$ | | V |
| $I_{IL}$ | Logical 0 input current, ports 1,2 & 3 | $V_{IN}$ = 0.45V | | -75 | µA |
| $I_{TL}$ | Logical 1 to 0 transition current, ports 1,2 & 3 | $V_{IN}$ = 2V | | -750 | µA |
| $I_{LI}$ | Input leakage, current port 0, $\overline{EA}$ | 0.45V < $V_{IN}$ < $V_{CC}$ | | +/-10 | µA |
| $R_{RST}$ | Reset pulldown resistor | | 50 | 150 | kΩ |
| $C_{IO}$[9] | Pin capacitance | Test freq= 1MHz, $T_A$ = 25°C | | 10 | pF |
| $I_{PD}$ | Power-down current[6] | $V_{CC}$ = 2V to 6V | | 75 | µA |

## AC SYMBOL DESIGNATIONS

Each timing symbol has five characters. The first character is always a "t" (t = time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A = Address
C = Clock
D = Input data
H = Logic level High
I = Instruction (Program Memory Contents)
L = Logic level Low or ALE
P = $\overline{PSEN}$
Q = Output data
R = $\overline{READ}$ signal
T = Time
V = Valid
W = $\overline{WRITE}$ signal
X = No longer a valid logic level
Z = Float

**Example:**

$t_{AVLL}$ = Time for address valid to ALE Low.
$t_{LLPL}$ = Time for ALE Low to $\overline{PSEN}$ Low.

## AC ELECTRICAL CHARACTERISTICS

$-55°C \le T_A \le +125°C$, $V_{CC} = 5V +/-20\%$, $V_{SS} = 0V$, load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80 pF.

| SYMBOL | PARAMETER | VARIABLE CLOCK | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| | **Program Memory (Figure 1)** | | | |
| $1/t_{CLCL}$ | Oscillator frequency, 80C31BH/80C51BH | 3.5 | 12 | MHz |
| $t_{LHLL}$ | ALE pulse width | $2t_{CLCL}-55$ | | ns |
| $t_{AVLL}$ | Address valid to ALE Low | $t_{CLCL}-70$ | | ns |
| $t_{LLAX}$ | Address hold after ALE Low | $t_{CLCL}-50$ | | ns |
| $t_{LLIV}$ | ALE Low to valid instr in | | $4t_{CLCL}-115$ | ns |
| $t_{LLPL}$ | ALE Low to $\overline{PSEN}$ Low | $t_{CLCL}-55$ | | ns |
| $t_{PLPH}$ | $\overline{PSEN}$ pulse width | $3t_{CLCL}-60$ | | ns |
| $t_{PLIV}$ | $\overline{PSEN}$ Low to valid instr in | | $3t_{CLCL}-120$ | ns |
| $t_{PXIX}$ | Input instr hold after $\overline{PSEN}$ | 0 | | ns |
| $t_{PXIZ}$ | Input instr float after $\overline{PSEN}$ | | $t_{CLCL}-40$ | ns |
| $t_{AVIV}$ | Address to valid instr in | | $5t_{CLCL}-120$ | ns |
| $t_{PLAZ}$ | $\overline{PSEN}$ Low to address float | | 25 | ns |
| | **External Data Memory (Figures 2 & 3)** | | | |
| $t_{RLRH}$ | $\overline{RD}$ pulse width | $6t_{CLCL}-100$ | | ns |
| $t_{WLWH}$ | $\overline{WR}$ pulse width | $6t_{CLCL}-100$ | | ns |
| $t_{RLDV}$ | $\overline{RD}$ Low to valid data in | | $5t_{CLCL}-185$ | ns |
| $t_{RHDX}$ | Data hold after $\overline{RD}$ | 0 | | ns |
| $t_{RHDZ}$ | Data float after $\overline{RD}$ | | $2t_{CLCL}-85$ | ns |
| $t_{LLDV}$ | ALE Low to valid data in | | $8t_{CLCL}-170$ | ns |
| $t_{AVDV}$ | Address to valid data in | | $9t_{CLCL}-185$ | ns |
| $t_{LLWL}$ | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | $3t_{CLCL}-65$ | $3t_{CLCL}+65$ | ns |
| $t_{AVWL}$ | Address valid to $\overline{WR}$ Low | $4t_{CLCL}-145$ | | ns |
| $t_{QVWX}$ | Data valid to $\overline{WR}$ transition | $t_{CLCL}-75$ | | ns |
| $t_{WHQX}$ | Data hold after $\overline{WR}$ | $t_{CLCL}-65$ | | ns |
| $t_{RLAZ}$ | $\overline{RD}$ Low to address float | | 0 | ns |
| $t_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE High | $t_{CLCL}-65$ | $t_{CLCL}+65$ | ns |
| | **External Clock (Figure 4)** | | | |
| $t_{CHCX}$ | High time | 20 | | ns |
| $t_{CLCX}$ | Low time | 20 | | ns |
| $t_{CLCH}$ | Rise time | | 20 | ns |
| $t_{CHCL}$ | Fall time | | 20 | ns |
| | **Serial Port Timing/Shift Register Mode (Figure 5)** | | | |
| $t_{XLXL}$[10] | Serial port clock cycle time | $12t_{CLCL}$ | | µs |
| $t_{QVXH}$[10] | Output data setup to clock rising edge | $10t_{CLCL}-133$ | | ns |
| $t_{XHQX}$[10] | Output data hold after clock rising edge | $2t_{CLCL}-117$ | | ns |
| $t_{XHDX}$[10] | Input data hold after clock rising edge | 0 | | ns |
| $t_{XHDV}$[10] | Clock rising edge to input data valid | | $10t_{CLCL}-133$ | ns |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified.
4. Capacitive loading on ports 0 and 2 can cause spurious noise pulses to be superimposed on the $V_{OLS}$ of ALE and ports 1 and 3. The noise is caused by external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE line can exceed 0.8V. In such cases it could be desirable to qualify ALE with a Schmitt trigger, or to use an address latch with a Schmitt trigger STROBE input.
5. Capacitive loading on ports 0 and 2 can cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall before the 0.9 $V_{CC}$ specification when the address bits are stabilizing.
6. Power-down $I_{CC}$ is measured with all output pins disconnected; $\overline{EA}$ = port 0 = $V_{CC}$; XTAL2 N.D.; RST = $V_{SS}$.
7. $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL}$ = $V_{SS}$ + .5V, $V_{IH}$ = $V_{CC}$ -.5V; XTAL2 N.C.; $\overline{EA}$ = RST = port 0 = $V_{CC}$. $I_{CC}$ will be slightly higher if a crystal oscillator is used.
8. Idle $I_{CC}$ is measured with all output pins disconnected: XTAL1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL}$ = $V_{SS}$ + 5.V, $V_{IH}$ = $V_{CC}$ – .5V; XTAL2 N.C.; port 0 = $V_{CC}$; $\overline{EA}$ = RST = $V_{SS}$.
9. $C_{IO}$ is tested initially and after any design or process change which may effect capacitance.
10. Parameter is guaranteed but not tested.

## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in the logic symbol on Page 1.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop; however, minimum and maximum High and Low times specified in the data sheet must be observed.

## DESIGN CONSIDERATIONS

At power-on, the voltage on $V_{CC}$ and RST must come up at the same time for a proper start-up.

Before entering the power-down mode, the contents of the carry bit and B.7 must be equal. (See Table 1.)

## IDLE MODE

In the idle mode, the CPU puts itself to sleep while all the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

## POWER-DOWN MODE

In the power-down mode the oscillator is stopped, and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduces power modes are in the special function register PCON.

**Table 2. External Pin Status During Idle and Power-Down Modes**

| MODE | PROGRAM MEMORY | ALE | $\overline{PSEN}$ | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power-down | External | 0 | 0 | Float | Data | Data | Data |

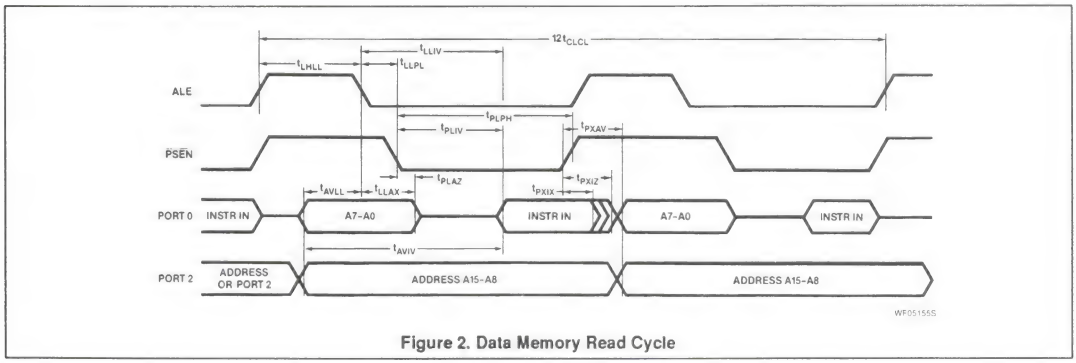



**Figure 2. Data Memory Read Cycle**

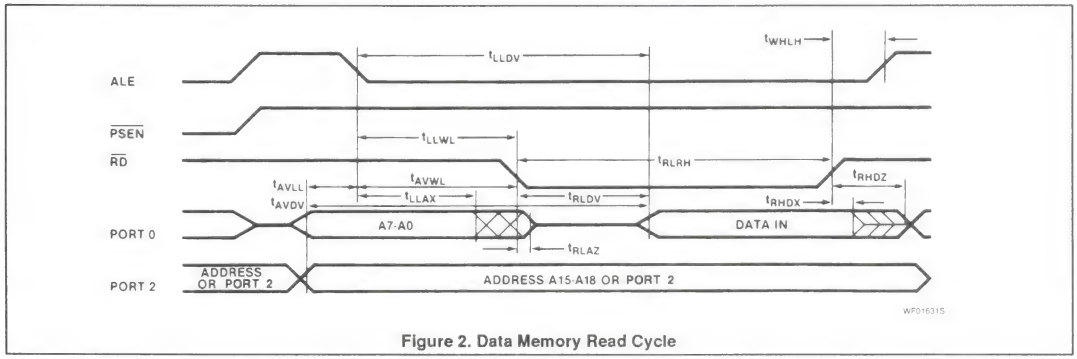



**Figure 2. Data Memory Read Cycle**

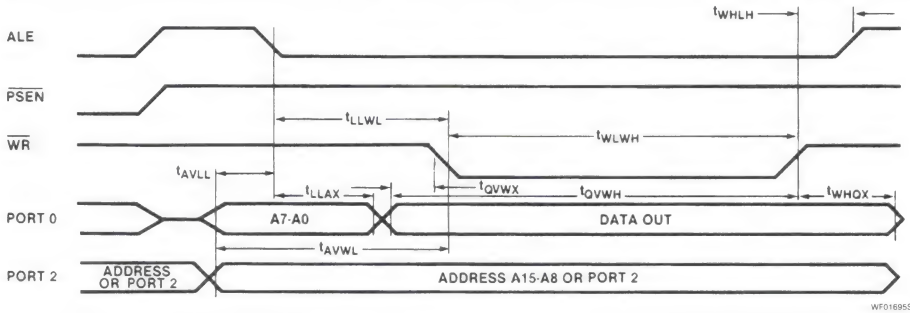



**Figure 3. Data Memory Write Cycle**

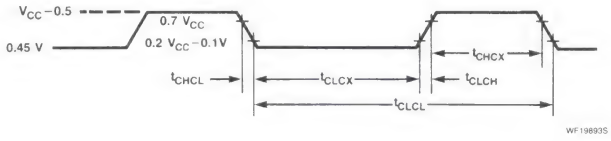



**Figure 4. External Clock Drive Waveform**

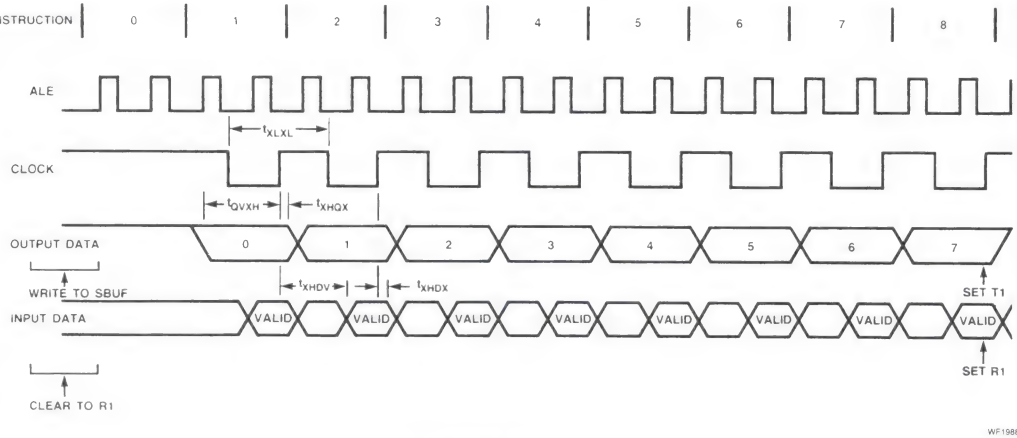
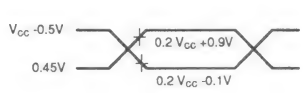



**Figure 5. Shift Register Mode Timing Waveforms**




**NOTE:**
AC inputs during testing are driven at $V_{CC}$ -0.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at $V_{IH}$ min. for a logic "1" and $V_{IL}$ max. for a logic "0."

**Figure 6. AC Testing Input, Output Waveforms**

**NOTE:**
For timing purposes a port pin is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OL}/I_{OH} > \pm 20$mA.

**Figure 7. Float Waveforms**

## Table 3. Instruction Set

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Arithmetic operations** | | | | |
| ADD | A,Rn | Add register to accumulator | 1 | 1 |
| ADD | A,direct | Add direct byte to accumulator | 2 | 1 |
| ADD | A,@Ri | Add indirect RAM to accumulator | 1 | 1 |
| ADD | A,R#data | Add immediate data to accumulator | 2 | 1 |
| ADDC | A,Rn | Add register to accumulator with carry | 1 | 1 |
| ADDC | A,direct | Add direct byte to A with carry flag | 2 | 1 |
| ADDC | A,@Ri | Add indirect RAM to A with carry flag | 1 | 1 |
| ADDC | A,#data | Add immediate data to A with carry flag | 2 | 1 |
| SUBB | A,Rn | Subtract register from A with borrow | 1 | 1 |
| SUBB | A,direct | Subtract direct byte from A with borrow | 2 | 1 |
| SUBB | A,@Ri | Subtract indirect RAM from A w/borrow | 1 | 1 |
| SUBB | A,#data | Subtract immed. data from A w/borrow | 2 | 1 |
| INC | A | Increment accumulator | 1 | 1 |
| INC | Rn | Increment register | 1 | 1 |
| INC | direct | Increment direct byte | 2 | 1 |
| INC | @Ri | Increment indirect RAM | 1 | 1 |
| DEC | A | Decrement accumulator | 1 | 1 |
| DEC | Rn | Decrement register | 1 | 1 |
| DEC | direct | Decrement direct byte | 2 | 1 |
| DEC | @Ri | Decrement indirect RAM | 1 | 1 |
| INC | DPTR | Increment data pointer | 1 | 2 |
| MUL | AB | Multiply A & B | 1 | 4 |
| DIV | AB | Divide A by B | 1 | 4 |
| DA | A | Decimal adjust accumulator | 1 | 1 |

**Table 2. Instruction Set** (Continued)

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Logical operations** | | | | |
| ANL | A,Rn | AND register to accumulator | 1 | 1 |
| ANL | A,direct | AND direct byte to accumulator | 2 | 1 |
| ANL | A,@Ri | AND indirect RAM to accumulator | 1 | 1 |
| ANL | A,#data | AND immediate data to accumulator | 2 | 1 |
| ANL | direct,A | AND accumulator to direct byte | 2 | 1 |
| ANL | direct,#data | AND immediate data to direct byte | 3 | 2 |
| ORL | A,Rn | OR register to accumulator | 1 | 1 |
| ORL | A,direct | OR direct byte to accumulator | 2 | 1 |
| ORL | A,@Ri | OR indirect RAM to accumulator | 1 | 1 |
| ORL | A,#data | OR immediate data to accumulator | 2 | 1 |
| ORL | direct,A | OR accumulator to direct byte | 2 | 1 |
| ORL | direct,#data | OR immediate data to direct byte | 3 | 2 |
| XRL | A,Rn | Exclusive-OR register to accumulator | 1 | 1 |
| XRL | A,direct | Exclusive-OR direct byte to accumulator | 2 | 1 |
| XRL | A,@Ri | Exclusive-OR indirect RAM to A | 1 | 1 |
| XRL | A,#data | Exclusive-OR immediate data to A | 2 | 1 |
| XRL | direct,A | Exclusive-OR accumulator to direct byte | 2 | 1 |
| XRL | direct,#data | Exclusive-OR immediate data to direct | 3 | 2 |
| CLR | A | Clear accumulator | 1 | 1 |
| CPL | A | Complement accumulator | 1 | 1 |
| RL | A | Rotate accumulator left | 1 | 1 |
| RLC | A | Rotate A left through the carry flag | 1 | 1 |
| RR | A | Rotate accumulator right | 1 | 1 |
| RRC | A | Rotate A right through carry flag | 1 | 1 |
| SWAP | A | Swap nibbles within the accumulator | 1 | 1 |
| **Data transfer** | | | | |
| MOV | A,Rn | Move register to accumulator | 1 | 1 |
| MOV | A,direct | Move direct byte to accumulator | 2 | 1 |
| MOV | A,@Ri | Move indirect RAM to accumulator | 1 | 1 |
| MOV | A,#data | Move immediate data to accumulator | 2 | 1 |
| MOV | Rn,A | Move accumulator to register | 1 | 1 |
| MOV | Rn,direct | Move direct byte to register | 2 | 2 |
| MOV | Rn,#data | Move immediate data to register | 2 | 1 |
| MOV | direct,A | Move accumulator to direct byte | 2 | 1 |
| MOV | direct,Rn | Move register to direct byte | 2 | 2 |
| MOV | direct,direct | Move direct byte to direct | 3 | 2 |
| MOV | direct,@Ri | Move indirect RAM to direct byte | 2 | 2 |
| MOV | direct,#data | Move immediate data to direct byte | 3 | 2 |
| MOV | @Ri,A | Move accumulator to indirect RAM | 1 | 1 |
| MOV | @Ri,direct | Move direct byte to indirect RAM | 2 | 2 |
| MOV | @Ri,#data | Move immediate data to indirect RAM | 2 | 1 |
| MOV | DPTR,#data16 | Load data pointer with a 16-bit constant | 3 | 2 |
| MOVC | A,@A + DPTR | Move code byte relative to DPTR to A | 1 | 2 |
| MOVC | A,@A + PC | Move code byte relative to PC to A | 1 | 2 |
| MOVX | A,@Ri | Move external RAM (8-bit addr) to A | 1 | 2 |
| MOVX | A,@DPTR | Move external RAM (16-bit addr) to A | 1 | 2 |
| MOVX | @Ri,A | Move A to external RAM (8-bit addr) | 1 | 2 |
| MOVX | @DPTR,A | Move A to external RAM (16-bit addr) | 1 | 2 |
| PUSH | direct | Push direct byte onto stack | 2 | 2 |
| POP | direct | Pop direct byte from stack | 2 | 2 |
| XCH | A,Rn | Exchange register with accumulator | 1 | 1 |
| XCH | A,direct | Exchange direct byte with accumulator | 2 | 1 |
| XCH | A,@Ri | Exchange indirect RAM with A | 1 | 1 |
| XCHD | A,#Ri | Exchange Low-order digit ind. RAM w/A | 1 | 1 |

**Table 2. Instruction Set** (Continued)

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Boolean variable manipulation** | | | | |
| CLR | C | Clear carry flag | 1 | 1 |
| CLR | bit | Clear direct bit | 2 | 1 |
| SETB | C | Set carry flag | 1 | 1 |
| SETB | bit | Set direct bit | 2 | 1 |
| CPL | C | Complement carry flag | 1 | 1 |
| CPL | bit | Complement direct bit | 2 | 1 |
| ANL | c,bit | AND direct bit to carry flag | 2 | 2 |
| ANL | c,/bit | AND complement of direct bit to carry | 2 | 2 |
| ORL | c,bit | OR direct bit to carry flag | 2 | 2 |
| ORL | c,/bit | OR complement of direct bit to carry | 2 | 2 |
| MOV | C,bit | Move direct bit to carry flag | 2 | 1 |
| MOV | bit,C | Move carry flag to direct bit | 2 | 2 |
| **Program and machine control** | | | | |
| ACALL | addr11 | Absolute subroutine call | 2 | 2 |
| LCALL | addr16 | Long subroutine call | 3 | 2 |
| RET | | Return from subroutine | 1 | 2 |
| RETI | | Return from interrupt | 1 | 2 |
| AJMP | addr11 | Absolute jump | 2 | 2 |
| LJMP | addr16 | Long jump | 3 | 2 |
| SJMP | rel | Short jump (relative addr) | 2 | 2 |
| JMP | @A + DPTR | Jump indirect relative to the DPTR | 1 | 2 |
| JZ | rel | Jump if accumulator is zero | 2 | 2 |
| JNZ | rel | Jump if accumulator is not zero | 2 | 2 |
| JC | rel | Jump if carry flag is set | 2 | 2 |
| JNC | rel | Jump if no carry flag | 2 | 2 |
| JB | bit,rel | Jump if direct bit set | 3 | 2 |
| JNB | bit,rel | Jump if direct bit not set | 3 | 2 |
| JBC | bit,rel | Jump if direct bit is set & clear bit | 3 | 2 |
| CJNE | A,direct,rel | Compare direct to A & jump if not equal | 3 | 2 |
| CJNE | A,#data,rel | Comp. immed. to A & jump if not equal | 3 | 2 |
| CJNE | Rn,#data,rel | Comp. immed. to reg. & jump if not equal | 3 | 2 |
| CJNE | @Ri,#data,rel | Comp. immed. to ind. & jump if not equal | 3 | 2 |
| DJNZ | Rn,rel | Decrement register & jump if not zero | 2 | 2 |
| DJNZ | direct,rel | Decrement direct & jump if not zero | 3 | 2 |
| NOP | | No operation | 1 | 1 |

**Notes on data addressing modes:**

Rn –Working register R0-R7

direct –128 internal RAM locations, any I/O port, control or status register

@Ri –Indirect internal RAM location addressed by register R0 or R1

#data –8-bit constant included in instruction

#data16 –16-bit constant included as bytes 2 & 3 of instruction

bit –128 software flags, any I/O pin, control or status bit

**Notes on program addressing modes:**

addr16 –Destination address for LCALL & LJMP may be anywhere within the 64-kilobyte program memory address space.

addr11 –Destination address for ACALL & AJMP will be within the same 2-kilobyte page of program memory as the first byte of the following instruction.

rel –SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127 – 128 bytes relative to first byte of the following instruction.

**Table 4. Instruction Opcodes in Hexadecimal Order**

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 00 | 1 | NOP | |
| 01 | 2 | AJMP | code addr |
| 02 | 3 | LJMP | code addr |
| 03 | 1 | RR | A |
| 04 | 1 | INC | A |
| 05 | 2 | INC | data addr |
| 06 | 1 | INC | @R0 |
| 07 | 1 | INC | @R1 |
| 08 | 1 | INC | R0 |
| 09 | 1 | INC | R1 |
| 0A | 1 | INC | R2 |
| 0B | 1 | INC | R3 |
| 0C | 1 | INC | R4 |
| 0D | 1 | INC | R5 |
| 0E | 1 | INC | R6 |
| 0F | 1 | INC | R7 |
| 10 | 3 | JBC | bit addr, code addr |
| 11 | 2 | ACALL | code addr |
| 12 | 3 | LCALL | code addr |
| 13 | 1 | RRC | A |
| 14 | 1 | DEC | A |
| 15 | 2 | DEC | data addr |
| 16 | 1 | DEC | @R0 |
| 17 | 1 | DEC | @R1 |
| 18 | 1 | DEC | R0 |
| 19 | 1 | DEC | R1 |
| 1A | 1 | DEC | R2 |
| 1B | 1 | DEC | R3 |
| 1C | 1 | DEC | R4 |
| 1D | 1 | DEC | R5 |
| 1E | 1 | DEC | R6 |
| 1F | 1 | DEC | R7 |
| 20 | 3 | JB | bit addr, code addr |
| 21 | 2 | AJMP | code addr |
| 22 | 1 | RET | |
| 23 | 1 | RL | A |
| 24 | 2 | ADD | A,#data |
| 25 | 2 | ADD | A,data addr |
| 26 | 1 | ADD | A,@R0 |
| 27 | 1 | ADD | A,@R1 |
| 28 | 1 | ADD | A,R0 |
| 29 | 1 | ADD | A,R1 |
| 2A | 1 | ADD | A,R2 |
| 2B | 1 | ADD | A,R3 |
| 2C | 1 | ADD | A,R4 |
| 2D | 1 | ADD | A,R5 |
| 2E | 1 | ADD | A,R6 |
| 2F | 1 | ADD | A,R7 |
| 30 | 3 | JNB | bit addr, code addr |
| 31 | 2 | ACALL | code addr |
| 32 | 1 | RETI | |
| 33 | 1 | RLC | A |
| 34 | 2 | ADDC | A,#data |
| 35 | 2 | ADDC | A,data addr |
| 36 | 1 | ADDC | A,@R0 |
| 37 | 1 | ADDC | A,@R1 |
| 38 | 1 | ADDC | A,R0 |
| 39 | 1 | ADDC | A,R1 |
| 3A | 1 | ADDC | A,R2, |
| 3B | 1 | ADDC | A,R3 |
| 3C | 1 | ADDC | A,R4 |
| 3D | 1 | ADDC | A,R5 |
| 3E | 1 | ADDC | A,R6 |
| 3F | 1 | ADDC | A,R7 |
| 40 | 2 | JC | code addr |
| 41 | 2 | AJMP | code addr |
| 42 | 2 | ORL | data addr,A |
| 43 | 3 | ORL | data addr,#data |
| 44 | 2 | ORL | A,#data |
| 45 | 2 | ORL | A,data addr |
| 46 | 1 | ORL | A,@R0 |
| 47 | 1 | ORL | A,@R1 |
| 48 | 1 | ORL | A,R0 |
| 49 | 1 | ORL | A,R1 |
| 4A | 1 | ORL | A,R2 |
| 4B | 1 | ORL | A,R3 |
| 4C | 1 | ORL | A,R4 |
| 4D | 1 | ORL | A,R5 |
| 4E | 1 | ORL | A,R6 |
| 4F | 1 | ORL | A,R7 |
| 50 | 2 | JNC | code addr |
| 51 | 2 | ACALL | code addr |
| 52 | 2 | ANL | data addr,A |
| 53 | 3 | ANL | data addr,#data |
| 54 | 2 | ANL | A,#data |
| 55 | 2 | ANL | A,data addr |
| 56 | 1 | ANL | A,@R0 |
| 57 | 1 | ANL | A,@R1 |
| 58 | 1 | ANL | A,R0 |
| 59 | 1 | ANL | A,R1 |
| 5A | 1 | ANL | A,R2 |
| 5B | 1 | ANL | A,R3 |
| 5C | 1 | ANL | A,R4 |
| 5D | 1 | ANL | A,R5 |
| 5E | 1 | ANL | A,R6 |
| 5F | 1 | ANL | A,R7 |
| 60 | 2 | JZ | code addr |
| 61 | 2 | AJMP | code addr |
| 62 | 2 | XRL | data addr,A |
| 63 | 3 | XRL | data addr,#data |
| 64 | 2 | XRL | A,#data |
| 65 | 2 | XRL | A,data addr |
| 66 | 1 | XRL | A,@R0 |
| 67 | 1 | XRL | A,@R1 |
| 68 | 1 | XRL | A,R0 |
| 69 | 1 | XRL | A,R1 |
| 6A | 1 | XRL | A,R2 |
| 6B | 1 | XRL | A,R3 |
| 6C | 1 | XRL | A,R4 |
| 6D | 1 | XRL | A,R5 |
| 6E | 1 | XRL | A,R6 |
| 6F | 1 | XRL | A,R7 |
| 70 | 2 | JNZ | code addr |
| 71 | 2 | ACALL | code addr |
| 72 | 2 | ORL | C,bit addr |
| 73 | 1 | JMP | @A + DPTR |
| 74 | 2 | MOV | A,#data |
| 75 | 3 | MOV | data addr,#data |
| 76 | 2 | MOV | @R0,#data |
| 77 | 2 | MOV | @R1,#data |
| 78 | 2 | MOV | R0,#data |
| 79 | 2 | MOV | R1,#data |
| 7A | 2 | MOV | R2,#data |
| 7B | 2 | MOV | R3,#data |
| 7C | 2 | MOV | R4,#data |
| 7D | 2 | MOV | R5,#data |
| 7E | 2 | MOV | R6,#data |
| 7F | 2 | MOV | R7,#data |

**Table 3. Instruction Opcodes in Hexadecimal Order** (Continued)

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 80 | 2 | SJMP | code addr |
| 81 | 2 | AJMP | code addr |
| 82 | 2 | ANL | C,bit addr |
| 83 | 1 | MOVC | A,@A + PC |
| 84 | 1 | DIV | AB |
| 85 | 3 | MOV | data addr,data addr |
| 86 | 2 | MOV | data addr,@R0 |
| 87 | 2 | MOV | data addr,@R1 |
| 88 | 2 | MOV | data addr,R0 |
| 89 | 2 | MOV | data addr,R1 |
| 8A | 2 | MOV | data addr,R2 |
| 8B | 2 | MOV | data addr,R3 |
| 8C | 2 | MOV | data addr,R4 |
| 8D | 2 | MOV | data addr,R5 |
| 8E | 2 | MOV | data addr,R6 |
| 8F | 2 | MOV | data addr,R7 |
| 90 | 3 | MOV | DPTR,#data |
| 91 | 2 | ACALL | code addr |
| 92 | 2 | MOV | bit addr,C |
| 93 | 1 | MOVC | A,@A + DPTR |
| 94 | 2 | SUBB | A,#data |
| 95 | 2 | SUBB | A,data addr |
| 96 | 1 | SUBB | A,@R0 |
| 97 | 1 | SUBB | A,@R1 |
| 98 | 1 | SUBB | A,R0 |
| 99 | 1 | SUBB | A,R1 |
| 9A | 1 | SUBB | A,R2 |
| 9B | 1 | SUBB | A,R3 |
| 9C | 1 | SUBB | A,R4 |
| 9D | 1 | SUBB | A,R5 |
| 9E | 1 | SUBB | A,R6 |
| 9F | 1 | SUBB | A,R7 |
| A0 | 2 | ORL | C,/bit addr |
| A1 | 2 | AJMP | code addr |
| A2 | 2 | MOV | C,bit addr |
| A3 | 1 | INC | DPTR |
| A4 | 1 | MUL | AB |
| A5 | | reserved | |
| A6 | 2 | MOV | @R0,data addr |
| A7 | 2 | MOV | @R1,data addr |
| A8 | 2 | MOV | R0,data addr |
| A9 | 2 | MOV | R1,data addr |
| AA | 2 | MOV | R2,data addr |
| AB | 2 | MOV | R3,data addr |
| AC | 2 | MOV | R4,data addr |
| AD | 2 | MOV | R5,data addr |
| AE | 2 | MOV | R6,data addr |
| AF | 2 | MOV | R7,data addr |
| B0 | 2 | ANL | C,/bit addr |
| B1 | 2 | ACALL | code addr |
| B2 | 2 | CPL | bit addr |
| B3 | 1 | CPL | C |
| B4 | 3 | CJNE | A,#data,code addr |
| B5 | 3 | CJNE | A,data addr,code addr |
| B6 | 3 | CJNE | @R0,#data,code addr |
| B7 | 3 | CJNE | @R1,#data,code addr |
| B8 | 3 | CJNE | R0,#data,code addr |
| B9 | 3 | CJNE | R1,#data,code addr |
| BA | 3 | CJNE | R2,#data,code addr |
| BB | 3 | CJNE | R3,#data,code addr |
| BC | 3 | CJNE | R4,#data,code addr |
| BD | 3 | CJNE | R5#data,code addr |
| BE | 3 | CJNE | R6,#data,code addr |
| BF | 3 | CJNE | R7,#data,code addr |

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| C0 | 2 | PUSH | data addr |
| C1 | 2 | AJMP | code addr |
| C2 | 2 | CLR | bit addr |
| C3 | 1 | CLR | C |
| C4 | 1 | SWAP | A |
| C5 | 2 | XCH | A,data addr |
| C6 | 1 | XCH | A,@R0 |
| C7 | 1 | XCH | A,@R1 |
| C8 | 1 | XCH | A,R0 |
| C9 | 1 | XCH | A,R1 |
| CA | 1 | XCH | A,R2 |
| CB | 1 | XCH | A,R3 |
| CC | 1 | XCH | A,R4 |
| CD | 1 | XCH | A,R5 |
| CE | 1 | XCH | A,R6 |
| CF | 1 | XCH | A,R7 |
| D0 | 2 | POP | data addr |
| D1 | 2 | ACALL | code addr |
| D2 | 2 | SETB | bit addr |
| D3 | 1 | SETB | C |
| D4 | 1 | DA | A |
| D5 | 3 | DJNZ | data addr,code addr |
| D6 | 1 | XCHD | A,@R0 |
| D7 | 1 | XCHD | A,@R1 |
| D8 | 2 | DJNZ | R0,code addr |
| D9 | 2 | DJNZ | R1,code addr |
| DA | 2 | DJNZ | R2,code addr |
| DB | 2 | DJNZ | R3,code addr |
| DC | 2 | DJNZ | R4,code addr |
| DD | 2 | DJNZ | R5,code addr |
| DE | 2 | DJNZ | R6,code addr |
| DF | 2 | DJNZ | R7,code addr |
| E0 | 1 | MOVX | A,@ DPTR |
| E1 | 2 | AJMP | code addr |
| E2 | 1 | MOVX | A,@R0 |
| E3 | 1 | MOVX | A,@R1 |
| E4 | 1 | CLR | A |
| E5 | 2 | MOV | A,data addr |
| E6 | 1 | MOV | A,@R0 |
| E7 | 1 | MOV | A,@R1 |
| E8 | 1 | MOV | A,R0 |
| E9 | 1 | MOV | A,R1 |
| EA | 1 | MOV | A,R2 |
| EB | 1 | MOV | A,R3 |
| EC | 1 | MOV | A,R4 |
| ED | 1 | MOV | A,R5 |
| EE | 1 | MOV | A,R6 |
| EF | 1 | MOV | A,R7 |
| F0 | 2 | MOVX | @ DPTR,A |
| F1 | 1 | ACALL | code addr |
| F2 | 1 | MOVX | @R0,A |
| F3 | 1 | MOVX | @R1,A |
| F4 | 1 | CPL | A |
| F5 | 2 | MOV | data addr,A |
| F6 | 1 | MOV | @R0,A |
| F7 | 1 | MOV | @R1,A |
| F8 | 1 | MOV | R0,A |
| F9 | 1 | MOV | R1,A |
| FA | 1 | MOV | R2,A |
| FB | 1 | MOV | R3,A |
| FC | 1 | MOV | R4,A |
| FD | 1 | MOV | R5,A |
| FE | 1 | MOV | R6,A |
| FF | 1 | MOV | R7,A |

Signetics

# 80C451/83C451
## I/O Expanded CMOS Microcontroller

*Product Specification*

**Military Microprocessor Products**

### DESCRIPTION

The Signetics 80C451/83C451 is an I/O expanded, single-chip microcontroller fabricated with Signetics high-density epitaxial CMOS technology. It is offered in a 68-pin LLCC and a 64-pin DIP. The Signetics CMOS technology combines the high-speed and high-density characteristics of HMOS with the low power of CMOS. Signetics epitaxial substrate minimizes latch-up sensitivity.

The 80C451/83C451 is a functional extension of the 80C31/80C51 microcontroller with three additional I/O ports and four I/O control lines. The LLCC version has a total of 68 pins. The DIP version has a total of 64 pins. The four added control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

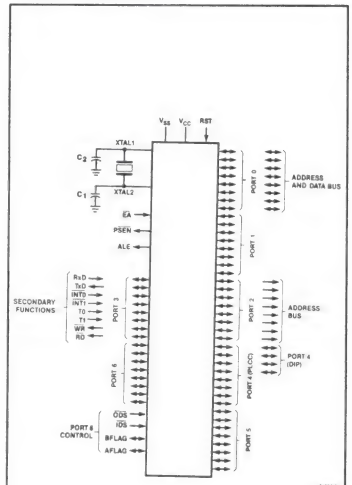
The 80C451/83C451 includes a 4k × 8 ROM; a 128 × 8 RAM; 56 (LLCC) or 52 (DIP) I/O lines; two 16-bit timer/counters; a five source, two priority level, nested interrupt structure; a serial I/O port for either a full-duplex UART, I/O expansion, or multiprocessor communications; and on-chip oscillator and clock circuits.

The 80C451/83C451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning., Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

### FEATURES

- **80C451 — CPU with RAM and I/O**
- **83C451 — 80C451 with mask-programmable ROM**
- **68-pin LLCC and 64-pin DIP packages**
  - **Seven 8-bit I/O ports (LLCC version)**
  - **Six 8-bit ports and one 4-bit port (DIP version)**
- **Port 6 features:**
  - **8 data pins**
  - **4 control pins**
  - **Direct MPU bus interface**
  - **Parallel printer interface**
- **Pin compatible with 87C451 microcontroller**
- **On the microcontroller:**
  - **80C51 CPU**
  - **4k × 8 ROM (83C451 only)**
  - **128 × 8 RAM**
  - **Two 16-bit timer/counters**
  - **Full-duplex serial I/O**
  - **Two external interrupts**
- **External memory addressing capability:**
  - **64k ROM and 64k RAM**
- **Low power consumption:**
  - **Normal operation: 24mA typical @ 5V, 12MHz**
  - **Idle mode: 3mA typical @ 5V, 12MHz**
  - **Power-down mode: 50μA typical @ 2V**

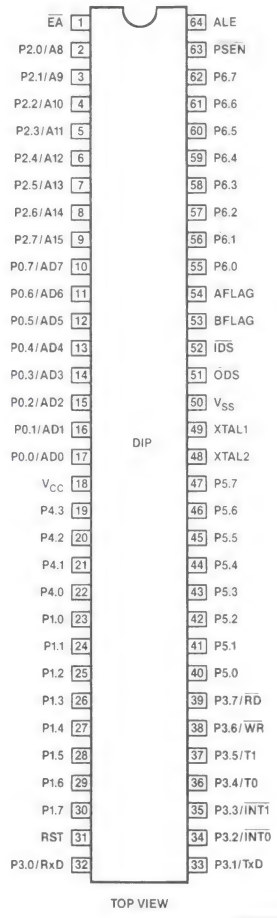
### LOGIC SYMBOL



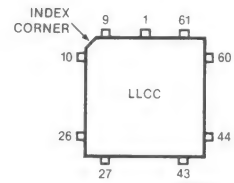

NOTES:
C1, C2 = 30 pfd ± 10pfd for crystals
= 40 pfd ± 10 pfd for ceramic resonators.

# I/O Expanded CMOS Microcontroller | 80C451/83C451

## PIN CONFIGURATIONS




TOP VIEW




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | EA | 35 | RST |
| 2 | P2.0/A8 | 36 | P3.0/R × D |
| 3 | P2.1/A9 | 37 | P3.1/T × D |
| 4 | P2.2/A10 | 38 | P3.2/INT0 |
| 5 | P2.3/A11 | 39 | P3.3/INT1 |
| 6 | P2.4/A12 | 40 | P3.4/T0 |
| 7 | P2.5/A13 | 41 | P3.5/T1 |
| 8 | P2.6/A14 | 42 | P3.6/WR |
| 9 | P2.7/A15 | 43 | P3.7/RD |
| 10 | P0.7/AD7 | 44 | P5.0 |
| 11 | P0.6/AD6 | 45 | P5.1 |
| 12 | P0.5/AD5 | 46 | P5.2 |
| 13 | P0.4/AD4 | 47 | P5.3 |
| 14 | P0.3/AD3 | 48 | P5.4 |
| 15 | P0.2/AD2 | 49 | P5.5 |
| 16 | P0.1/AD1 | 50 | P5.6 |
| 17 | P0.0/AD0 | 51 | P5.7 |
| 18 | VCC | 52 | XTAL2 |
| 19 | P4.7 | 53 | XTAL1 |
| 20 | P4.6 | 54 | VSS |
| 21 | P4.5 | 55 | ODS |
| 22 | P4.4 | 56 | IDS |
| 23 | P4.3 | 57 | BFLAG |
| 24 | P4.2 | 58 | AFLAG |
| 25 | P4.1 | 59 | P6.0 |
| 26 | P4.0 | 60 | P6.1 |
| 27 | P1.0 | 61 | P6.2 |
| 28 | P1.1 | 62 | P6.3 |
| 29 | P1.2 | 63 | P6.4 |
| 30 | P1.3 | 64 | P6.5 |
| 31 | P1.4 | 65 | P6.6 |
| 32 | P1.5 | 66 | P6.7 |
| 33 | P1.6 | 67 | PSEN |
| 34 | P1.7 | 68 | ALE |

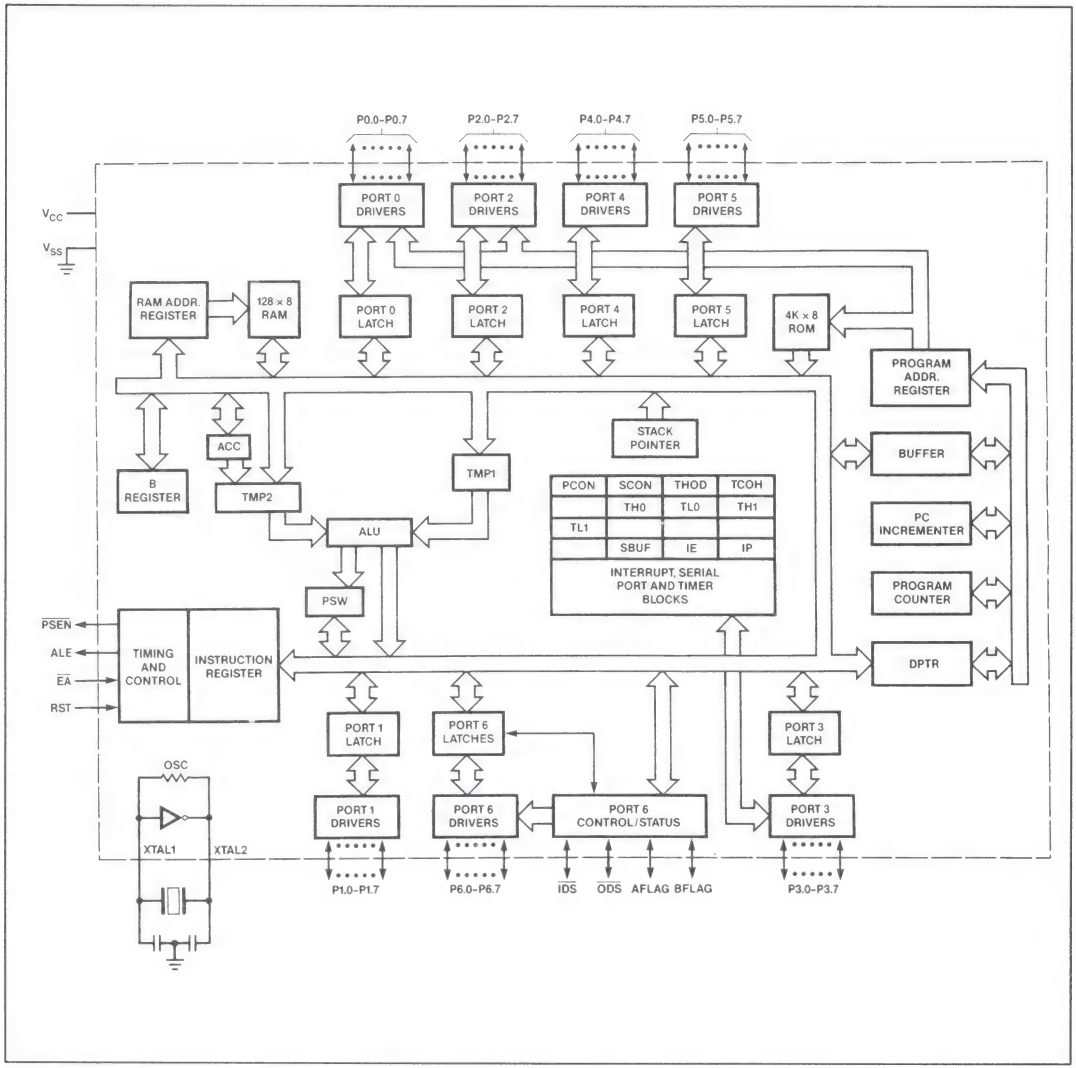
# I/O Expanded CMOS Microcontroller — 80C451/83C451

## ORDERING INFORMATION

| PACKAGES | ORDER CODE | |
|---|---|---|
| 64-Pin Ceramic DIP | 80C451/BXA | 83C451*/BXA |
| 68-Pin LLCC | 80C451/BUA | 83C451*/BUA |

**NOTES:**
* Factory will assign a unique CVXXXX part number.

## BLOCK DIAGRAM



## PIN CONFIGURATION

| MNEMONIC | PIN NUMBER | | | NAME AND FUNCTION |
|---|---|---|---|---|
| | DIP | LLCC | TYPE | |
| $V_{SS}$ | 50 | 54 | | **Ground:** OV reference |
| $V_{CC}$ | 18 | 18 | | **Power Supply:** +5V |
| P0.0-P0.7 | 17-10 | 17-10 | I/O | **Port 0:** An 8-bit open drain, bidirectional I/O port. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory, and outputs instruction bytes during program verification. External pull-ups are required during program verification. Port 0 can sink/source eight LS TTL inputs. |
| P1.0-P1.7 | 23-30 | 27-34 | I/O | **Port 1:** An 8-bit bidirectional I/O port with internal pull-ups. Port 1 receives the low-order address bytes during program verification. In the 83C451, port 1 can sink/source three LS TTL inputs, and drive CMOS inputs without external pull-ups. |
| P2.0-P2.7 | 2-9 | 2-9 | I/O | **Port 2:** An 8-bit bidirectional I/O port with internal pull-ups. Port 2 emits the high-order address bytes during accesses to external memory and receives the high-order address bit and control signals during program verification in the 83C451. Port 2 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. |
| P3.0-P3.7 | 32-39 | 36-43 | I/O | **Port 3:** An 8-bit bidirectional I/O port with internal pull-ups. Port 3 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. Port 3 also serves the 83C451 special functions listed below: |
| | 32 | 36 | I | RXD (P3.0): Serial input port |
| | 33 | 37 | O | TXD (P3.1): Serial output port |
| | 34 | 38 | I | $\overline{INT0}$ (P3.2): External interrupt 0 |
| | 35 | 39 | I | $\overline{INT1}$ (P3.3): External interrupt 1 |
| | 36 | 40 | I | T0 (P3.4): Timer 0 external input |
| | 37 | 41 | I | T1 (P3.5): Timer 1 external input |
| | 38 | 42 | O | $\overline{WR}$ (P3.6): External data memory write strobe |
| | 39 | 43 | O | $\overline{RD}$ (P3.7): External data memory read strobe |
| P4.0-P4.3<br>P4.0-P4.7 | 22-19 | 26-19 | I/O<br>I/O | **Port 4:** A 4- or 8-bit bidirectional port with internal pull-ups. Port 4 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. |
| P5.0-P5.7 | 40-47 | 44-51 | I/O | **Port 5:** An 8-bit I/O port with internal pull-ups. Port 5 can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. |
| P6.0-P6.7 | 55-62 | 59-66 | I/O | **Port 6:** A specialized 8-bit bidirectional I/O port with internal pull-ups. This special port can sink/source three LS TTL inputs and drive CMOS inputs without external pull-ups. Port 6 can be used in a strobed or non-strobed mode of operation, and in conjunction with four control pins that serve the functions listed below. |
| | | | | **Port 6 Control Lines:** |
| $\overline{ODS}$ | 51 | 55 | I | $\overline{ODS}$: Output data strobe |
| $\overline{IDS}$ | 52 | 56 | I | $\overline{IDS}$: Input data strobe |
| BFLAG | 53 | 57 | I/O | BFLAG: A bidirectional I/O pin with internal pull-ups |
| AFLAG | 54 | 58 | I/O | A FLAG: A bidirectional I/O pin with internal pull-ups |
| RST | 31 | 35 | I | **RESET:** A High level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits power-on reset using only a capacitor connected to the $V_{CC}$. |
| ALE | 64 | 68 | O | **Address Latch Enable:** An output for latching the Low byte of the address during accesses to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access, at which time one ALE is skipped. ALE can sink/source eight LS TTL inputs and drive CMOS inputs without an external pull-up. |
| $\overline{PSEN}$ | 63 | 67 | O | **Program Store Enable:** This output is the read strobe to external program memory. $\overline{PSEN}$ is activated twice each machine cycle during fetches from external program memory; however, when executing out of external program memory, two activations of $\overline{PSEN}$ are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. $\overline{PSEN}$ can sink/source eight LS TTL inputs and drive CMOS inputs without an external pull-up. |
| $\overline{EA}$ | 1 | 1 | I | **Instruction Execution Control:** When $\overline{EA}$ is held High, the CPU executes out of internal program memory, unless the program counter exceeds OFFFH. When $\overline{EA}$ is held Low, the CPU executes out of external program memory. $\overline{EA}$ must never be allowed to float. |
| XTAL1 | 49 | 53 | I | **Crystal 1:** An input to the inverting amplifier that forms the oscillator. This input receives the external oscillator when an external oscillator is used. |
| XTAL2 | 48 | 52 | O | **Crystal 2:** Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used. |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |
| $V_{CC}$ | Voltage from $V_{CC}$ to $V_{SS}$[2] | -0.5 to +6.5 | V |
| $V_I$ | Voltage from any pin to $V_{SS}$[2] | -0.5 to $V_{CC}$ +0.5 | V |
| PD | Power dissipation | 200 | mW |

## DC ELECTRICAL CHARACTERISTICS $T_A$ = -55°C to +125°C, $V_{CC}$ = 5V ± 20%, $V_{SS}$ = 0V.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IL}$ | Input Low voltage, except $\overline{EA}$ | | -0.5 | 0.2 $V_{CC}$ – 0.1 | V |
| $V_{IL1}$ | Input Low voltage, $\overline{EA}$ | | -0.5 | 0.2 $V_{CC}$ – 0.3 | V |
| $V_{IH}$ | Input High voltage, except XTAL1, RST | | 0.2 $V_{CC}$ +0.9 | $V_{CC}$ + 0.5 | V |
| $V_{IH1}$ | Input High voltage, XTAL1, RST | | 0.7 $V_{CC}$ | $V_{CC}$ + .05 | V |
| $V_{OL}$ | Output Low voltage, ports 1,2,3,4,5,6, AFLAG, BFLAG | $I_{OL}$ = 1.6mA[4] | | 0.45 | V |
| $V_{OL1}$ | Output Low voltage, port 0, ALE, $\overline{PSEN}$ | $I_{OL}$ = 3.2mA[4] | | 0.45 | V |
| $V_{OH}$ | Output High voltage, ports 1,2,3,4,5,6, AFLAG, BFLAG | $V_{CC}$ = 5V ± 10% | | | |
| | | $I_{OH}$ = -60µA | 2.4 | | V |
| | | $I_{OH}$ = -25µA | 0.75$V_{CC}$ | | V |
| | | $I_{OH}$ = -10µA | 0.9$V_{CC}$ | | V |
| $V_{OH1}$ | Output High voltage, port 0 in external bus mode, ALE, $\overline{PSEN}$ | $V_{CC}$ = 5V ± 10% | | | |
| | | $I_{OH}$ = -400µA | 2.4 | | V |
| | | $I_{OH}$ = -150µA | 0.75$V_{CC}$ | | V |
| | | $I_{OH}$ = -40µA[5] | 0.9$V_{CC}$ | | V |
| $I_{IL}$ | Logical 0 input current, ports 1,2,3,4,5,6, AFLAG, BFLAG | $V_{IN}$ = 0.45V | | -50 | µA |
| $I_{TL}$ | Logical 1 to 0 transition current, ports 1,2,3,4,5,6, AFLAG, BFLAG | $V_{IN}$ = 2V | | -650 | µA |
| $I_{LI}$ | Input leakage, current port 0, $\overline{EA}$, $\overline{IDS}$, $\overline{ODS}$ | 0.45V ≤ $V_{IN}$ ≤ $V_{CC}$ | | ±10 | µA |
| $R_{RST}$ | Reset pulldown resistor | | 50 | 150 | kΩ |
| $C_{IO}$ | Pin capacitance[9] | Test freq= 1MHz, $T_A$ = 25°C | | 10 | pF |
| $I_{PD}$ | Power-down current | $V_{CC}$ = 2V to 6V[6] | | 50 | µA |

## MAXIMUM $I_{CC}$ (mA)

| FREQUENCY/SUPPLY VOLTAGE | OPERATING[7] | | | IDLE[8] | | | UNITS |
|---|---|---|---|---|---|---|---|
| | 4V | 5V | 6V | 4V | 5V | 6V | |
| 3.5MHz[10] | 5.0 | 7.0 | 9.0 | 1.5 | 2.5 | 3.5 | mA |
| 8.0MHz[10] | 11.0 | 14.5 | 18.0 | 2.0 | 3.5 | 4.5 | mA |
| 12MHz | 15.0 | 20.0 | 25.0 | 2.5 | 4.0 | 5.0 | mA |

## AC ELECTRICAL CHARACTERISTICS

$T_A$ = -55°C to +125°C, $V_{CC}$ = 5V ± 20%, $V_{SS}$ = OV, load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80 pF[3]

| SYMBOL | PARAMETER | 12MHz CLOCK | | VARIABLE CLOCK ($f = 1/t_{CLCL}$) | | UNIT |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| | Speed range (see ordering code) | | | | | |
| | 0 | | | 3.5 | 12 | |
| $1/t_{CLCL}$ | 1 | | | 3.5 | 16 | MHz |
| | 2 | | | 0.5 | 12 | |
| $t_{LHLL}$ | ALE pluse width | 127 | | $2t_{CLCL}$-40 | | ns |
| $t_{AVLL}$ | Address valid to ALE Low | 28 | | $t_{CLCL}$-55 | | ns |
| $t_{LLAX}$ | Address hold after ALE Low | 48 | | $t_{CLCL-35}$ | | ns |
| $t_{LLIV}$ | ALE Low to valid instr in | | 234 | | $4t_{CLCL}$-100 | ns |
| $t_{LLPL}$ | ALE Low to $\overline{PSEN}$ Low | 43 | | $t_{CLCL}$-40 | | ns |
| $t_{PLPH}$ | $\overline{PSEN}$ pulse width | 205 | | $3t_{CLCL}$-45 | | ns |
| $t_{PLIV}$ | $\overline{PSEN}$ Low to valid instr in | | 145 | | $3t_{CLCL}$-105 | ns |
| $t_{PXIX}$ | Input instr hold after $\overline{PSEN}$ | 0 | | 0 | | ns |
| $t_{PXIZ}$ | Input instr float after $\overline{PSEN}$ | | 59 | | $t_{CLCL}$-25 | ns |
| $t_{AVIV}$ | Address to valid instr in | | 312 | | $5t_{CLCL}$-105 | ns |
| $t_{PLAZ}$ | $\overline{PSEN}$ Low to address float | | 20 | | 20 | ns |
| $t_{RLRH}$ | $\overline{RD}$ pulse width | 400 | | $6t_{CLCL}$-100 | | ns |
| $t_{WLWH}$ | $\overline{WR}$ pulse width | 400 | | $6t_{CLCL}$-100 | | ns |
| $t_{RLDV}$ | $\overline{RD}$ Low to valid data in | | 252 | | $5t_{CLCL}$-165 | ns |
| $t_{RHDX}$ | Data hold after $\overline{RD}$ | 0 | | 0 | | ns |
| $t_{RHDZ}$ | Data float after $\overline{RD}$ | | 97 | | $2t_{CLCL}$-70 | ns |
| $t_{LLDV}$ | ALE Low to valid data in | | 517 | | $8t_{CLCL}$-150 | ns |
| $t_{AVDV}$ | Address to valid data in | | 585 | | $9t_{CLCL}$-165 | ns |
| $t_{LLWL}$ | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 200 | 300 | $3t_{CLCL}$-50 | $3t_{CLCL}$+50 | ns |
| $t_{QVWX}$ | Data valid to $\overline{WR}$ transition | 23 | | $t_{CLCL}$-60 | | ns |
| $t_{WHQX}$ | Data hold after $\overline{WR}$ | 33 | | $t_{CLCL}$-50 | | ns |
| $t_{RLAZ}$ | $\overline{RD}$ Low to address float | | 0 | | 0 | ns |
| $t_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE High | 43 | 123 | $t_{CLCL}$-40 | $t_{CLCL}$+40 | ns |
| **Port 6 input (input rise and fall times ≤ 5ns)** | | | | | | |
| $t_{ILIH}$ | $\overline{IDS}$ width | 270 | | $3t_{CLCL}$+20 | | ns |
| $t_{DVIH}$ | Data setup to $\overline{IDS}$ High | 10 | | 10 | | ns |
| $t_{IHDX}$ | Data hold after $\overline{IDS}$ | 30 | | 30 | | ns |
| $t_{FLIL}$ | PE to $\overline{IDS}$ | 25 | | 25 | | ns |
| $t_{IVFV}$ | $\overline{IDS}$ to BFLAG (IBF) delay | | 130 | | 130 | ns |
| **Port 6 ouput** | | | | | | |
| $t_{OLOH}$ | $\overline{ODS}$ width | 270 | | $3t_{CLCL}$+20 | | ns |
| $t_{FVDV}$ | SEL to data out delay | | 85 | | 85 | ns |
| $t_{OLDV}$ | $\overline{ODS}$ to data out delay | | 80 | | 80 | ns |
| $t_{OHDZ}$ | $\overline{ODS}$ to data float delay | | 35 | | 35 | ns |
| $t_{OVFV}$ | $\overline{ODS}$ to AFLAG (OBF) delay | | 100 | | 100 | ns |
| $t_{FLDV}$ | PE to data out delay | | 120 | | 120 | ns |
| $t_{OHFH}$ | $\overline{ODS}$ High to AFLAG (SEL) delay | 100 | | 100 | | ns |

**NOTES:**

1. Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection on its internal devices from damaging effects of excessive static charge. Nonetheless it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified.
4. Capacitive loading on ports 0 and 2 can cause spurious noise to be superimposed on the $V_{OLS}$ of ALE and ports 1 and 3. The noise is caused by external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases it could be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.
5. Capacitive loading on ports 0 and 2 can cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall before the $0.9V_{CC}$ specification when the address bits are stabilizing.
6. Power-down $I_{CC}$ is measured with all output pins disconnected; $\overline{EA}$ = port 0 = $V_{CC}$; XTAL2 N.C.; RST = $V_{SS}$.
7. $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL}$ = $V_{SS}$+ 0.5V, $V_{IH}$ = $V_{CC}$ -0.5V; XTAL1 N.C.; $\overline{EA}$ = RST = Port 0 = $V_{CC}$. $I_{CC}$ will be slightly higher if a crystal oscillator is used.
8. Idle $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL}$ = $V_{SS}$+ 0.5V, $V_{IH}$ = $V_{CC}$ -0.5V; XTAL N.C.; port 0 = $V_{CC}$; $\overline{EA}$ = RST = $V_{SS}$.
9. $C_{IO}$ is measured initially and after any design changes which may affect capacitance.
10. This parameter is guaranteed, but not tested.

## PORTS 4 and 5

Ports 4 and 5 are bidirectional I/O ports with internal pull-ups. Port 4 is an 8-bit port (LLCC version) or a 4-bit port (DIP version). Port 4 and port 5 pins, with ones written to them, are pulled High by the internal pull-ups, and in that state can be used as inputs. Ports 4 and 5 are addressed at the special function register addresses shown in Table 1.

## PORT 6

Port 6 is a special 8-bit bidirectional I/O port with internal pull-ups. (See Figure 1.) This port can be used as a standard I/O port, or in strobed modes of operation in conjunction with four special control lines: $\overline{ODS}$, $\overline{IDS}$, AFLAG, and BFLAG. Port 6 operating modes are controlled by the port 6 control status register (CSR). Port 6 and the CSR are addressed at the special function register addresses when in Table 1. The following four control pins are used in conjunction with port 6:

**$\overline{ODS}$:** Output data strobe input for port 6. $\overline{ODS}$ can be programmed to control the port 6 output drivers and the output buffer full flag (OBF), or to clear only the OBF flag bit in the CSR (output-always mode). $\overline{ODS}$ is active Low for output driver control. The OBF flag can be programmed to be cleared on the negative or positive edge of $\overline{ODS}$.

**$\overline{IDS}$**: Input data strobe input for port 6. $\overline{IDS}$ is used to control the port 6 input latch and input buffer full flag (IBF) bit in the CSR. The input data latch can be programmed to be transparent when the $\overline{IDS}$ is Low and latched on the positive transition of $\overline{IDS}$, or to latch only on the positive transition of $\overline{IDS}$. Correspondingly, the IBF flag is set on the negative or positive transition of $\overline{IDS}$.

**AFLAG:** A bidirectional I/O pin. AFLAG can be programmed to be an output set High or Low under program control, or to output the state of the output buffer full flag. AFLAG can also be programmed to be an input which selects whether the contents of the output buffer, or the contents of the port 6 control status register will be output on port 6. This feature grants complete port 6 status to external devices.

**BFLAG:** A bidirectional I/O pin. BFLAG can be programmed to be an output, set High or Low under program control, or to output the state of the input buffer full flag. BFLAG can also be programmed to input an enable signal for port 6. When BFLAG is used as an enable input, port 6 output drivers are in the High impedance state, and the input latch does not respond to the $\overline{IDS}$ strobe when BFLAG is High. Both features are enabled when BFLAG is Low. This feature facilitates the use of the 83C451 in bused multiprocessor systems..

## CONTROL STATUS REGISTER

The control status register (CSR) establishes the mode of operation for port 6 and indicates the current status of the port 6 I/O registers. All control status register bits can be read and written by the CPU, except bits 0 and 1, which are read only. Reset writes ones to bits 2 through 7, and writes zeros to bits 0 and 1.

**CSR.0 — Input Buffer Full Flag (IBF) (Read only)**
The IBFR bit is set to a logic 1 when port 6 data is loaded into the input buffer under control of $\overline{IDS}$. This can occur on the negative or positive edge of $\overline{IDS}$, as determined by CSR.2. IBF is cleared when the CPU reads the input buffer register.

**CSR.1 — Output Buffer Full Flag (OBF) (Read only)**
The OBF flag is set to a logic 1 when the CPU writes to the port 6 output data buffer. OBF is cleared by the positive or negative edge of $\overline{ODS}$, as determined by CSR.3.

**CSR.2 — IDS Mode Select (IDSM)**
When CSR.2 = 0, a Low-to-High transition on the $\overline{IDS}$ pin sets the IBF flag. The port 6 input buffer is loaded on the $\overline{IDS}$ positive edge. When CSR.2 = 1, a High-to-Low transition on the $\overline{IDS}$ pin sets the IBF flag. The port 6 input buffer is transparent when $\overline{IDS}$ is Low, and latched when $\overline{IDS}$ is High.

**CSR.3 — Output Buffer Full Flag Clear Mode (OBFC)**
When CSR.3 = 1, the positive edge of the $\overline{ODS}$ input clears the OBF flag. When CSR.3 = 0, the negative edge of the $\overline{ODS}$ input clears the OBF flag.

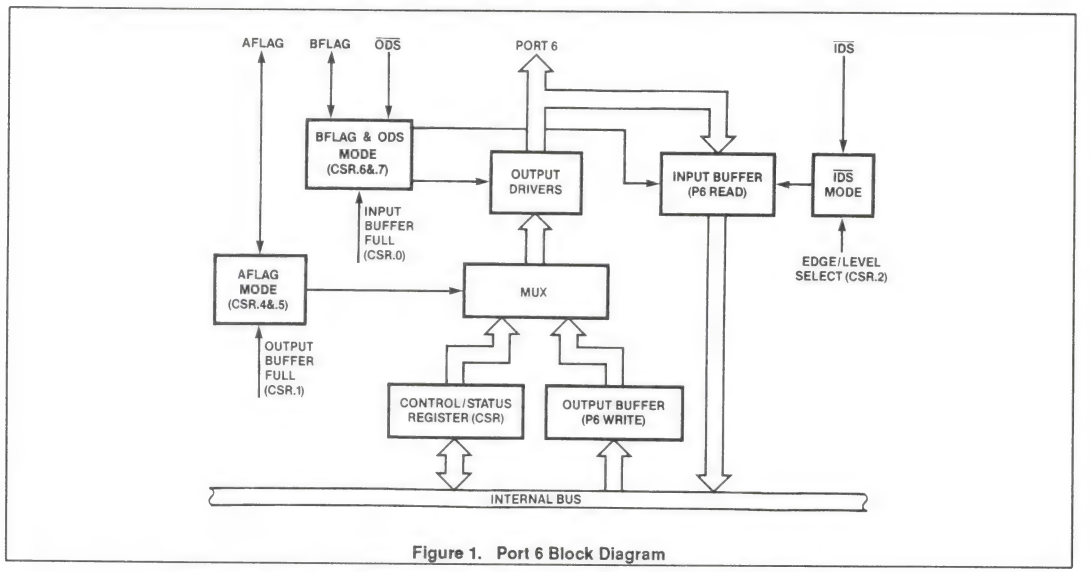



**Figure 1. Port 6 Block Diagram**

**CSR.4, CSR.5 — AFLAG Mode Select (MA0, MA1)**
Bits 4 and 5 select the mode of operation for the AFLAG pin, as follows:

| MA1 | MA0 | AFLAG Function |
|---|---|---|
| 0 | 0 | Logic 0 output |
| 0 | 1 | Logic 1 output |
| 1 | 0 | OBF flag output (CSR.1) |
| 1 | 1 | Select (SEL) input mode |

The select (SEL) input mode is used to determine whether the port 6 data register or the control status register is output on port 6. When the select feature is enabled, the AFLAG input controls the source of port 6 output data. A logic 0 on AFLAG input selects the port 6 data register, and a logic 1 on AFLAG input selects the control status register.

**CSR.6, CSR.7 — BFLAG Mode Select (MB0, MB1)**
Bits 6 and 7 select the mode of operation for the BFLAG pin, as follows:

| MB1 | MB0 | BFLAG Function |
|---|---|---|
| 0 | 0 | Logic 0 output |
| 0 | 1 | Logic 1 output |
| 1 | 0 | IBF flag output (CSR.0) |
| 1 | 1 | Port enable ($\overline{PE}$) |

In the port enable mode, $\overline{IDS}$ and $\overline{ODS}$ inputs are disabled when BFLAG input is High. When the BFLAG input is Low, the port is enabled for I/O.

## CONTROL STATUS REGISTER

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (CSR) | MB1 | MB0 | MA1 | MA0 | OBFC | IDSM | OBF | IBF |
| | BFLAG mode select | | AFLAG mode select | | Output buffer flag clear mode | Input data strobe mode | Output buffer full flag | Input buffer full flag |
| | 0/0 = Logic 0 output*<br>0/1 = Logic 1 output*<br>1/0 = IBF output<br>1/1 = $\overline{PE}$ input<br>(0 = Select)<br>(1 = disable I/O) | | 0/0 = Logic 0 output<br>0/1 = Logic 1 output<br>1/0 = OBF output*<br>1/1 = SEL input<br>(0 = Data)<br>(1 = Control/status) | | 0 = Negative edge of $\overline{ODS}$<br>1 = Positive edge of $\overline{ODS}$ | 0 = Positive edge of $\overline{IDS}$<br>1 = Low level of $\overline{IDS}$ | 0 = Output data buffer empty<br>1 = Output data buffer full | 0 = Input data buffer empty<br>1 = input data buffer full |

* Output-always mode: MB1 = 0, MA1 = 1, and MA0 = 0. In this mode port 6 is always enabled for output. $\overline{ODS}$ only clears the OBF flag.

## SPECIAL FUNCTION REGISTER ADDRESSES

Special function register addresses for the 83C451 are identical to those of the 80C51, except for the additional registers listed in Table 1.

**Table 1. Special Function Register Addresses**

| REGISTER ADDRESS | | | BIT ADDRESS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Name | Symbol | Address | MSB | | | | | | | LSB |
| Port 4 | P4 | C0 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Port 5 | P5 | C8 | CF | CE | CD | CC | CB | CA | C9 | C8 |
| Port 6 data | P6 | D8 | DF | DE | DD | DC | DB | DA | D9 | D8 |
| Port 6 control status | CSR | E8 | EF | EE | ED | EC | EB | EA | E9 | E8 |

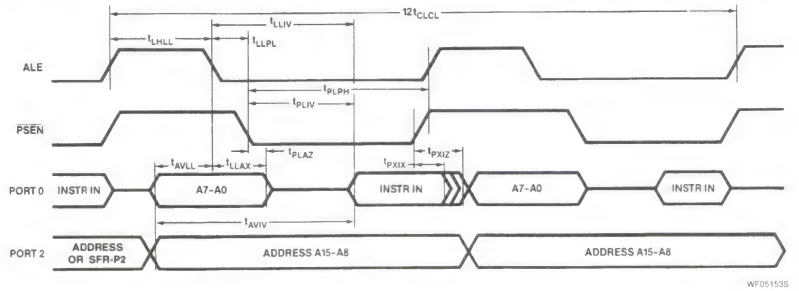



**Figure 2. Program Memory Read Cycle**

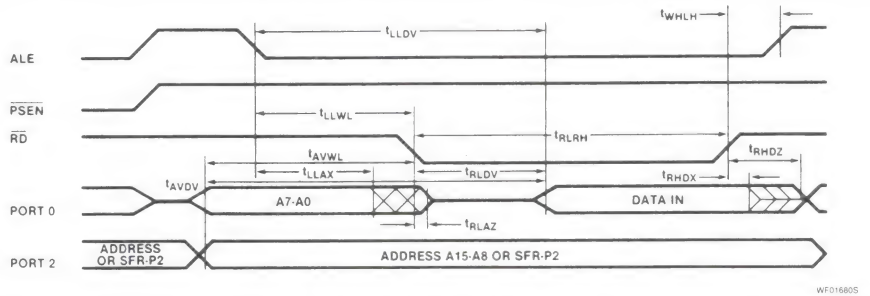



**Figure 3. Data Memory Read Cycle**

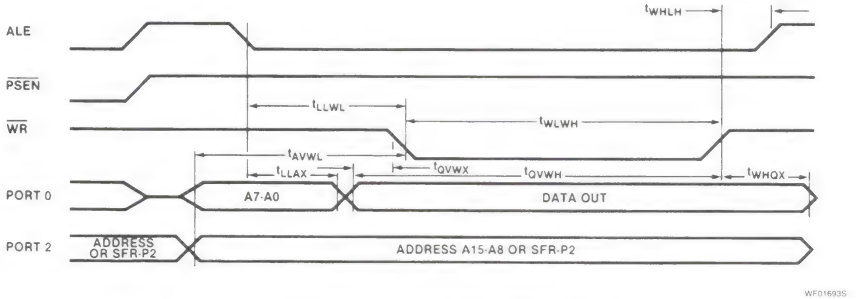



**Figure 4. Data Memory Write Cycle**

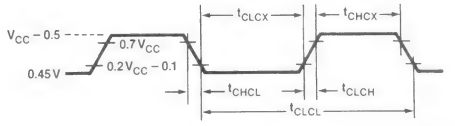
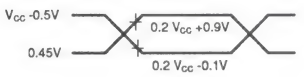
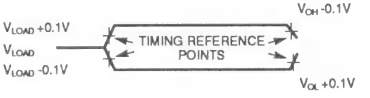



**Figure 5. External Clock Drive Waveform**




**NOTE:**
AC inputs during testing are driven at $V_{CC}$ -0.5V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at $V_{IH}$ min. for a logic "1" and $V_{IL}$ max. for a logic "0."

**Figure 6. AC Testing Input, Output Waveforms**




**NOTE:**
For timing purposes a port pin is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OL}/I_{OH} > \pm 20$mA.

**Figure 7. Float Waveforms**

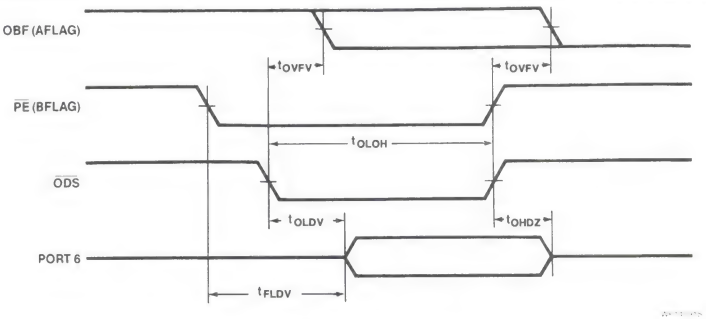



**Figure 8. Port 6 Output Waveforms**

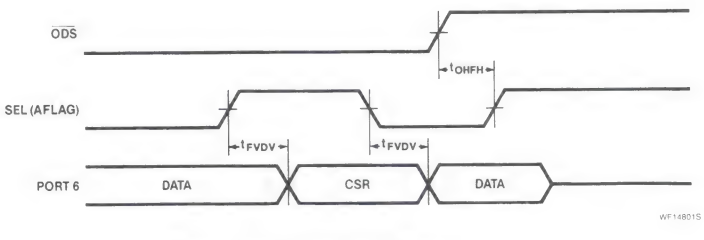



**Figure 9. Port 6 Select Mode Waveforms**

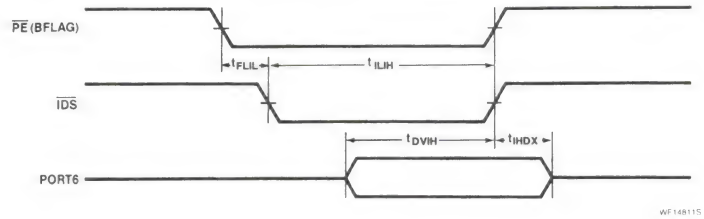



**Figure 10. Port 6 Input Waveforms**

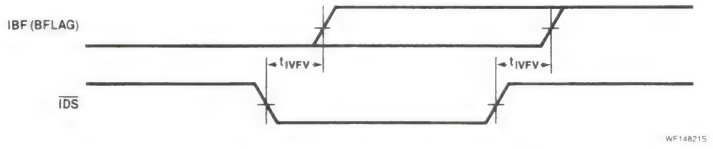
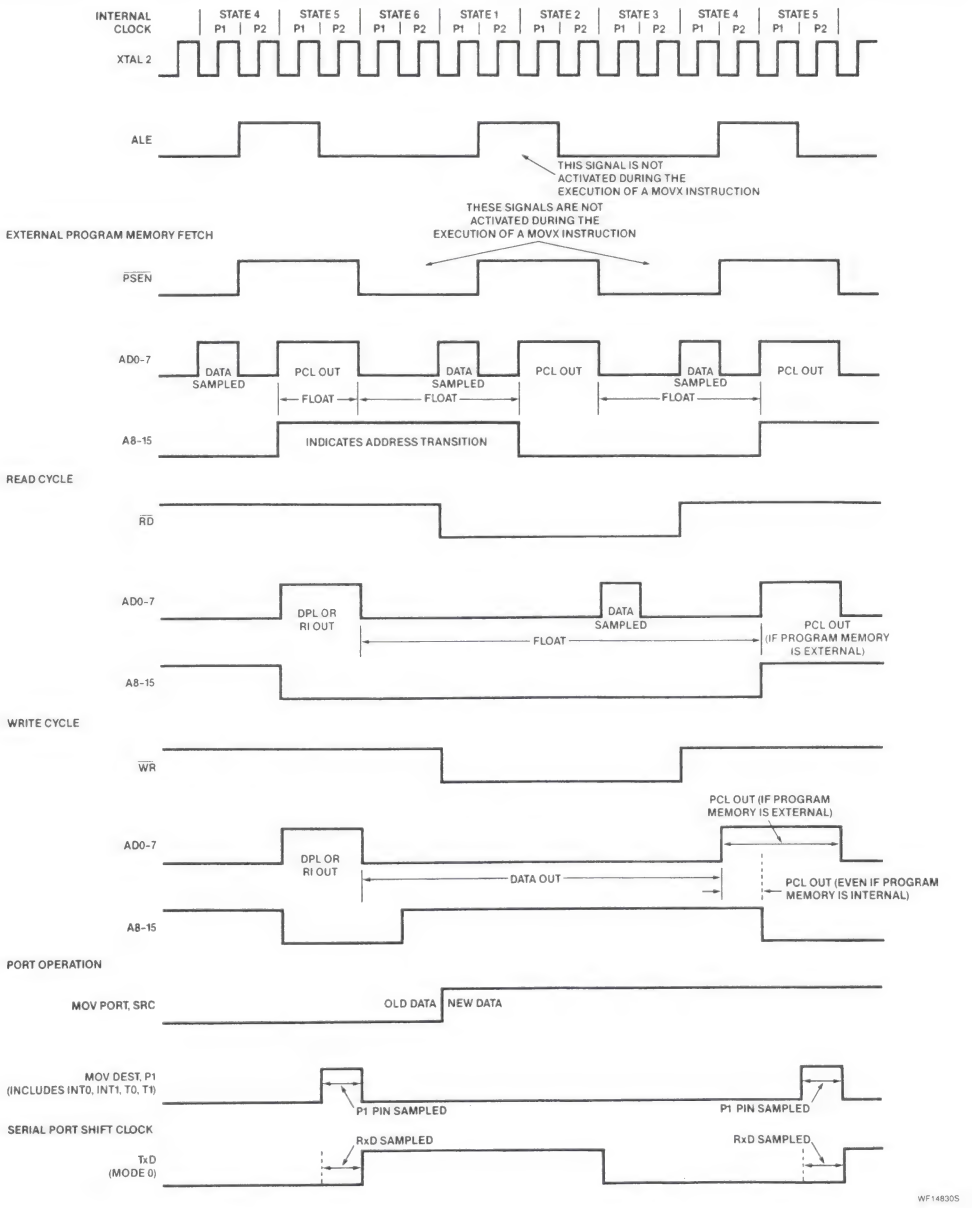



**Figure 11. IBF Flag Output Waveforms**




**NOTE:**
This diagram indicates when signals are clocked internally, however, the time it takes the signals to propagate to the pins ranges from 25ns to 125ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically ($T_A$ = 25°C, fully loaded), $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns; propagation delays for other signals are approximately 85ns. These timing delays are incorporated in the AC specifications.

**Figure 12. Timing Waveforms**

**Table 2. Instruction Set**

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Arithmetic operations** | | | | |
| ADD | A,Rn | Add register to accumulator | 1 | 1 |
| ADD | A,direct | Add direct byte to accumulator | 2 | 1 |
| ADD | A,@Ri | Add indirect RAM to accumulator | 1 | 1 |
| ADD | A,R#data | Add immediate data to accumulator | 2 | 1 |
| ADDC | A,Rn | Add register to accumulator with carry | 1 | 1 |
| ADDC | A,direct | Add direct byte to A with carry flag | 2 | 1 |
| ADDC | A,@Ri | Add indirect RAM to A with carry flag | 1 | 1 |
| ADDC | A,#data | Add immediate data to A with carry flag | 2 | 1 |
| SUBB | A,Rn | Subtract register from A with borrow | 1 | 1 |
| SUBB | A,direct | Subtract direct byte from A with borrow | 2 | 1 |
| SUBB | A,@Ri | Subtract indirect RAM from A w/borrow | 1 | 1 |
| SUBB | A,#data | Subtract immed. data from A w/borrow | 2 | 1 |
| INC | A | Increment accumulator | 1 | 1 |
| INC | Rn | Increment register | 1 | 1 |
| INC | direct | Increment direct byte | 2 | 1 |
| INC | @Ri | Increment indirect RAM | 1 | 1 |
| DEC | A | Decrement accumulator | 1 | 1 |
| DEC | Rn | Decrement register | 1 | 1 |
| DEC | direct | Decrement direct byte | 2 | 1 |
| DEC | @Ri | Decrement indirect RAM | 1 | 1 |
| INC | DPTR | Increment data pointer | 1 | 2 |
| MUL | AB | Multiply A & B | 1 | 4 |
| DIV | AB | Divide A by B | 1 | 4 |
| DA | A | Decimal adjust accumulator | 1 | 1 |
| **Logical operations** | | | | |
| ANL | A,Rn | AND register to accumulator | 1 | 1 |
| ANL | A,direct | AND direct byte to accumulator | 2 | 1 |
| ANL | A,@Ri | AND indirect RAM to accumulator | 1 | 1 |
| ANL | A,#data | AND immediate data to accumulator | 2 | 1 |
| ANL | direct,A | AND accumulator to direct byte | 2 | 1 |
| ANL | direct,#data | AND immediate data to direct byte | 3 | 2 |
| ORL | A,Rn | OR register to accumulator | 1 | 1 |
| ORL | A,direct | OR direct byte to accumulator | 2 | 1 |
| ORL | A,@Ri | OR indirect RAM to accumulator | 1 | 1 |
| ORL | A,#data | OR immediate data to accumulator | 2 | 1 |
| ORL | direct,A | OR accumulator to direct byte | 2 | 1 |
| ORL | direct,#data | OR immediate data to direct byte | 3 | 2 |
| XRL | A,Rn | Exclusive-OR register to accumulator | 1 | 1 |
| XRL | A,direct | Exclusive-OR direct byte to accumulator | 2 | 1 |
| XRL | A,@Ri | Exclusive-OR indirect RAM to A | 1 | 1 |
| XRL | A,#data | Exclusive-OR immediate data to A | 2 | 1 |
| XRL | direct,A | Exclusive-OR accumulator to direct byte | 2 | 1 |
| XRL | direct,#data | Exclusive-OR immediate data to direct | 3 | 2 |
| CLR | A | Clear accumulator | 1 | 1 |
| CPL | A | Complement accumulator | 1 | 1 |
| RL | A | Rotate accumulator left | 1 | 1 |
| RLC | A | Rotate A left through the carry flag | 1 | 1 |
| RR | A | Rotate accumulator right | 1 | 1 |
| RRC | A | Rotate A right through carry flag | 1 | 1 |
| SWAP | A | Swap nibbles within the accumulator | 1 | 1 |
| **Data transfer** | | | | |
| MOV | A,Rn | Move register to accumulator | 1 | 1 |
| MOV | A,direct | Move direct byte to accumulator | 2 | 1 |
| MOV | A,@Ri | Move indirect RAM to accumulator | 1 | 1 |
| MOV | A,#data | Move immediate data to accumulator | 2 | 1 |
| MOV | Rn,A | Move accumulator to register | 1 | 1 |
| MOV | Rn,direct | Move direct byte to register | 2 | 2 |
| MOV | Rn,#data | Move immediate data to register | 2 | 1 |
| MOV | direct,A | Move accumulator to direct byte | 2 | 1 |
| MOV | direct,Rn | Move register to direct byte | 2 | 2 |
| MOV | direct,direct | Move direct byte to direct | 3 | 2 |
| MOV | direct,@Ri | Move indirect RAM to direct byte | 2 | 2 |
| MOV | direct,#data | Move immediate data to direct byte | 3 | 2 |
| MOV | @Ri,A | Move accumulator to indirect RAM | 1 | 1 |
| MOV | @Ri,direct | Move direct byte to indirect RAM | 2 | 2 |

**Table 2. Instruction Set** (Continued)

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Data transfer (continued)** | | | | |
| MOV | @Ri,#data | Move immediate data to indirect RAM | 2 | 1 |
| MOV | DPTR,#data16 | Load data pointer with a 16-bit constant | 3 | 2 |
| MOVC | A,@A + DPTR | Move code byte relative to DPTR to A | 1 | 2 |
| MOVC | A,@A + PC | Move code byte relative to PC to A | 1 | 2 |
| MOVX | A,@Ri | Move external RAM (8-bit addr) to A | 1 | 2 |
| MOVX | A,@DPTR | Move external RAM (16-bit addr) to A | 1 | 2 |
| MOVX | @Ri,A | Move A to external RAM (8-bit addr) | 1 | 2 |
| MOVX | @DPTR,A | Move A to external RAM (16-bit addr) | 1 | 2 |
| PUSH | direct | Push direct byte onto stack | 2 | 2 |
| POP | direct | Pop direct byte from stack | 2 | 2 |
| XCH | A,Rn | Exchange register with accumulator | 1 | 1 |
| XCH | A,direct | Exchange direct byte with accumulator | 2 | 1 |
| XCH | A,@Ri | Exchange indirect RAM with A | 1 | 1 |
| XCHD | A,#Ri | Exchange low-order digit ind. RAM w/A | 1 | 1 |
| **Boolean variable manipulation** | | | | |
| CLR | C | Clear carry flag | 1 | 1 |
| CLR | bit | Clear direct bit | 2 | 1 |
| SETB | C | Set carry flag | 1 | 1 |
| SETB | bit | Set direct bit | 2 | 1 |
| CPL | C | Complement carry flag | 1 | 1 |
| CPL | bit | Complement direct bit | 2 | 1 |
| ANL | c,bit | AND direct bit to carry flag | 2 | 2 |
| ANL | c,/bit | AND complement of direct bit to carry | 2 | 2 |
| ORL | c,bit | OR direct bit to carry flag | 2 | 2 |
| ORL | c,/bit | OR complement of direct bit to carry | 2 | 2 |
| MOV | C,bit | Move direct bit to carry flag | 2 | 1 |
| MOV | bit,C | Move carry flag to direct bit | 2 | 2 |
| **Program and machine control** | | | | |
| ACALL | addr11 | Absolute subroutine call | 2 | 2 |
| LCALL | addr16 | Long subroutine call | 3 | 2 |
| RET | | Return from subroutine | 1 | 2 |
| RETI | | Return from interrupt | 1 | 2 |
| AJMP | addr11 | Absolute jump | 2 | 2 |
| LJMP | addr16 | Long jump | 3 | 2 |
| SJMP | rel | Short jump (relative addr) | 2 | 2 |
| JMP | @A + DPTR | Jump indirect relative to the DPTR | 1 | 2 |
| JZ | rel | Jump if accumulator is zero | 2 | 2 |
| JNZ | rel | Jump if accumulator is not zero | 2 | 2 |
| JC | rel | Jump if carry flag is set | 2 | 2 |
| JNC | rel | Jump if no carry flag | 2 | 2 |
| JB | bit,rel | Jump if direct bit set | 3 | 2 |
| JNB | bit,rel | Jump if direct bit not set | 3 | 2 |
| JBC | bit,rel | Jump if direct bit is set & clear bit | 3 | 2 |
| CJNE | A,direct,rel | Compare direct to A & jump if not equal | 3 | 2 |
| CJNE | A,#data,rel | Comp. immed. to A & jump if not equal | 3 | 2 |
| CJNE | Rn,#data,rel | Comp. immed. to reg. & jump if not equal | 3 | 2 |
| CJNE | @Ri,#data,rel | Comp. immed. to ind. & jump if not equal | 3 | 2 |
| DJNZ | Rn,rel | Decrement register & jump if not zero | 2 | 2 |
| DJNZ | direct,rel | Decrement direct & jump if not zero | 3 | 2 |
| NOP | | No operation | 1 | 1 |

**Notes on data addressing modes:**

Rn –Working register R0-R7

direct –128 internal RAM locations, any I/O port, control or status register

@Ri –Indirect internal RAM location addressed by register R0 or R1

#data –8-bit constant included in instruction

#data16 –16-bit constant included as bytes 2 & 3 of instruction

bit –128 software flags, any I/O pin, control or status bit

**Notes on program addressing modes:**

addr16 –Destination address for LCALL & LJMP may be anywhere within the 64-kilobyte program memory address space.

addr11 –Destination address for ACALL & AJMP will be within the same 2-kilobyte page of program memory as the first byte of the following instruction.

rel –SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127 – 128 bytes relative to first byte of the following instruction.

**Table 3. Instruction Opcodes in Hexadecimal Order**

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 00 | 1 | NOP | |
| 01 | 2 | AJMP | code addr |
| 02 | 3 | LJMP | code addr |
| 03 | 1 | RR | A |
| 04 | 1 | INC | A |
| 05 | 2 | INC | data addr |
| 06 | 1 | INC | @R0 |
| 07 | 1 | INC | @R1 |
| 08 | 1 | INC | R0 |
| 09 | 1 | INC | R1 |
| 0A | 1 | INC | R2 |
| 0B | 1 | INC | R3 |
| 0C | 1 | INC | R4 |
| 0D | 1 | INC | R5 |
| 0E | 1 | INC | R6 |
| 0F | 1 | INC | R7 |
| 10 | 3 | JBC | bit addr, code addr |
| 11 | 2 | ACALL | code addr |
| 12 | 3 | LCALL | code addr |
| 13 | 1 | RRC | A |
| 14 | 1 | DEC | A |
| 15 | 2 | DEC | data addr |
| 16 | 1 | DEC | @R0 |
| 17 | 1 | DEC | @R1 |
| 18 | 1 | DEC | R0 |
| 19 | 1 | DEC | R1 |
| 1A | 1 | DEC | R2 |
| 1B | 1 | DEC | R3 |
| 1C | 1 | DEC | R4 |
| 1D | 1 | DEC | R5 |
| 1E | 1 | DEC | R6 |
| 1F | 1 | DEC | R7 |
| 20 | 3 | JB | bit addr, code addr |
| 21 | 2 | AJMP | code addr |
| 22 | 1 | RET | |
| 23 | 1 | RL | A |
| 24 | 2 | ADD | A,#data |
| 25 | 2 | ADD | A,data addr |
| 26 | 1 | ADD | A,@R0 |
| 27 | 1 | ADD | A,@R1 |
| 28 | 1 | ADD | A,R0 |
| 29 | 1 | ADD | A,R1 |
| 2A | 1 | ADD | A,R2 |
| 2B | 1 | ADD | A,R3 |
| 2C | 1 | ADD | A,R4 |
| 2D | 1 | ADD | A,R5 |
| 2E | 1 | ADD | A,R6 |
| 2F | 1 | ADD | A,R7 |
| 30 | 3 | JNB | bit addr, code addr |
| 31 | 2 | ACALL | code addr |
| 32 | 1 | RETI | |
| 33 | 1 | RLC | A |
| 34 | 2 | ADDC | A,#data |
| 35 | 2 | ADDC | A,data addr |
| 36 | 1 | ADDC | A,@R0 |
| 37 | 1 | ADDC | A,@R1 |
| 38 | 1 | ADDC | A,R0 |
| 39 | 1 | ADDC | A,R1 |
| 3A | 1 | ADDC | A,R2, |
| 3B | 1 | ADDC | A,R3 |
| 3C | 1 | ADDC | A,R4 |
| 3D | 1 | ADDC | A,R5 |
| 3E | 1 | ADDC | A,R6 |
| 3F | 1 | ADDC | A,R7 |
| 40 | 2 | JC | code addr |
| 41 | 2 | AJMP | code addr |
| 42 | 2 | ORL | data addr,A |
| 43 | 3 | ORL | data addr,#data |
| 44 | 2 | ORL | A,#data |
| 45 | 2 | ORL | A,data addr |
| 46 | 1 | ORL | A,@R0 |
| 47 | 1 | ORL | A,@R1 |
| 48 | 1 | ORL | A,R0 |
| 49 | 1 | ORL | A,R1 |
| 4A | 1 | ORL | A,R2 |
| 4B | 1 | ORL | A,R3 |
| 4C | 1 | ORL | A,R4 |
| 4D | 1 | ORL | A,R5 |
| 4E | 1 | ORL | A,R6 |
| 4F | 1 | ORL | A,R7 |
| 50 | 2 | JNC | code addr |
| 51 | 2 | ACALL | code addr |
| 52 | 2 | ANL | data addr,A |
| 53 | 3 | ANL | data addr,#data |
| 54 | 2 | ANL | A,#data |
| 55 | 2 | ANL | A,data addr |
| 56 | 1 | ANL | A,@R0 |
| 57 | 1 | ANL | A,@R1 |
| 58 | 1 | ANL | A,R0 |
| 59 | 1 | ANL | A,R1 |
| 5A | 1 | ANL | A,R2 |
| 5B | 1 | ANL | A,R3 |
| 5C | 1 | ANL | A,R4 |
| 5D | 1 | ANL | A,R5 |
| 5E | 1 | ANL | A,R6 |
| 5F | 1 | ANL | A,R7 |
| 60 | 2 | JZ | code addr |
| 61 | 2 | AJMP | code addr |
| 62 | 2 | XRL | data addr,A |
| 63 | 3 | XRL | data addr,#data |
| 64 | 2 | XRL | A,#data |
| 65 | 2 | XRL | A,data addr |
| 66 | 1 | XRL | A,@R0 |
| 67 | 1 | XRL | A,@R1 |
| 68 | 1 | XRL | A,R0 |
| 69 | 1 | XRL | A,R1 |
| 6A | 1 | XRL | A,R2 |
| 6B | 1 | XRL | A,R3 |
| 6C | 1 | XRL | A,R4 |
| 6D | 1 | XRL | A,R5 |
| 6E | 1 | XRL | A,R6 |
| 6F | 1 | XRL | A,R7 |
| 70 | 2 | JNZ | code addr |
| 71 | 2 | ACALL | code addr |
| 72 | 2 | ORL | C,bit addr |
| 73 | 1 | JMP | @A + DPTR |
| 74 | 2 | MOV | A,#data |
| 75 | 3 | MOV | data addr,#data |
| 76 | 2 | MOV | @R0,#data |
| 77 | 2 | MOV | @R1,#data |
| 78 | 2 | MOV | R0,#data |
| 79 | 2 | MOV | R1,#data |
| 7A | 2 | MOV | R2,#data |
| 7B | 2 | MOV | R3,#data |
| 7C | 2 | MOV | R4,#data |
| 7D | 2 | MOV | R5,#data |
| 7E | 2 | MOV | R6,#data |
| 7F | 2 | MOV | R7,#data |

**Table 3. Instruction Opcodes in Hexadecimal Order** (Continued)

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 80 | 2 | SJMP | code addr |
| 81 | 2 | AJMP | code addr |
| 82 | 2 | ANL | C,bit addr |
| 83 | 1 | MOVC | A,@A + PC |
| 84 | 1 | DIV | AB |
| 85 | 3 | MOV | data addr,data addr |
| 86 | 2 | MOV | data addr,@R0 |
| 87 | 2 | MOV | data addr,@R1 |
| 88 | 2 | MOV | data addr,R0 |
| 89 | 2 | MOV | data addr,R1 |
| 8A | 2 | MOV | data addr,R2 |
| 8B | 2 | MOV | data addr,R3 |
| 8C | 2 | MOV | data addr,R4 |
| 8D | 2 | MOV | data addr,R5 |
| 8E | 2 | MOV | data addr,R6 |
| 8F | 2 | MOV | data addr,R7 |
| 90 | 3 | MOV | DPTR,#data |
| 91 | 2 | ACALL | code addr |
| 92 | 2 | MOV | bit addr,C |
| 93 | 1 | MOVC | A,@A + DPTR |
| 94 | 2 | SUBB | A,#data |
| 95 | 2 | SUBB | A,data addr |
| 96 | 1 | SUBB | A,@R0 |
| 97 | 1 | SUBB | A,@R1 |
| 98 | 1 | SUBB | A,R0 |
| 99 | 1 | SUBB | A,R1 |
| 9A | 1 | SUBB | A,R2 |
| 9B | 1 | SUBB | A,R3 |
| 9C | 1 | SUBB | A,R4 |
| 9D | 1 | SUBB | A,R5 |
| 9E | 1 | SUBB | A,R6 |
| 9F | 1 | SUBB | A,R7 |
| A0 | 2 | ORL | C,/bit addr |
| A1 | 2 | AJMP | code addr |
| A2 | 2 | MOV | C,bit addr |
| A3 | 1 | INC | DPTR |
| A4 | 1 | MUL | AB |
| A5 | | reserved | |
| A6 | 2 | MOV | @R0,data addr |
| A7 | 2 | MOV | @R1,data addr |
| A8 | 2 | MOV | R0,data addr |
| A9 | 2 | MOV | R1,data addr |
| AA | 2 | MOV | R2,data addr |
| AB | 2 | MOV | R3,data addr |
| AC | 2 | MOV | R4,data addr |
| AD | 2 | MOV | R5,data addr |
| AE | 2 | MOV | R6,data addr |
| AF | 2 | MOV | R7,data addr |
| B0 | 2 | ANL | C,/bit addr |
| B1 | 2 | ACALL | code addr |
| B2 | 2 | CPL | bit addr |
| B3 | 1 | CPL | C |
| B4 | 3 | CJNE | A,#data,code addr |
| B5 | 3 | CJNE | A,data addr,code addr |
| B6 | 3 | CJNE | @R0,#data,code addr |
| B7 | 3 | CJNE | @R1,#data,code addr |
| B8 | 3 | CJNE | R0,#data,code addr |
| B9 | 3 | CJNE | R1,#data,code addr |
| BA | 3 | CJNE | R2,#data,code addr |
| BB | 3 | CJNE | R3,#data,code addr |
| BC | 3 | CJNE | R4,#data,code addr |
| BD | 3 | CJNE | R5#data,code addr |
| BE | 3 | CJNE | R6,#data,code addr |
| BF | 3 | CJNE | R7,#data,code addr |
| C0 | 2 | PUSH | data addr |
| C1 | 2 | AJMP | code addr |
| C2 | 2 | CLR | bit addr |
| C3 | 1 | CLR | C |
| C4 | 1 | SWAP | A |
| C5 | 2 | XCH | A,data addr |
| C6 | 1 | XCH | A,@R0 |
| C7 | 1 | XCH | A,@R1 |
| C8 | 1 | XCH | A,R0 |
| C9 | 1 | XCH | A,R1 |
| CA | 1 | XCH | A,R2 |
| CB | 1 | XCH | A,R3 |
| CC | 1 | XCH | A,R4 |
| CD | 1 | XCH | A,R5 |
| CE | 1 | XCH | A,R6 |
| CF | 1 | XCH | A,R7 |
| D0 | 2 | POP | data addr |
| D1 | 2 | ACALL | code addr |
| D2 | 2 | SETB | bit addr |
| D3 | 1 | SETB | C |
| D4 | 1 | DA | A |
| D5 | 3 | DJNZ | data addr,code addr |
| D6 | 1 | XCHD | A,@R0 |
| D7 | 1 | XCHD | A,@R1 |
| D8 | 2 | DJNZ | R0,code addr |
| D9 | 2 | DJNZ | R1,code addr |
| DA | 2 | DJNZ | R2,code addr |
| DB | 2 | DJNZ | R3,code addr |
| DC | 2 | DJNZ | R4,code addr |
| DD | 2 | DJNZ | R5,code addr |
| DE | 2 | DJNZ | R6,code addr |
| DF | 2 | DJNZ | R7,code addr |
| E0 | 1 | MOVX | A,@ DPTR |
| E1 | 2 | AJMP | code addr |
| E2 | 1 | MOVX | A,@R0 |
| E3 | 1 | MOVX | A,@R1 |
| E4 | 1 | CLR | A |
| E5 | 2 | MOV | A,.data addr |
| E6 | 1 | MOV | A,@R0 |
| E7 | 1 | MOV | A,@R1 |
| E8 | 1 | MOV | A,R0 |
| E9 | 1 | MOV | A,R1 |
| EA | 1 | MOV | A,R2 |
| EB | 1 | MOV | A,R3 |
| EC | 1 | MOV | A,R4 |
| ED | 1 | MOV | A,R5 |
| EE | 1 | MOV | A,R6 |
| EF | 1 | MOVX | A,R7 |
| F0 | 1 | MOVX | @ DPTR,A |
| F1 | 2 | ACALL | code addr |
| F2 | 1 | MOVX | @R0,A |
| F3 | 1 | MOVX | @R1,A |
| F4 | 1 | CPL | A |
| F5 | 2 | MOV | data addr,A |
| F6 | 1 | MOV | @R0,A |
| F7 | 1 | MOV | @R1,A |
| F8 | 1 | MOV | R0,A |
| F9 | 1 | MOV | R1,A |
| FA | 1 | MOV | R2,A |
| FB | 1 | MOV | R3,A |
| FC | 1 | MOV | R4,A |
| FD | 1 | MOV | R5,A |
| FE | 1 | MOV | R6,A |
| FF | 1 | MOV | R7,A |

Signetics

# 83C552/80C552

## Single-Chip 8-Bit Microcontroller With A/D, Capture/Compare Timer, With High-Speed Outputs, PWM

*Objective Specification*

**Military**
**Customer Specific Products**

### DESCRIPTION

The 83C552/80C552 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C552/80C552 has the same instruction set as the 80C51. Two versions of the derivative exist.

- 83C552 — 8K bytes mask programmable ROM
- 80C552 - ROMless version of the 83C552

The 83C552 contains a non-volatile 8K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a 'watchdog' timer and on-chip oscillator and timing circuits.

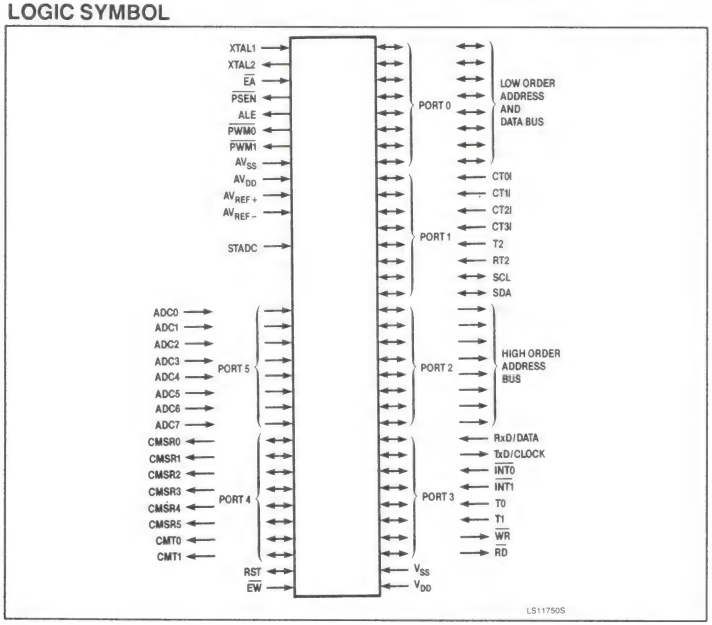
For systems that require extra capability, the 83C552 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1µs and 40% in 2µs. Multiply and divide instructions require 4µs.

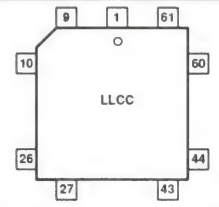
### FEATURES

- **80C51B central processing unit**
- **8K x 8 ROM (83C552), expandable externally to 64K bytes**
- **256 x 8 RAM, expandable externally to 64K bytes**
- **Two standard 16-bit timer/counters**
- **An additional 16-bit timer/counter coupled to four capture registers and three compare registers**
- **Capable of producing 8 synchronized, timed outputs**
- **A 10-bit ADC with 8 multiplexed analog inputs**
- **Two 8-bit resolution, pulse width modulation outputs**
- **Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs**
- **I²C-bus serial I/O port with byte oriented master and slave functions**
- **Full-duplex UART compatible with the standard 80C51**
- **On-chip watchdog timer**

### LOGIC SYMBOL




### PIN CONFIGURATION




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | P5.0/ADC0 | 35 | XTAL1 |
| 2 | $V_{DD}$ | 36 | $V_{SS}$ |
| 3 | STADC | 37 | $V_{SS}$ |
| 4 | $\overline{PWM0}$ | 38 | NC |
| 5 | $\overline{PWM1}$ | 39 | P2.0/A08 |
| 6 | $\overline{EW}$ | 40 | P2.1/A09 |
| 7 | P4.0/CMSR0 | 41 | P2.2/A10 |
| 8 | P4.1/CMRS1 | 42 | P2.3/A11 |
| 9 | P4.2CMSR2 | 43 | P2.4/A12 |
| 10 | P4.3/CMSR3 | 44 | P2.5/A13 |
| 11 | P4.4/CMSR4 | 45 | P2.6/A14 |
| 12 | P4.5/CMSR5 | 45 | P2.7/A15 |
| 13 | P4.6/CMT0 | 47 | $\overline{PSEN}$ |
| 14 | P4.7/CMT1 | 48 | ALE |
| 15 | RST | 49 | $\overline{EA}$ |
| 15 | P1.0/CT0I | 50 | P0.7/AD7 |
| 17 | P1.1/CT1I | 51 | P0.6/AD6 |
| 18 | P1.2/CT2I | 52 | P0.5/AD5 |
| 19 | P1.3/CT3I | 53 | P0.4/AD4 |
| 20 | P1.4/T2 | 54 | P0.3/AD3 |
| 21 | P1.5/RT2 | 55 | P0.2/AD2 |
| 22 | P1.6/SCL | 56 | P0.1/AD1 |
| 23 | P1.7/SDA | 57 | P0.0/AD0 |
| 24 | P3.0/RxD | 58 | $AV_{ref-}$ |
| 25 | P3.1TxD | 59 | $AV_{ref+}$ |
| 26 | P3.2/$\overline{INT0}$ | 60 | $AV_{SS}$ |
| 27 | P3.3/$\overline{INT1}$ | 61 | $AV_{DD}$ |
| 28 | P3.4/T0 | 62 | P5.7/ADC7 |
| 29 | P3.5/T1 | 63 | P5.6/ADC6 |
| 30 | P3.6/$\overline{WR}$ | 64 | P5.5/ADC5 |
| 31 | P3.7/$\overline{RD}$ | 65 | P5.4/ADC4 |
| 32 | NC | 66 | P5.3/ADC3 |
| 33 | NC | 67 | P5.2/ADC2 |
| 34 | XTAL2 | 68 | P5.1/ADC1 |

Signetics

# 83C751
## CMOS Single-Chip 8-Bit Microcontroller

*Objective Specification*

**Military Microprocessor Products**

## DESCRIPTION

The Signetics 83C751 offers many of the advantages of the 80C51 architecture in a small package and at low cost.

The Signetics 83C751 microcontroller is fabricated with Signetics high-density CMOS technology. Signetics epitaxial substrate minimizes CMOS latch-up sensitivity.

The 83C751 contains a 2K x 8 ROM; a 64 x 8 RAM; 19 I/O lines, a 16-bit counter/timer, a fixed-rate timer, a five-source, fixed-priority interrupt structure, a bidirectional Inter-Integrated Circuit ($I^2C$) serial bus interface, and an on-chip oscillator.

The onboard Inter-Integrated Circuit ($I^2C$) bus interface allows the 83C751 to operate as a master or slave device on the $I^2C$ small area network. This capability facilitates I/O and RAM expansion, access to EPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated $I^2C$ peripherals.

## FEATURES

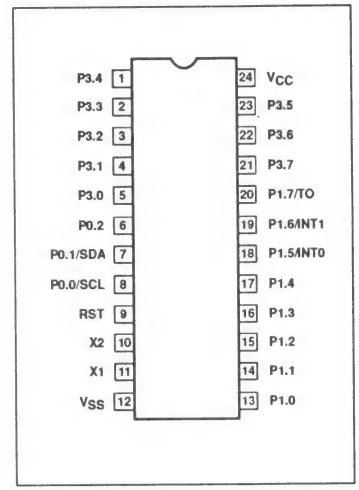
- **80C51 based architecture**
- **Inter-Integrated Circuit ($I^2C$) serial bus interface**
- **Small package sizes**
  - **24-pin DIP (300mil "skinny DIP")**
- **Wide power supply voltage range**
- **Wide oscillator frequency range**
- **Low power consumption:**
  - **Normal operation: less than 24mA @ 5V, 12MHz**
  - **Idle mode**
  - **Power down mode**
- **2K X 8 ROM, 64 X 8 RAM**
- **16-bit counter/timer**
- **Fixed-rate timer**
- **Boolean processor**
- **CMOS and TTL compatible**

## ORDERING INFORMATION

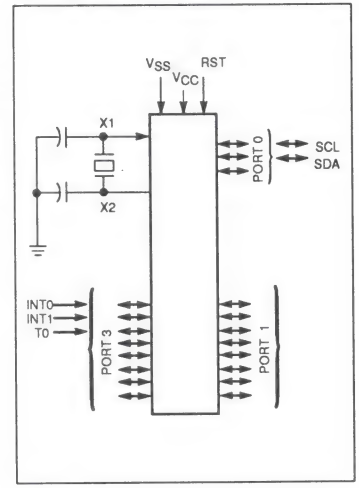
| PACKAGE | ORDER CODE |
|---|---|
| 24-Pin Ceramic DIP 300mil-wide | 83C751/BLA* |

* Factory will assign a customer unique CVXXXX number for ROM coding.

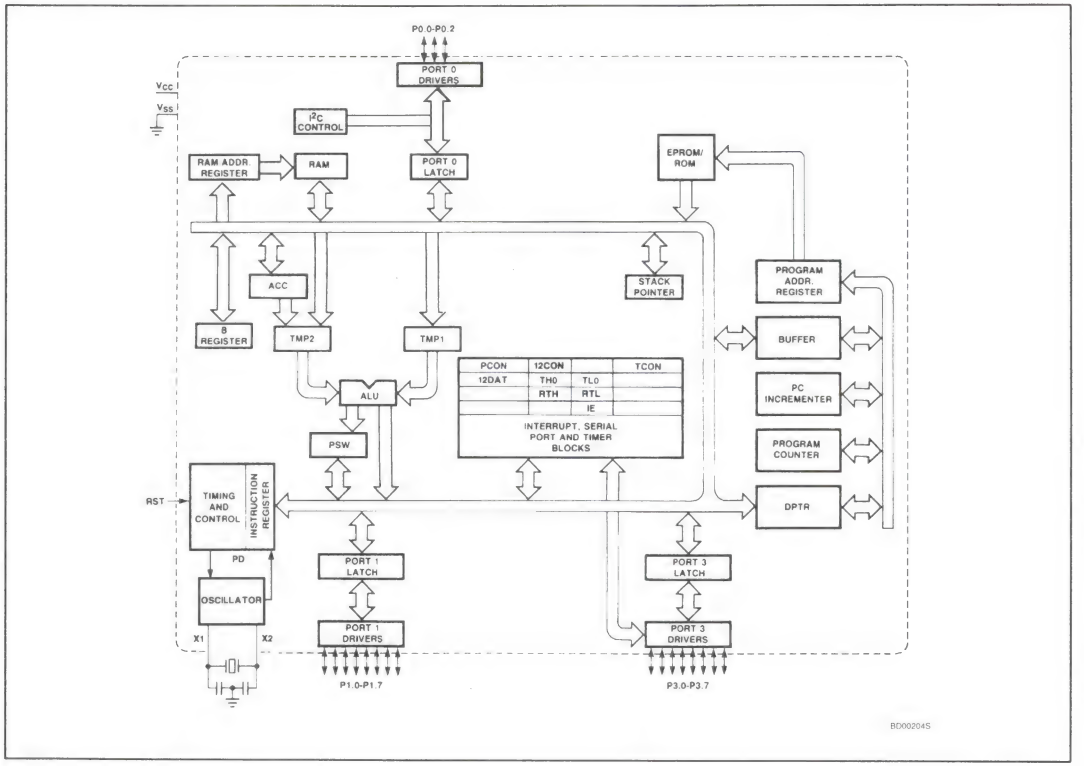
## PIN CONFIGURATION




## LOGIC SYMBOL



## BLOCK DIAGRAM



## PIN DESCRIPTION

| MNEMONIC | PIN NO. | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| $V_{SS}$ | 12 | I | **Ground:** Circuit ground potential. |
| $V_{CC}$ | 24 | I | **Power Supply:** Supply voltage during normal, and power down operation. |
| P0.0–P0.2 | 8–6 | I/O | **Port 0:** Port 0 is a 3–bit open–drain bidirectional port. Port 0 pins that have 1s written to them float, and in that state can be used as high–impedance inputs.<br>Port 0 also serves as the serial $I^2C$ interface, as shown in the pinout diagram. When this feature is activated by software, SCL and SDA are driven Low in accordance with the $I^2C$ protocol. These pins are driven Low if the port register bit is written as 0 or if the $I^2C$ subsystem presents a 0. The state of the pin can always be read from the port register by the program.<br>To comply with the $I^2C$ specification, P0.0 and P0.1 are open–drain bidirectional I/O pins with the electrical characteristics listed in the tables that follow. While these differ from 'standard TTL' characteristics they are close enough for the pins to still be used as general–purpose I/Os in non–$I^2C$ applications. |
| | 7 | I/O | SDA (P0.1) $I^2C$ data. |
| | 8 | I/O | SCL (P0.0) $I^2C$ clock. |
| P1.0–P1.7 | 13–20 | I/O | **Port 1:** Port 1 is an 8–bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1's written to them are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled Low will source current because of the internal pull-ups. (See DC Electrical Characteristic: $I_{IL}$). Port 1 also serves the special feature functions of the 80C51 family, as listed below: |
| | 18 | | $\overline{INT0}$ (P1.5): External interrupt. |
| | 19 | | $\overline{INT1}$ (P1.6): External interrupt. |
| | 20 | | T0 (P1.7): Timer 0 external input. |
| P3.0–P3.7 | 5–1, 23–21 | I/O | **Port 3:** Port 3 is an 8–bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled Low will source current because of the pull-ups. (See DC Electrical Characteristic: $I_{IL}$) |
| RST | 9 | I | **Reset:** A High on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power–on reset using only an external capacitor to $V_{CC}$. |
| X1 | 11 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| X2 | 10 | O | **Crystal 2:** Output from the inverting oscillator amplifier. |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Operating ambient temperature range | –55 to +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| | Voltage from $V_{CC}$ to $V_{SS}$[2] | –0.5 to +6.5 | V |
| | Voltage from any pin to $V_{SS}$[2] | –0.5 to $V_{CC}$ +0.5 | V |
| $P_D$ | Power dissipation | +1.0 | W |

## MAXIMUM $I_{CC}$ (mA)[9]

| FREQUENCY $V_{CC}$ | OPERATING[6] | | | IDLE[8] | | |
|---|---|---|---|---|---|---|
| | 4V | 5V | 6V | 4V | 5V | 6V |
| 0.5MHz | 1.6 | 2.2 | 3 | 0.6 | 0.9 | 1.2 |
| 3.5MHz | 4.3 | 5.7 | 7.5 | 1.1 | 1.6 | 2.2 |
| 8.0MHz | 8.3 | 11 | 14 | 1.8 | 2.7 | 3.7 |
| 12MHz | 12 | 16 | 20 | 2.5 | 3.7 | 5.0 |

# CMOS Single-Chip 8-Bit Microcontroller — 83C751

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.0V \le V_{CC} \le 6.0V$, $V_{SS} = OV$[3]

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IL}$ | Input Low voltage | | –0.5 | 0.2 $V_{CC}$ – 0.25 | V |
| $V_{IH}$ | Input High voltage, except X1, RST | | 0.2 $V_{CC}$ +.1.1 | $V_{CC}$ +0.5 | V |
| $V_{IH1}$ | Input High voltage, X1, RST | | 0.7 $V_{CC}$ + 0.2 | $V_{CC}$ +0.5 | V |
| | Port 0.0 and 0.1 ($I^2C$) – Receivers: | | | | |
| $V_{IL}$ | Input Low voltage | | | 0.3 X $V_{CC}$ | V |
| | | | 0.7 X $V_{CC}$ | 1.5 | V |
| $V_{IH}$ | Input High voltage | $V_{CC}$ = 5V | 3.5 | | V |
| | | | | | V |
| $V_{TH+}$ – $V_{TH-}$ | Hysteresis | $V_{CC}$ = 5V | 200 | | mV |
| $V_{OL}$ | Output Low voltage, Ports 1 & 3[4] | $I_{OL}$ = 1.6mA | | 0.45 | V |
| $V_{OL1}$ | Output Low voltage, Port 0.2[4] | $I_{OL}$ = 3.2mA | | 0.45 | V |
| $V_{OH}$ | Output High voltage, Ports 1 & 3 | $I_{OH}$ = –60µA | 2.4 | | V |
| | $V_{CC}$ = 5V ± 10% | $I_{OH}$ = –25µA | 0.75$V_{CC}$ | | V |
| | | $I_{OH}$ = –10µA | 0.9$V_{CC}$ | | V |
| | Port 0.0 and 0.1 ($I^2C$) – Drivers: | | | | |
| $V_{OL}$ | Output Low voltage | $I_{OL}$ = 3mA | | 0.4 | V |
| | Driver, receiver combined: | (over $V_{CC}$ range) | | | |
| $I_{IL}$ | Input Low current | V = 0.4 | | –10 | µA |
| $I_{IH}$ | Input High current | V = 0.9 X $V_{CC}$ | | 10 | µA |
| $C_{IO}$ | Capacitance[7] | | | 10 | pF |
| $I_{IL}$ | Logical 0 input current, Ports 1 & 3 | $V_{IN}$ = 0.45V | | –75 | µA |
| $I_{TL}$ | Logical 1 to 0 transition current, Ports 1 & 3 | $V_{IN}$ = 2V | | –750 | µA |
| $I_{LI}$ | Input leakage current, Port 0 | 0.45V < $V_{IN}$ < $V_{CC}$ | | ± 10 | µA |
| $R_{RST}$ | Reset pulldown resistor | | 50 | 150 | kΩ |
| $C_{IO}$ | Pin capacitance[7] | Test freq= 1MHz, $T_A$ = 25°C | | 10 | pF |
| $I_{PD}$ | Power–down current[6] | $V_{CC}$ = 2V to 6V | | 75 | µA |

## AC ELECTRICAL CHARACTERISTICS[10] $-55°C \le T_A \le +125°C$, $4V \le V_{CC} \le 6V$, $V_{SS} = OV$[3]

| SYMBOL | PARAMETER | 12MHz CLOCK | | VARIABLE CLOCK | | UNIT |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator frequency | | | 3.5 | 12 | MHz |
| | External clock (Figure 1) | | | | | |
| $t_{CHCX}$ | High time | 20 | | | | ns |
| $t_{CLCX}$ | Low time | 20 | | | | ns |
| $t_{CLCH}$ | Rise time | | 20 | | | ns |
| $t_{CHCL}$ | Fall time | | 20 | | | ns |

## AC SYMBOL DESIGNATIONS

Each timing symbol has five characters. The first character is always a "t" (t = time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

C = Clock
D = Input data
H = Logic level High
L = Logic level Low
Q = Output data
T = Time
V = Valid
X = No longer a valid logic level
Z = Float

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages with respect to $V_{SS}$ unless otherwise noted.
4. Capacitive loading on ports 0 and 2 can cause spurious noise pulses to be superimposed on the $V_{OLS}$ of ports 1 and 3. The noise is caused by external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1–to–0 transitions during bus operations.
5. Power down $I_{CC}$ is measured with all output pins disconnected; port 0 = $V_{CC}$; X2 n.c.; RST = $V_{SS}$.
6. $I_{CC}$ is measured with all output pins disconnected; X1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL}$ = $V_{SS}$ + 0.5V, $V_{IH}$ = $V_{CC}$ –0.5V; X2 n.c.; RST = port 0 = $V_{CC}$, $I_{CC}$ will be slightly higher if a crystal oscillator is used.
7. $C_{IO}$ is tested initially and after any design or process change which may effect capacitance.
8. Idle $I_{CC}$ is measured with all output pins disconnected: X1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL}$ = $V_{SS}$ + 0.5V, $V_{IH}$ = $V_{CC}$ – 0.5V; X2 n.c.; port 0 = $V_{CC}$; RST = $V_{SS}$.
9. Typical operating $I_{CC}$ at 3MHz and $V_{CC}$ = 5.0V is 3.8mA, and varies with frequency at the rate of 0.67mA/MHz.
10. Load capacitance for ports = 80pF.

## OSCILLATOR CHARACTERISTICS

X1 and X2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on–chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, X1 should be driven while X2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide–by–two flip–flop. However, minimum and maximum High and Low times specified in the data sheet must be observed.

## IDLE MODE

In the idle mode, the CPU puts itself to sleep while all the on–chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on–chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power–on reset.

## POWER–DOWN MODE

In the power–down mode, the oscillator is stopped, and the instruction to invoke power–down is the last instruction executed. Only the contents of the on–chip RAM are preserved. A hardware reset is the only way to terminate the power–down mode. The control bits for the reduced power modes are in the special function register PCON.

## DESIGN CONSIDERATIONS

At power–down, the voltage on $V_{CC}$ and RST must come up at the same time for a proper start–up.

Before entering the power–down mode, the contents of the carry bit and B.7 must be equal. (See Table 1.)

### Table 1. External Pin Status During Idle and Power Down Modes

| MODE | PORT0 | PORT1 | PORT3 |
|---|---|---|---|
| Idle | Data | Data | Data |
| Power–down | Data | Data | Data |

## Differences Between the 83C751 and the 80C51

**Program Memory**

On the 83C751, program memory is 2048 bytes long and is not externally expandable. Program memory can contain 83C751 instructions and constant data. The only fixed allocations in program memory are the addresses at which execution is taken up in response to reset and to interrupts, which are as follows:

| Event | Program Memory Address |
|---|---|
| Reset | 000 |
| External INT0 | 003 |
| Counter/Timer 0 | 00B |
| External INT1 | 013 |
| Timer I | 01B |
| $I^2C$ Serial | 023 |

**Counter/Timer Subsystem**

The 83C751 has one counter/timer called timer/counter 0. Its operation is similar to mode 2 operation on the 80C51, extended to 16 bits. The controls for this counter are centralized in a single register called TCON.

A watchdog timer, called Timer I, is for use with the $I^2C$ subsystem. In $I^2C$ applications, this timer is dedicated to time–generation and bus monitoring of the $I^2C$. In non–$I^2C$ applications, it is available for use as a fixed time base.

**Interrupt Subsystem — Fixed Priority**

The IP register and the 2–level interrupt system of the 80C51 are eliminated. Simultaneous interrupt conditions are resolved by a single–level, fixed priority as follows:

| | |
|---|---|
| Highest priority: | Pin INT0 |
| | Counter/Timer flag 0 |
| | Pin INT1 |
| | Timer I |
| Lowest priority: | Serial $I^2C$ |

**Serial Communications**

The 83C751 contains an $I^2C$ serial communications port instead of the 80C51 UART. The $I^2C$ serial port is a single bit hardware necessary to support multimaster and slave operations. Also included are receiver digital filters and timer (timer I) for communication watchdog purposes. The $I^2C$ serial port is controlled through three special function registers; $I^2C$ control, $I^2C$ data and $I^2C$ configuration.

**Special Function Register Address**

Special function register addresses for the 83C751 are identical to those of the 80C51, except for the additional registers listed in Table 2.

80C51 special function registers not present in the 83C751 are TMOD (89), P2 (A0) and IP (B8). The 80C51 registers TH1, TL1 SCON and SBUF are replaced with the 83C751 registers RTH, RTL I2CON and I2DAT, respectively.

### Table 2. Special Function Register Addresses

| REGISTER ADDRESS | | | BIT ADDRESS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Name | Symbol | Address | MSB | | | | | | | LSB |
| $I^2C$ control | I2CON | 98 | 9F | 9E | 9D | 9C | 9B | 9A | 99 | 98 |
| $I^2C$ data | I2DAT | 99 | – | – | – | – | – | – | – | – |
| $I^2C$ configuration | I2CFG | D8 | DF | DE | DD | DC | DB | DA | D9 | D8 |

# CMOS Single-Chip 8-Bit Microcontroller

# 83C751

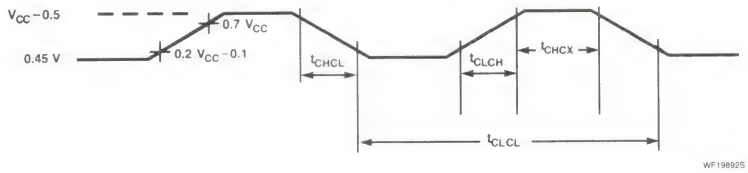



**Figure 1. External Clock Drive Waveform**

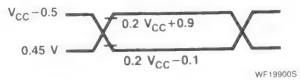



**Figure 2. AC Testing Input/Output Waveform**

## INSTRUCTION SET

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Arithmetic operations** | | | | |
| ADD | A,Rn | Add register to accumulator | 1 | 1 |
| ADD | A,direct | Add direct byte to accumulator | 2 | 1 |
| ADD | A,@Ri | Add indirect RAM to accumulator | 1 | 1 |
| ADD | A,R#data | Add immediate data to accumulator | 2 | 1 |
| ADDC | A,Rn | Add register to accumulator with carry | 1 | 1 |
| ADDC | A,direct | Add direct byte to A with carry flag | 2 | 1 |
| ADDC | A,@Ri | Add indirect RAM to A with carry flag | 1 | 1 |
| ADDC | A,#data | Add immediate data to A with carry flag | 2 | 1 |
| SUBB | A,Rn | Subtract register from A with borrow | 1 | 1 |
| SUBB | A,direct | Subtract direct byte from A with borrow | 2 | 1 |
| SUBB | A,@Ri | Subtract indirect RAM from A w/borrow | 1 | 1 |
| SUBB | A,#data | Subtract immed. data from A w/borrow | 2 | 1 |
| INC | A | Increment accumulator | 1 | 1 |
| INC | Rn | Increment register | 1 | 1 |
| INC | direct | Increment direct byte | 2 | 1 |
| INC | @Ri | Increment indirect RAM | 1 | 1 |
| DEC | A | Decrement accumulator | 1 | 1 |
| DEC | Rn | Decrement register | 1 | 1 |
| DEC | direct | Decrement direct byte | 2 | 1 |
| DEC | @Ri | Decrement indirect RAM | 1 | 1 |
| INC | DPTR | Increment data pointer | 1 | 2 |
| MUL | AB | Multiply A & B | 1 | 4 |
| DIV | AB | Divide A by B | 1 | 4 |
| DA | A | Decimal adjust accumulator | 1 | 1 |
| **Logical operations** | | | | |
| ANL | A,Rn | AND register to accumulator | 1 | 1 |
| ANL | A,direct | AND direct byte to accumulator | 2 | 1 |
| ANL | A,@Ri | AND indirect RAM to accumulator | 1 | 1 |
| ANL | A,#data | AND immediate data to accumulator | 2 | 1 |
| ANL | direct,A | AND accumulator to direct byte | 2 | 1 |
| ANL | direct,#data | AND immediate data to direct byte | 3 | 2 |
| ORL | A,Rn | OR register to accumulator | 1 | 1 |
| ORL | A,direct | OR direct byte to accumulator | 2 | 1 |
| ORL | A,@Ri | OR indirect RAM to accumulator | 1 | 1 |
| ORL | A,#data | OR immediate data to accumulator | 2 | 1 |
| ORL | direct,A | OR accumulator to direct byte | 2 | 1 |
| ORL | direct,#data | OR immediate data to direct byte | 3 | 2 |
| XRL | A,Rn | Exclusive–OR register to accumulator | 1 | 1 |
| XRL | A,direct | Exclusive–OR direct byte to accumulator | 2 | 1 |
| XRL | A,@Ri | Exclusive–OR indirect RAM to A | 1 | 1 |
| XRL | A,#data | Exclusive–OR immediate data to A | 2 | 1 |
| XRL | direct,A | Exclusive–OR accumulator to direct byte | 2 | 1 |
| XRL | direct,#data | Exclusive–OR immediate data to direct | 3 | 2 |
| CLR | A | Clear accumulator | 1 | 1 |
| CPL | A | Complement accumulator | 1 | 1 |
| RL | A | Rotate accumulator left | 1 | 1 |
| RLC | A | Rotate A left through the carry flag | 1 | 1 |
| RR | A | Rotate accumulator right | 1 | 1 |
| RRC | A | Rotate A right through carry flag | 1 | 1 |
| SWAP | A | Swap nibbles within the accumulator | 1 | 1 |
| **Data transfer** | | | | |
| MOV | A,Rn | Move register to accumulator | 1 | 1 |
| MOV | A,direct | Move direct byte to accumulator | 2 | 1 |
| MOV | A,@Ri | Move indirect RAM to accumulator | 1 | 1 |
| MOV | A,#data | Move immediate data to accumulator | 2 | 1 |
| MOV | Rn,A | Move accumulator to register | 1 | 1 |
| MOV | Rn,direct | Move direct byte to register | 2 | 2 |
| MOV | Rn,#data | Move immediate data to register | 2 | 1 |
| MOV | direct,A | Move accumulator to direct byte | 2 | 1 |
| MOV | direct,Rn | Move register to direct byte | 2 | 2 |
| MOV | direct,direct | Move direct byte to direct | 3 | 2 |
| MOV | direct,@Ri | Move indirect RAM to direct byte | 2 | 2 |
| MOV | direct,#data | Move immediate data to direct byte | 3 | 2 |
| MOV | @Ri,A | Move accumulator to indirect RAM | 1 | 1 |
| MOV | @Ri,direct | Move direct byte to indirect RAM | 2 | 2 |

# CMOS Single-Chip 8-Bit Microcontroller — 83C751

## Instruction Set (Continued)

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Data transfer (continued)** | | | | |
| MOV | @Ri,#data | Move immediate data to indirect RAM | 2 | 1 |
| MOV | DPTR,#data16 | Load data pointer with a 16–bit constant | 3 | 2 |
| MOVC | A,@A + DPTR | Move code byte relative to DPTR to A | 1 | 2 |
| MOVC | A,@A + PC | Move code byte relative to PC to A | 1 | 2 |
| PUSH | direct | Push direct byte onto stack | 2 | 2 |
| POP | direct | Pop direct byte from stack | 2 | 2 |
| XCH | A,Rn | Exchange register with accumulator | 1 | 1 |
| XCH | A,direct | Exchange direct byte with accumulator | 2 | 1 |
| XCH | A,@Ri | Exchange indirect RAM with A | 1 | 1 |
| XCHD | A,@Ri | Exchange low–order digit ind. RAM w/A | 1 | 1 |
| **Boolean variable manipulation** | | | | |
| CLR | C | Clear carry flag | 1 | 1 |
| CLR | bit | Clear direct bit | 2 | 1 |
| SETB | C | Set carry flag | 1 | 1 |
| SETB | bit | Set direct bit | 2 | 1 |
| CPL | C | Complement carry flag | 1 | 1 |
| CPL | bit | Complement direct bit | 2 | 1 |
| ANL | C,bit | AND direct bit to carry flag | 2 | 2 |
| ANL | C,/bit | AND complement of direct bit to carry | 2 | 2 |
| ORL | C,bit | OR direct bit to carry flag | 2 | 2 |
| ORL | C,/bit | OR complement of direct bit to carry | 2 | 2 |
| MOV | C,bit | Move direct bit to carry flag | 2 | 1 |
| MOV | bit,C | Move carry flag to direct bit | 2 | 2 |
| **Program and machine control** | | | | |
| ACALL | addr11 | Absolute subroutine call | 2 | 2 |
| RET | | Return from subroutine | 1 | 2 |
| RETI | | Return from interrupt | 1 | 2 |
| AJMP | addr11 | Absolute jump | 2 | 2 |
| LJMP* | addr16 | Long jump | 3 | 2 |
| SJMP | rel | Short jump (relative addr) | 2 | 2 |
| JMP | @A + DPTR | Jump indirect relative to the DPTR | 1 | 2 |
| JZ | rel | Jump if accumulator is zero | 2 | 2 |
| JNZ | rel | Jump if accumulator is not zero | 2 | 2 |
| JC | rel | Jump if carry flag is set | 2 | 2 |
| JNC | rel | Jump if no carry flag | 2 | 2 |
| JB | bit,rel | Jump if direct bit set | 3 | 2 |
| JNB | bit,rel | Jump if direct bit not set | 3 | 2 |
| JBC | bit,rel | Jump if direct bit is set & clear bit | 3 | 2 |
| CJNE | A,direct,rel | Compare direct to A & jump if not equal | 3 | 2 |
| CJNE | A,#data,rel | Comp. immed. to A & jump if not equal | 3 | 2 |
| CJNE | Rn,#data,rel | Comp. immed. to reg. & jump if not equal | 3 | 2 |
| CJNE | @Ri,#data,rel | Comp. immed. to ind. & jump if not equal | 3 | 2 |
| DJNZ | Rn,rel | Decrement register & jump if not zero | 2 | 2 |
| DJNZ | direct,rel | Decrement direct & jump if not zero | 3 | 2 |
| NOP | | No operation | 1 | 1 |

**Notes on data addressing modes:**

Rn –Working register R0–R7
direct –64 internal RAM locations, any I/O port, control or status register
@Ri –Indirect internal RAM location addressed by register R0 or R1
#data –8–bit constant included in instruction
#data16 –16–bit constant included as bytes 2 & 3 of instruction
bit –128 software flags, any I/O pin, control or status bit

**Notes on program addressing modes:**

addr16 –Destination address for LJMP. Only eleven bits of this 16–bit field are used.
addr11 –Destination address for ACALL & AJMP will be within the same 2–kilobyte page of program memory as the first byte of the following instruction.
rel –SJMP and all conditional jumps include an 8–bit offset byte. Range is + 127 – 128 bytes relative to first byte of the following instruction.

## INSTRUCTION OPCODES IN HEXADECIMAL ORDER

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 00 | 1 | NOP | |
| 01 | 2 | AJMP | code addr |
| 02 | 3 | LJMP* | |
| 03 | 1 | RR | A |
| 04 | 1 | INC | A |
| 05 | 2 | INC | data addr |
| 06 | 1 | INC | @R0 |
| 07 | 1 | INC | @R1 |
| 08 | 1 | INC | R0 |
| 09 | 1 | INC | R1 |
| 0A | 1 | INC | R2 |
| 0B | 1 | INC | R3 |
| 0C | 1 | INC | R4 |
| 0D | 1 | INC | R5 |
| 0E | 1 | INC | R6 |
| 0F | 1 | INC | R7 |
| 10 | 3 | JBC | bit addr, code addr |
| 11 | 2 | ACALL | code addr |
| 12* | | | |
| 13 | 1 | RRC | A |
| 14 | 1 | DEC | A |
| 15 | 2 | DEC | data addr |
| 16 | 1 | DEC | @R0 |
| 17 | 1 | DEC | @R1 |
| 18 | 1 | DEC | R0 |
| 19 | 1 | DEC | R1 |
| 1A | 1 | DEC | R2 |
| 1B | 1 | DEC | R3 |
| 1C | 1 | DEC | R4 |
| 1D | 1 | DEC | R5 |
| 1E | 1 | DEC | R6 |
| 1F | 1 | DEC | R7 |
| 20 | 3 | JB | bit addr, code addr |
| 21 | 2 | AJMP | code addr |
| 22 | 1 | RET | |
| 23 | 1 | RL | A |
| 24 | 2 | ADD | A,#data |
| 25 | 2 | ADD | A,data addr |
| 26 | 1 | ADD | A,@R0 |
| 27 | 1 | ADD | A,@R1 |
| 28 | 1 | ADD | A,R0 |
| 29 | 1 | ADD | A,R1 |
| 2A | 1 | ADD | A,R2 |
| 2B | 1 | ADD | A,R3 |
| 2C | 1 | ADD | A,R4 |
| 2D | 1 | ADD | A,R5 |
| 2E | 1 | ADD | A,R6 |
| 2F | 1 | ADD | A,R7 |
| 30 | 3 | JNB | bit addr, code addr |
| 31 | 2 | ACALL | code addr |
| 32 | 1 | RETI | |
| 33 | 1 | RLC | A |
| 34 | 2 | ADDC | A,#data |
| 35 | 2 | ADDC | A,data addr |
| 36 | 1 | ADDC | A,@R0 |
| 37 | 1 | ADDC | A,@R1 |
| 38 | 1 | ADDC | A,R0 |
| 39 | 1 | ADDC | A,R1 |
| 3A | 1 | ADDC | A,R2, |
| 3B | 1 | ADDC | A,R3 |
| 3C | 1 | ADDC | A,R4 |
| 3D | 1 | ADDC | A,R5 |
| 3E | 1 | ADDC | A,R6 |
| 3F | 1 | ADDC | A,R7 |

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 40 | 2 | JC | code addr |
| 41 | 2 | AJMP | code addr |
| 42 | 2 | ORL | data addr,A |
| 43 | 3 | ORL | data addr,#data |
| 44 | 2 | ORL | A,#data |
| 45 | 2 | ORL | A,data addr |
| 46 | 1 | ORL | A,@R0 |
| 47 | 1 | ORL | A,@R1 |
| 48 | 1 | ORL | A,R0 |
| 49 | 1 | ORL | A,R1 |
| 4A | 1 | ORL | A,R2 |
| 4B | 1 | ORL | A,R3 |
| 4C | 1 | ORL | A,R4 |
| 4D | 1 | ORL | A,R5 |
| 4E | 1 | ORL | A,R6 |
| 4F | 1 | ORL | A,R7 |
| 50 | 2 | JNC | code addr |
| 51 | 2 | ACALL | code addr |
| 52 | 2 | ANL | data addr,A |
| 53 | 3 | ANL | data addr,#data |
| 54 | 2 | ANL | A,#data |
| 55 | 2 | ANL | A,data addr |
| 56 | 1 | ANL | A,@R0 |
| 57 | 1 | ANL | A,@R1 |
| 58 | 1 | ANL | A,R0 |
| 59 | 1 | ANL | A,R1 |
| 5A | 1 | ANL | A,R2 |
| 5B | 1 | ANL | A,R3 |
| 5C | 1 | ANL | A,R4 |
| 5D | 1 | ANL | A,R5 |
| 5E | 1 | ANL | A,R6 |
| 5F | 1 | ANL | A,R7 |
| 60 | 2 | JZ | code addr |
| 61 | 2 | AJMP | code addr |
| 62 | 2 | XRL | data addr,A |
| 63 | 3 | XRL | data addr,#data |
| 64 | 2 | XRL | A,#data |
| 65 | 2 | XRL | A,data addr |
| 66 | 1 | XRL | A,@R0 |
| 67 | 1 | XRL | A,@R1 |
| 68 | 1 | XRL | A,R0 |
| 69 | 1 | XRL | A,R1 |
| 6A | 1 | XRL | A,R2 |
| 6B | 1 | XRL | A,R3 |
| 6C | 1 | XRL | A,R4 |
| 6D | 1 | XRL | A,R5 |
| 6E | 1 | XRL | A,R6 |
| 6F | 1 | XRL | A,R7 |
| 70 | 2 | JNZ | code addr |
| 71 | 2 | ACALL | code addr |
| 72 | 2 | ORL | C,bit addr |
| 73 | 1 | JMP | @A + DPTR |
| 74 | 2 | MOV | A,#data |
| 75 | 3 | MOV | data addr,#data |
| 76 | 2 | MOV | @R0,#data |
| 77 | 2 | MOV | @R1,#data |
| 78 | 2 | MOV | R0,#data |
| 79 | 2 | MOV | R1,#data |
| 7A | 2 | MOV | R2,#data |
| 7B | 2 | MOV | R3,#data |
| 7C | 2 | MOV | R4,#data |
| 7D | 2 | MOV | R5,#data |
| 7E | 2 | MOV | R6,#data |
| 7F | 2 | MOV | R7,#data |

## INSTRUCTION OPCODES IN HEXADECIMAL ORDER (Continued)

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 80 | 2 | SJMP | code addr |
| 81 | 2 | AJMP | code addr |
| 82 | 2 | ANL | C,bit addr |
| 83 | 1 | MOVC | A,@A + PC |
| 84 | 1 | DIV | AB |
| 85 | 3 | MOV | data addr,data addr |
| 86 | 2 | MOV | data addr,@R0 |
| 87 | 2 | MOV | data addr,@R1 |
| 88 | 2 | MOV | data addr,R0 |
| 89 | 2 | MOV | data addr,R1 |
| 8A | 2 | MOV | data addr,R2 |
| 8B | 2 | MOV | data addr,R3 |
| 8C | 2 | MOV | data addr,R4 |
| 8D | 2 | MOV | data addr,R5 |
| 8E | 2 | MOV | data addr,R6 |
| 8F | 2 | MOV | data addr,R7 |
| 90 | 3 | MOV | DPTR,#data |
| 91 | 2 | ACALL | code addr |
| 92 | 2 | MOV | bit addr,C |
| 93 | 1 | MOVC | A,@A + DPTR |
| 94 | 2 | SUBB | A,#data |
| 95 | 2 | SUBB | A,data addr |
| 96 | 1 | SUBB | A,@R0 |
| 97 | 1 | SUBB | A,@R1 |
| 98 | 1 | SUBB | A,R0 |
| 99 | 1 | SUBB | A,R1 |
| 9A | 1 | SUBB | A,R2 |
| 9B | 1 | SUBB | A,R3 |
| 9C | 1 | SUBB | A,R4 |
| 9D | 1 | SUBB | A,R5 |
| 9E | 1 | SUBB | A,R6 |
| 9F | 1 | SUBB | A,R7 |
| A0 | 2 | ORL | C,/bit addr |
| A1 | 2 | AJMP | code addr |
| A2 | 2 | MOV | C,bit addr |
| A3 | 1 | INC | DPTR |
| A4 | 1 | MUL | AB |
| A5 | | reserved | |
| A6 | 2 | MOV | @R0,data addr |
| A7 | 2 | MOV | @R1,data addr |
| A8 | 2 | MOV | R0,data addr |
| A9 | 2 | MOV | R1,data addr |
| AA | 2 | MOV | R2,data addr |
| AB | 2 | MOV | R3,data addr |
| AC | 2 | MOV | R4,data addr |
| AD | 2 | MOV | R5,data addr |
| AE | 2 | MOV | R6,data addr |
| AF | 2 | MOV | R7,data addr |
| B0 | 2 | ANL | C,/bit addr |
| B1 | 2 | ACALL | code addr |
| B2 | 2 | CPL | bit addr |
| B3 | 1 | CPL | C |
| B4 | 3 | CJNE | A,#data,code addr |
| B5 | 3 | CJNE | A,data addr,code addr |
| B6 | 3 | CJNE | @R0,#data,code addr |
| B7 | 3 | CJNE | @R1,#data,code addr |
| B8 | 3 | CJNE | R0,#data,code addr |
| B9 | 3 | CJNE | R1,#data,code addr |
| BA | 3 | CJNE | R2,#data,code addr |
| BB | 3 | CJNE | R3,#data,code addr |
| BC | 3 | CJNE | R4,#data,code addr |
| BD | 3 | CJNE | R5#data,code addr |
| BE | 3 | CJNE | R6,#data,code addr |
| BF | 3 | CJNE | R7,#data,code addr |
| C0 | 2 | PUSH | data addr |
| C1 | 2 | AJMP | code addr |
| C2 | 2 | CLR | bit addr |
| C3 | 1 | CLR | C |
| C4 | 1 | SWAP | A |
| C5 | 2 | XCH | A,data addr |
| C6 | 1 | XCH | A,@R0 |
| C7 | 1 | XCH | A,@R1 |
| C8 | 1 | XCH | A,R0 |
| C9 | 1 | XCH | A,R1 |
| CA | 1 | XCH | A,R2 |
| CB | 1 | XCH | A,R3 |
| CC | 1 | XCH | A,R4 |
| CD | 1 | XCH | A,R5 |
| CE | 1 | XCH | A,R6 |
| CF | 1 | XCH | A,R7 |
| D0 | 2 | POP | data addr |
| D1 | 2 | ACALL | code addr |
| D2 | 2 | SETB | bit addr |
| D3 | 1 | SETB | C |
| D4 | 1 | DA | A |
| D5 | 3 | DJNZ | data addr,code addr |
| D6 | 1 | XCHD | A,@R0 |
| D7 | 1 | XCHD | A,@R1 |
| D8 | 2 | DJNZ | R0,code addr |
| D9 | 2 | DJNZ | R1,code addr |
| DA | 2 | DJNZ | R2,code addr |
| DB | 2 | DJNZ | R3,code addr |
| DC | 2 | DJNZ | R4,code addr |
| DD | 2 | DJNZ | R5,code addr |
| DE | 2 | DJNZ | R6,code addr |
| DF | 2 | DJNZ | R7,code addr |
| E0* | | | |
| E1 | 2 | AJMP | code addr |
| E2* | | | |
| E3* | | | |
| E4 | 1 | CLR | A |
| E5 | 2 | MOV | A,data addr |
| E6 | 1 | MOV | A,@R0 |
| E7 | 1 | MOV | A,@R1 |
| E8 | 1 | MOV | A,R0 |
| E9 | 1 | MOV | A,R1 |
| EA | 1 | MOV | A,R2 |
| EB | 1 | MOV | A,R3 |
| EC | 1 | MOV | A,R4 |
| ED | 1 | MOV | A,R5 |
| EE | 1 | MOV | A,R6 |
| EF | 1 | MOV | A,R7 |
| F0* | | | |
| F1 | 1 | ACALL | code addr |
| F2* | | | |
| F3* | | | |
| F4 | 1 | CPL | A |
| F5 | 2 | MOV | data addr,A |
| F6 | 1 | MOV | @R0,A |
| F7 | 1 | MOV | @R1,A |
| F8 | 1 | MOV | R0,A |
| F9 | 1 | MOV | R1,A |
| FA | 1 | MOV | R2,A |
| FB | 1 | MOV | R3,A |
| FC | 1 | MOV | R4,A |
| FD | 1 | MOV | R5,A |
| FE | 1 | MOV | R6,A |
| FF | 1 | MOV | R7,A |

* Missing 80C51 instructions are not applicable to the 83C751. Should these instructions be executed, the appropriate number of ROM bytes will be fetched, but no operation will take place. The use of these codes is not recommended. The addr16 field is allowed for compatiblilty with existing software tools, however, only the least significant 11 bits of the address field will be used.

Signetics

# 87C51

## CMOS Single-Chip 8-Bit EPROM Microcontroller

*Product Specification*

**Military Microprocessor Products**

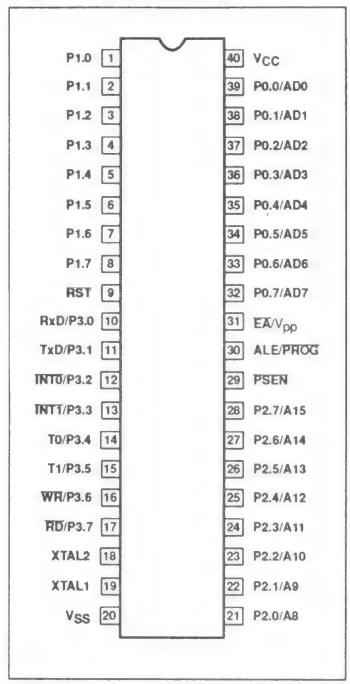
## DESCRIPTION

The Signetics 87C51 is a high-performance microcontroller fabricated with Signetics high-density CMOS technology. The CMOS 87C51 is functionally compatible with the NMOS 8031/8051 and 80C51 microcontrollers. The Signetics CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Signetics epitaxial substrate minimizes latch-up sensitivity.

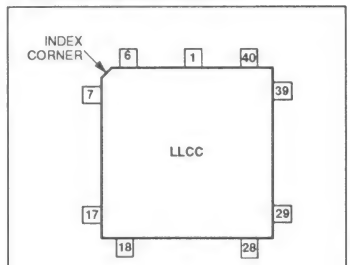
The 87C51 contains a 4K x 8 EPROM, a 128 x 9 RAM, 32 I/O lines, two 16-bit counter/timers, a five-source, two priority level nested interrupt structure, a serial I/O port for either multiprocessor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 87C51 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

## PIN CONFIGURATION




## PIN CONFIGURATION




| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | NC | 23 | NC |
| 2 | P1.0 | 24 | P2.0/A8 |
| 3 | P1.1 | 25 | P2.1/A9 |
| 4 | P1.2 | 26 | P2.2/A10 |
| 5 | P1.3 | 27 | P2.3/A11 |
| 6 | P1.4 | 28 | P2.4/A12 |
| 7 | P1.5 | 29 | P2.5/A13 |
| 8 | P1.6 | 30 | P2.6/A14 |
| 9 | P1.7 | 31 | P2.7/A15 |
| 10 | RST | 32 | PSEN |
| 11 | RxD/P3.0 | 33 | ALE/PROG |
| 12 | NC | 34 | NC |
| 13 | TxD/P3.1 | 35 | EA/Vpp |
| 14 | INT0/P3.2 | 36 | P0.7/AD7 |
| 15 | INT1/P3.4 | 37 | P0.6/AD6 |
| 16 | T0/P3.4 | 38 | P0.5/AD5 |
| 17 | T1/P3.5 | 39 | P0.4/AD4 |
| 18 | WR/P3.6 | 40 | P0.3/AD3 |
| 19 | RD/P3.7 | 41 | P0.2/AD2 |
| 20 | XTAL2 | 42 | P0.1/AD1 |
| 21 | XTAL1 | 43 | P0.0/AD0 |
| 22 | GND | 44 | VCC |

## FEATURES

- **8031/8051/80C51 compatible**
  - **4K x 8 EPROM**
  - **128 x 8 RAM**
  - **Two 16-bit counter/timers**
  - **Full duplex serial channel**
  - **Boolean processor**
- **Memory addressing capability**
  - **64K ROM and 64K RAM**
- **Power control modes:**
  - **Idle mode**
  - **Power-down mode**
- **CMOS and TTL compatible**

# CMOS Single–Chip 8–Bit EPROM Microcontroller — 87C51

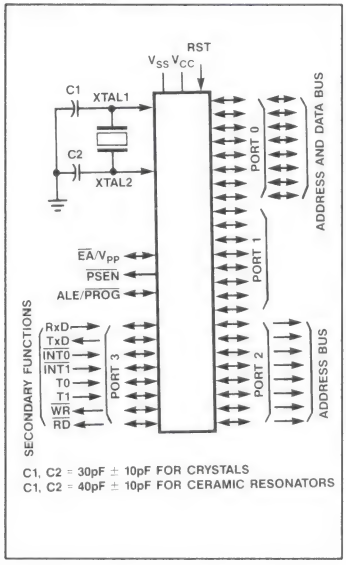
## ORDERING INFORMATION

| PACKAGES | ORDER CODE | SMD CODE |
|---|---|---|
| 40-Pin Ceramic DIP | 87C51/BQA | 5962–8768401QA |
| 40-Pin Ceramic LLCC | 87C51/BUA | 5962–8768401UA |

## ELECTRICAL PERFORMANCE CHARACTERISTICS AND TEST REQUIREMENTS

For Absolute Maximum Ratings, Recommended Operating Conditions, and Electrical Test Requirements, refer to the following documents: Military Drawing 5962–8768401

## LOGIC SYMBOL



Signetics

# 87C451

## CMOS Single-Chip 8-Bit EPROM Microcontroller

*Objective Specification*

**Military Microprocessor Products**

### DESCRIPTION

The Signetics 87C451 is an I/O expanded, single-chip microcontroller fabricated with Signetics high-density CMOS technology. Signetics epitaxial substrate minimizes latch-up sensitivity.

The 87C451 has 4K of EPROM on chip as program memory and is otherwise identical to the 83C451.

The 87C451 is a functional extension of the 87C51 microcontroller with three additional I/O ports and four I/O control lines. Four control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

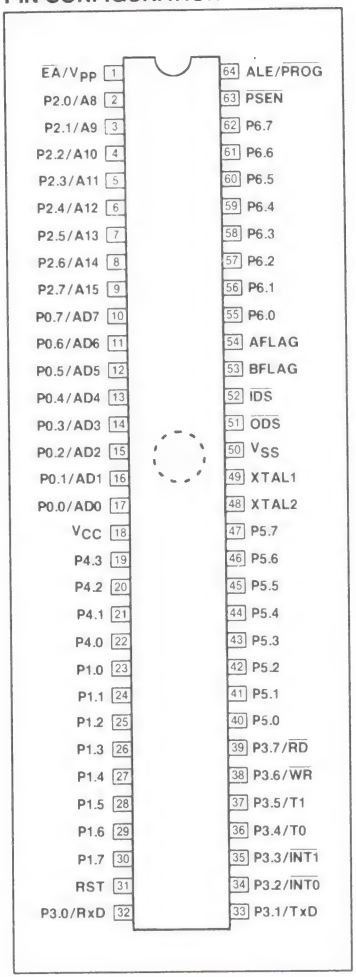
The 87C451 includes a 4K × 8 EPROM; a 128 × 8 RAM; 64 I/O lines; two 16-bit timer/counters; a five source, two priority level, nested interrupt structure; a serial I/O port for either a full-duplex UART, I/O expansion, or multiprocessor communications; and on-chip oscillator and clock circuits.

The 87C451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

### FEATURES

- **User-programmable microcontroller**
- **80C51-based architecture**
- **64-Pin DIP package**
  - **Six 8-bit ports and one 4-bit port**
- **Port 6 features:**
  - **8 data pins**
  - **4 control pins**
  - **Direct MPU bus interface**
  - **Parallel printer interface**
- **On the microcontroller**
  - **4K X 8 EPROM**
  - **128 X 8 RAM**
  - **Two 16-bit counter/timers**
  - **Two external interrupts**
- **External memory addressing capability:**
  - **64K ROM and 64K RAM**
- **Low power consumption:**
  - **Normal operation: less than 24mA at 5V, 12MHz**
  - **Idle mode**
  - **Power-down mode**

### PIN CONFIGURATION

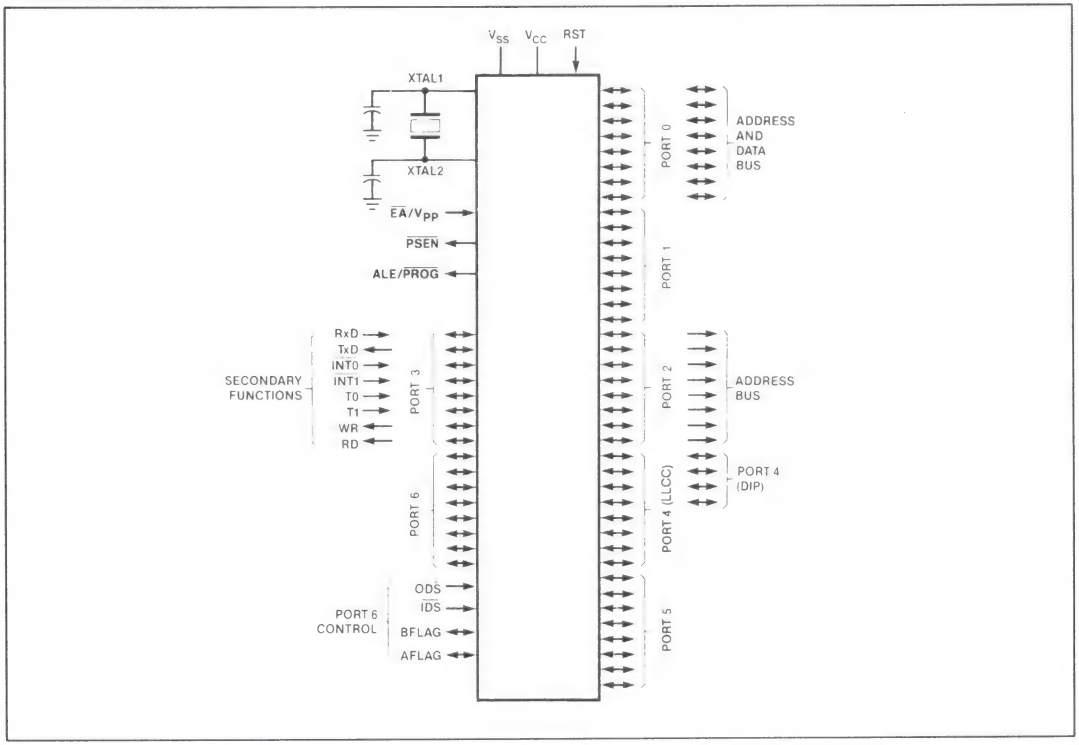


# CMOS Single-Chip 8-Bit EPROM Microcontroller — 87C451

## ORDERING INFORMATION

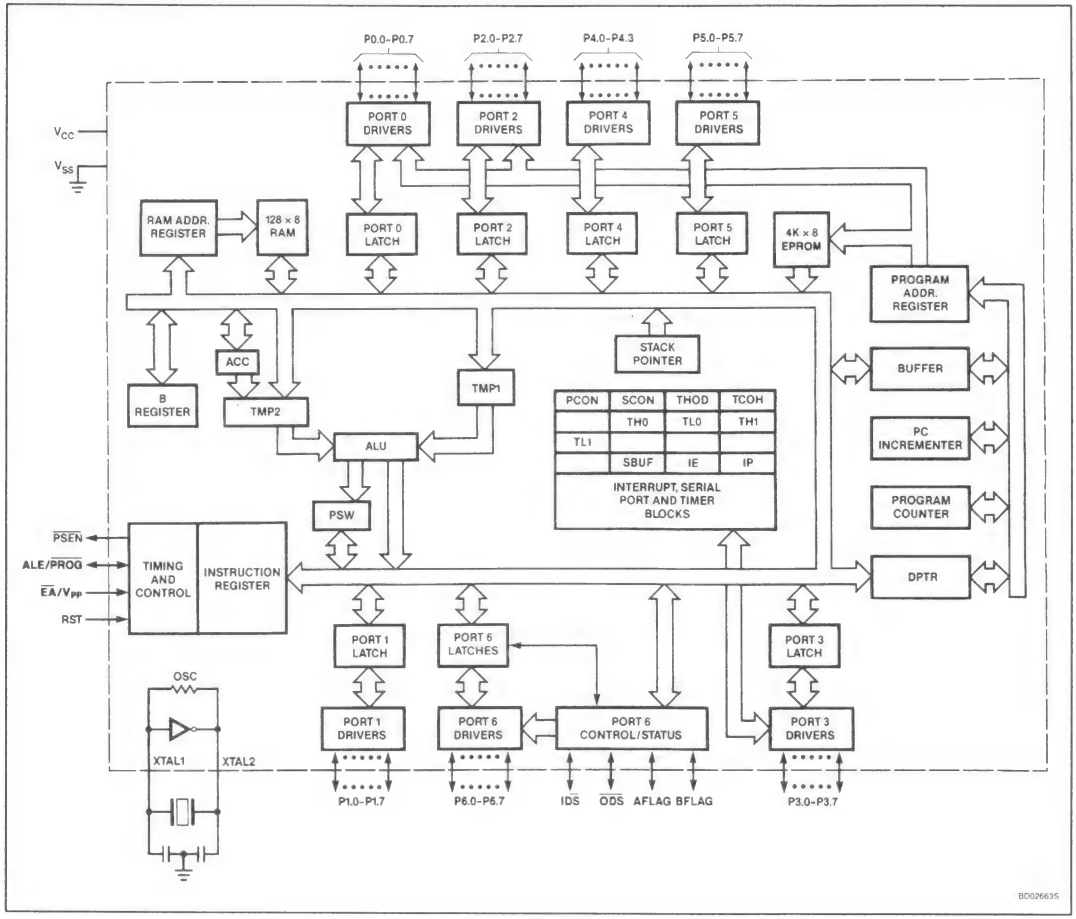
| PACKAGE | ORDER CODE |
|---|---|
| 64–Pin Ceramic DIP w/Quartz window | 87C451/BXA |
| 64–Pin Ceramic DIP w/o Quartz window | 87C451/BXA OT[1] |

## LOGIC SYMBOL



# CMOS Single-Chip 8-Bit EPROM Microcontroller — 87C451

## BLOCK DIAGRAM



# CMOS Single-Chip 8-Bit EPROM Microcontroller — 87C451

## PIN DESCRIPTION

| MNEMONIC | PIN NO | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| $V_{SS}$ | 50 | | **Ground:** 0V reference |
| $V_{CC}$ | 18 | | **Power Supply:** +5V. |
| P0.0–P0.7 | 17–10 | I/O | **Port 0:** An 8–bit open–drain, bidirectional I/O port. Port 0 is also the multiplexed low–order address and data bus during accesses to external memory, and outputs instruction bytes during program verification. External pull–ups are required during program verification. Port 0 can sink/source eight LSTTL inputs. |
| P1.0–P1.7 | 23–30 | I/O | **Port 1:** An 8–bit bidirectional I/O port with internal pull–ups. Port 1 receives the low–order address bytes during program verification. In the 87C451, port 1 can sink/source three LSTTL inputs, and drive CMOS inputs without external pull–ups. |
| P2.0–P2.7 | 2–9 | I/O | **Port 2:** An 8–bit bidirectional I/O port with internal pull–ups. Port 2 emits the high–order address bytes during accesses to external memory and receives the high–order address bit and control signals during program verification in the 87C451. Port 2 can sink/source three LSTTL inputs and drive CMOS inputs without external pull–ups. |
| P3.0–P3.7 | 32–39 | I/O | **Port 3:** An 8–bit bidirectional I/O port with internal pull–ups. Port 3 can sink/source three LSTTL inputs and drive CMOS inputs without external pull–ups. Port 3 also serves the 87C451 special functions listed below: |
| | 32 | I | RxD (P3.0): Serial input port |
| | 33 | O | TxD (P3.1): Serial output port |
| | 34 | I | $\overline{INT0}$ (P3.2): External interrupt 0 |
| | 35 | I | $\overline{INT1}$ (P3.3): External interrupt 1 |
| | 36 | I | T0 (P3.4): Timer 0 external input |
| | 37 | I | T1 (P3.5): Timer 1 external input |
| | 38 | O | $\overline{WR}$ (P3.6): External data memory write strobe |
| | 39 | O | $\overline{RD}$ (P3.7): External data memory read strobe |
| P4.0–P4.3 | 22–19 | I/O | **Port 4:** A 4–bit bidirectional port with internal pull–ups. Port 4 can sink/source three LSTTL inputs and drive CMOS inputs without external pull–ups. |
| P5.0–P5.7 | 40–47 | I/O | **Port 5:** An 8–bit I/O port with internal pull–ups. Port 5 can sink/source three LSTTL inputs and drive CMOS inputs without external pull–ups. |
| P6.0–P6.7 | 55–62 | I/O | **Port 6:** A specialized 8–bit bidirectional I/O port with internal pull–ups. This special port can sink/source three LSTTL inputs and drive CMOS inputs without external pull–ups. Port 6 can be used in a strobed or non–strobed mode of operation, and in conjunction with four control pins that serve the functions listed below. |
| | | | **Port 6 Control Lines:** |
| $\overline{ODS}$ | 51 | I | $\overline{ODS}$: Output data strobe |
| $\overline{IDS}$ | 52 | I | $\overline{IDS}$: Input data strobe |
| BFLAG | 53 | I/O | BFLAG: A bidirectional I/O pin with internal pull–ups |
| AFLAG | 54 | I/O | A FLAG: A bidirectional I/O pin with internal pull–ups |
| RST | 31 | I | **RESET:** A High level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull–down resistor permits power–on reset using only a capacitor connected to the $V_{CC}$. |
| ALE/$\overline{PROG}$ | 64 | I/O | **Address Latch Enable Program Pulse:** An output for latching the Low byte of the address during accesses to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access, at which time one ALE is skipped. ALE can sink/source eight LSTTL inputs and drive CMOS inputs without an external pull–up. This pin is also the program pulse input during EPROM programming. |
| $\overline{PSEN}$ | 63 | O | **Program Store Enable:** This output is the read strobe to external program memory. $\overline{PSEN}$ is activated twice each machine cycle during fetches from external program memory; however, when executing out of external program memory, two activations of $\overline{PSEN}$ are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. $\overline{PSEN}$ can sink/source eight LSTTL inputs and drive CMOS inputs without an external pull–up. |
| $\overline{EA}$/$V_{PP}$ | 1 | I | **Instruction Execution Control/Programming Supply Voltage:** When $\overline{EA}$ is held High, the CPU executes out of internal program memory, unless the program counter exceeds OFFFH. When $\overline{EA}$ is held Low, the CPU executes out of external program memory. $\overline{EA}$ must never be allowed to float. This pin also receives the 12.75V programming supply voltage ($V_{PP}$) during EPROM programming. |
| XTAL1 | 49 | I | **Crystal 1:** An input to the inverting amplifier that forms the oscillator. This input receives the external oscillator when an external oscillator is used. |
| XTAL2 | 48 | O | **Crystal 2:** Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used. |

# CMOS Single-Chip 8-Bit EPROM Microcontroller — 87C451

## ABSOLUTE MAXIMUM RATINGS[2]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Operating ambient temperature range | –55 to +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| | Voltage from $V_{CC}$ to $V_{SS}$[3] | –0.5 to +6.5 | V |
| | Voltage from any pin to $V_{SS}$ (except $V_{PP}$)[3] | –0.5 to $V_{CC}$ +0.5 | V |
| | Voltage on $V_{PP}$ | –0.5 to 13.0 | V |
| $P_D$ | Power dissipation | 200 | mW |

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.0V \le V_{CC} \le 6.0V$, $V_{SS} = 0V$.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IL}$ | Input Low voltage, except $\overline{EA}$ | | –0.5 | 0.2 $V_{CC}$ – 0.25 | V |
| $V_{IL1}$ | Input Low voltage, $\overline{EA}$ | | | 0.2 $V_{CC}$ – 0.45 | V |
| $V_{IH}$ | Input High voltage, except XTAL1, RST | | 0.2 $V_{CC}$ +1.1 | $V_{CC}$ + 0.5 | V |
| $V_{IH1}$ | Input High voltage, XTAL1, RST | | 0.7 $V_{CC}$ +0.2 | $V_{CC}$ + .05 | V |
| $V_{OL}$ | Output Low voltage, ports 1,2,3,4,5,6, AFLAG, BFLAG | $I_{OL}$ = 1.6mA[4] | | 0.45 | V |
| $V_{OL1}$ | Output Low voltage, port 0, ALE, $\overline{PSEN}$ | $I_{OL}$ = 3.2mA[4] | | 0.45 | V |
| $V_{OH}$ | Output High voltage, ports 1,2,3,4,5,6, AFLAG, BFLAG | $I_{OH}$ = –60µA,<br>$V_{CC}$ = 5V ± 10%<br>$I_{OH}$ = –25µA<br>$I_{OH}$ = –10µA | <br>2.4<br>0.75$V_{CC}$<br>0.9$V_{CC}$ | | <br>V<br>V<br>V |
| $V_{OH1}$ | Output High voltage, port 0 in external bus mode, ALE, $\overline{PSEN}$ | $I_{OH}$ = –800µA,<br>$V_{CC}$ = 5V ± 10%<br>$I_{OH}$ = –150µA<br>$I_{OH}$ = –80µA[5] | <br>2.4<br>0.75$V_{CC}$<br>0.9$V_{CC}$ | | <br>V<br>V<br>V |
| $I_{IL}$ | Logical 0 input current, ports 1,2,3,4,5,6, AFLAG, BFLAG | $V_{IN}$ = 0.45V | | –75 | µA |
| $I_{TL}$ | Logical 1 to 0 transition current, ports 1,2,3,4,5,6, AFLAG, BFLAG | $V_{IN}$ = 2V | | –750 | µA |
| $I_{LI}$ | Input leakage, current port 0, $\overline{EA}$, $\overline{IDS}$, $\overline{ODS}$ | $0.45V \le V_{IN} \le V_{CC}$ | | ±10 | µA |
| $R_{RST}$ | Reset pulldown resistor | | 50 | 150 | kΩ |
| $C_{IO}$[7] | Pin capacitance | Test freq. = 1MHz,<br>$T_A$ = 25°C | | 10 | pF |
| $I_{PD}$ | Power–down current | $V_{CC}$ = 2V to 6V[3] | | 50 | µA |

## MAXIMUM $I_{CC}$ (mA)

| Frequency/ $V_{CC}$ | OPERATING[8] | | | IDLE[9] | | |
|---|---|---|---|---|---|---|
| | 4V | 5V | 6V | 4V | 5V | 6V |
| 3.5MHz<br>8.0MHz<br>12MHz | TBD | TBD | TBD | TBD | TBD | TBD |

# CMOS Single-Chip 8-Bit EPROM Microcontroller — 87C451

## AC ELECTRICAL CHARACTERISTICS

$-55°C \leq T_A \leq +125°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80 pF[10]

| SYMBOL | PARAMETER | 12MHz CLOCK | | VARIABLE CLOCK ($f = 1/t_{CLCL}$) | | UNIT |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | | | | 3.5 | 12 | MHz |
| $t_{LHLL}$ | ALE pulse width | 112 | | $2t_{CLCL}-55$ | | ns |
| $t_{AVLL}$ | Address valid to ALE Low | 13 | | $t_{CLCL}-70$ | | ns |
| $t_{LLAX}$ | Address hold after ALE Low | 33 | | $t_{CLCL}-50$ | | ns |
| $t_{LLIV}$ | ALE Low to valid instr in | | 218 | | $4t_{CLCL}-115$ | ns |
| $t_{LLPL}$ | ALE Low to $\overline{PSEN}$ Low | 28 | | $t_{CLCL}-55$ | | ns |
| $t_{PLPH}$ | $\overline{PSEN}$ pulse width | 190 | | $3t_{CLCL}-60$ | | ns |
| $t_{PLIV}$ | $\overline{PSEN}$ Low to valid instr in | | 130 | | $3t_{CLCL}-120$ | ns |
| $t_{PXIX}$ | Input instr hold after $\overline{PSEN}$ | 0 | | 0 | | ns |
| $t_{PXIZ}$ | Input instr float after $\overline{PSEN}$ | | 58 | | $t_{CLCL}-25$ | ns |
| $t_{AVIV}$ | Address to valid instr in | | 297 | | $5t_{CLCL}-120$ | ns |
| $t_{PLAZ}$ | $\overline{PSEN}$ Low to address float | | 25 | | 25 | ns |
| $t_{RLRH}$ | $\overline{RD}$ pulse width | 400 | | $6t_{CLCL}-100$ | | ns |
| $t_{WLWH}$ | $\overline{WR}$ pulse width | 400 | | $6t_{CLCL}-100$ | | ns |
| $t_{RLDV}$ | $\overline{RD}$ Low to valid data in | | 232 | | $5t_{CLCL}-185$ | ns |
| $t_{RHDX}$ | Data hold after $\overline{RD}$ | 0 | | 0 | | ns |
| $t_{RHDZ}$ | Data float after $\overline{RD}$ | | 82 | | $2t_{CLCL}-85$ | ns |
| $t_{LLDV}$ | ALE Low to valid data in | | 496 | | $8t_{CLCL}-170$ | ns |
| $t_{AVDV}$ | Address to valid data in | | 565 | | $9t_{CLCL}-185$ | ns |
| $t_{LLWL}$ | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 185 | 315 | $3t_{CLCL}-65$ | $3t_{CLCL}+65$ | ns |
| $t_{QVWX}$ | Data valid to $\overline{WR}$ transition | 8 | | $t_{CLCL}-75$ | | ns |
| $t_{WHQX}$ | Data hold after $\overline{WR}$ | 18 | | $t_{CLCL}-65$ | | ns |
| $t_{RLAZ}$ | $\overline{RD}$ Low to address float | | 0 | | 0 | ns |
| $t_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE High | 18 | 148 | $t_{CLCL}-65$ | $t_{CLCL}+65$ | ns |
| **Port 6 input (input rise and fall times ≤ 5ns)** | | | | | | |
| $t_{ILIH}$ | $\overline{IDS}$ width | 270 | | $3t_{CLCL}+20$ | | ns |
| $t_{DVIH}$ | Data setup to $\overline{IDS}$ High | 0 | | 0 | | ns |
| $t_{IHDX}$ | Data hold after $\overline{IDS}$ | 30 | | 30 | | ns |
| $t_{FLIL}$ | $\overline{PE}$ to $\overline{IDS}$ | 25 | | 25 | | ns |
| $t_{IVFV}$ | $\overline{IDS}$ to BFLAG (IBF) delay | | 130 | | 130 | ns |
| **Port 6 ouput** | | | | | | |
| $t_{OLOH}$ | $\overline{ODS}$ width | 270 | | $3t_{CLCL}+20$ | | ns |
| $t_{FVDV}$ | SEL to data out delay | | 85 | | 85 | ns |
| $t_{OLDV}$ | $\overline{ODS}$ to data out delay | | 80 | | 80 | ns |
| $t_{OHDZ}$ | $\overline{ODS}$ to data float delay | | 35 | | 35 | ns |
| $t_{OVFV}$ | $\overline{ODS}$ to AFLAG (OBF) delay | | 100 | | 100 | ns |
| $t_{FLDV}$ | $\overline{PE}$ to data out delay | | 120 | | 120 | ns |
| $t_{OHFH}$ | $\overline{ODS}$ High to AFLAG (SEL) delay | 100 | | 100 | | ns |

**NOTES:**

1. Erase characteristics do not apply for one time programming (OT).
2. Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
3. This product includes circuitry specifically designed for the protection on its internal devices from damaging effects of excessive static charge. Nonetheless it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maximum.
4. Capacitive loading on ports 0 and 2 can cause spurious noise to be superimposed on the $V_{OLS}$ of ALE and ports 1 and 3. The noise is caused by external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1–to–0 transitions during bus operations. In the worst cases it could be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.
5. Capacitive loading on ports 0 and 2 can cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall before the $0.9V_{CC}$ specification when the address bits are stabilizing.
6. Power–down $I_{CC}$ is measured with all output pins disconnected; $\overline{EA}$ = port 0 = $V_{CC}$; XTAL2 = N.C.; RST = $V_{SS}$.
7. $C_{IO}$ is tested initially and after any design or process changes which may affect capacitance.
8. $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL}$ = $V_{SS}$+ 0.5V, $V_{IH}$ = $V_{CC}$–0.5V; XTAL1 = N.C.; XTAL2 = $\overline{EA}$ = RST = Port 0 = $V_{CC}$. $I_{CC}$ will be slightly higher if a crystal oscillator is used.
9. Idle $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL}$ = $V_{SS}$+ 0.5V, $V_{IH}$ = $V_{CC}$–0.5V; XTAL = N.C.; port 0 = $V_{CC}$; $\overline{EA}$ = RST = $V_{SS}$.
10. Parameters are valid over operating temperature range unless otherwise specified.

## PORTS 4 and 5

Ports 4 and 5 are bidirectional I/O ports with internal pull–ups. Port 4 is a 4–bit port. Port 4 and port 5 pins, with ones written to them, are pulled High by the internal pull–ups, and in that state can be used as inputs. Ports 4 and 5 are addressed at the special function register addresses shown in Table 1.

## PORT 6

Port 6 is a special 8–bit bidirectional I/O port with internal pull–ups. (See Figure 1.) This port can be used as a standard I/O port, or in strobed modes of operation in conjunction with four special control lines: $\overline{ODS}$, $\overline{IDS}$, AFLAG, and BFLAG. Port 6 operating modes are controlled by the port 6 Control Status Register (CSR). Port 6 and the CSR are addressed at the special function register addresses shown in Table 1. The following four control pins are used in conjunction with port 6:

**$\overline{ODS}$:** Output data strobe input for port 6. $\overline{ODS}$ can be programmed to control the port 6 output drivers and the Output Buffer Full Flag (OBF), or to clear only the OBF flag bit in the CSR (output–always mode). $\overline{ODS}$ is Active–Low for output driver control. The OBF flag can be programmed to be cleared on the negative or positive edge of $\overline{ODS}$.

**$\overline{IDS}$**: Input data strobe input for port 6. $\overline{IDS}$ is used to control the port 6 input latch and Input Buffer Full Flag (IBF) bit in the CSR. The input data latch can be programmed to be transparent when the $\overline{IDS}$ is Low and latched on the positive transition of $\overline{IDS}$, or to latch only on the positive transition of $\overline{IDS}$. Correspondingly, the IBF flag is set on the negative or positive transition of $\overline{IDS}$.

**AFLAG:** A bidirectional I/O pin. AFLAG can be programmed to be an output set High or Low under program control, or to output the state of the output buffer full flag. AFLAG can also be programmed to be an input which selects whether the contents of the output buffer, or the contents of the port 6 control status register will be output on port 6. This feature grants complete port 6 status to external devices.

**BFLAG:** A bidirectional I/O pin. BFLAG can be programmed to be an output, set High or Low under program control, or to output the state of the input buffer full flag. BFLAG can also be programmed to input an enable signal for port 6. When BFLAG is used as an enable input, port 6 output drivers are in the High impedance state, and the input latch does not respond to the $\overline{IDS}$ strobe when BFLAG is High. Both features are enabled when BFLAG is Low. This feature facilitates the use of the 87C451 in bused multiprocessor systems.

## CONTROL STATUS REGISTER

The Control Status Register (CSR) establishes the mode of operation for port 6 and indicates the current status of the port 6 I/O registers. All control status register bits can be read and written by the CPU, except bits 0 and 1, which are read only. Reset writes ones to bits 2 through 7, and writes zeros to bits 0 and 1.

**CSR.0 — Input Buffer Full Flag (IBF) (Read only)**
The IBF bit is set to a logic 1 when port 6 data is loaded into the input buffer under control of $\overline{IDS}$. This can occur on the negative or positive edge of $\overline{IDS}$, as determined by CSR.2. IBF is cleared when the CPU reads the input buffer register.

**CSR.1 — Output Buffer Full Flag (OBF) (Read only)**
The OBF flag is set to a logic 1 when the CPU writes to the port 6 output data buffer. OBF is cleared by the positive or negative edge of $\overline{ODS}$, as determined by CSR.3.

**CSR.2 — IDS Mode Select (IDSM)**
When CSR.2 = 0, a Low–to–High transition on the $\overline{IDS}$ pin sets the IBF flag. The port 6 input buffer is loaded on the $\overline{IDS}$ positive edge. When CSR.2 = 1, a High–to–Low transition on the $\overline{IDS}$ pin sets the IBF flag. The port 6 input buffer is transparent when $\overline{IDS}$ is Low, and latched when $\overline{IDS}$ is High.

**CSR.3 — Output Buffer Full Flag Clear Mode (OBFC)**
When CSR.3 = 1, the positive edge of the $\overline{ODS}$ input clears the OBF flag. When CSR.3 = 0, the negative edge of the $\overline{ODS}$ input clears the OBF flag.

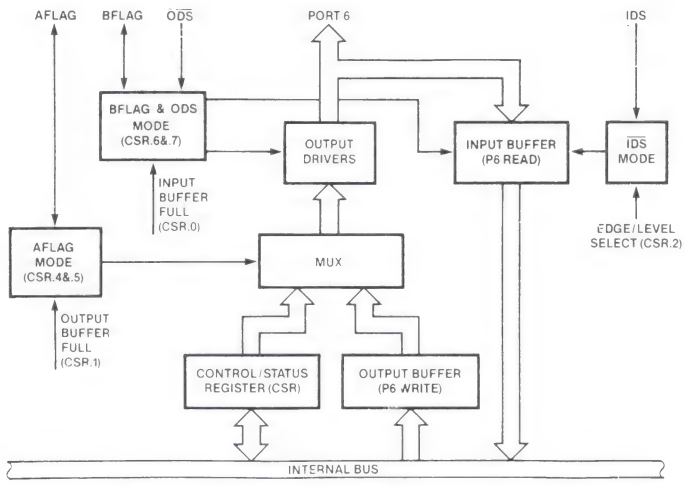



**Figure 1. Port 6 Block Diagram**

**CSR.4, CSR.5 — AFLAG Mode Select (MA0, MA1)**
Bits 4 and 5 select the mode of operation for the AFLAG pin, as follows:

| MA1 | MA0 | AFLAG Function |
|---|---|---|
| 0 | 0 | Logic 0 output |
| 0 | 1 | Logic 1 output |
| 1 | 0 | OBF flag output (CSR.1) |
| 1 | 1 | Select (SEL) input mode |

The select (SEL) input mode is used to determine whether the port 6 data register or the control status register is output on port 6. When the select feature is enabled, the AFLAG input controls the source of port 6 output data. A logic 0 on AFLAG input selects the port 6 data register, and a logic 1 on AFLAG input selects the control status register.

**CSR.6, CSR.7 — BFLAG Mode Select (MB0, MB1)**
Bits 6 and 7 select the mode of operation for the BFLAG pin, as follows:

| MB1 | MB0 | BFLAG Function |
|---|---|---|
| 0 | 0 | Logic 0 output |
| 0 | 1 | Logic 1 output |
| 1 | 0 | IBF flag output (CSR.0) |
| 1 | 1 | Port enable ($\overline{PE}$) |

In the port enable mode, $\overline{IDS}$ and $\overline{ODS}$ inputs are disabled when BFLAG input is High. When the BFLAG input is Low, the port is enabled for I/O.

## CONTROL STATUS REGISTER

| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| (CSR) | MB1 | MB0 | MA1 | MA0 | OBFC | IDSM | OBF | IBF |
| | BFLAG mode select | | AFLAG mode select | | Output buffer flag clear mode | Input data strobe mode | Output buffer full flag | Input buffer full flag |
| | 0/0 = Logic 0 output*<br>0/1 = Logic 1 output*<br>1/0 = IBF output<br>1/1 = $\overline{PE}$ input<br>(0 = Select)<br>(1 = disable I/O) | | 0/0 = Logic 0 output<br>0/1 = Logic 1 output<br>1/0 = OBF output*<br>1/1 = SEL input<br>(0 = Data)<br>(1 = Control/status) | | 0 = Negative edge of $\overline{ODS}$<br>1 = Positive edge of $\overline{ODS}$ | 0 = Positive edge of $\overline{IDS}$<br>1 = Low level of $\overline{IDS}$ | 0 = Output data buffer empty<br>1 = Output data buffer full | 0 = Input data buffer empty<br>1 = input data buffer full |

* Output–always mode: MB1 = 0, MA1 = 1, and MA0 = 0. In this mode port 6 is always enabled for output. $\overline{ODS}$ only clears the OBF flag.

**Table 1. Special Function Register Addresses**

| REGISTER ADDRESS | | | BIT ADDRESS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Name | Symbol | Address | MSB | | | | | | | LSB |
| Port 4 | P4 | C0 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Port 5 | P5 | C8 | CF | CE | CD | CC | CB | CA | C9 | C8 |
| Port 6 data | P6 | D8 | DF | DE | DD | DC | DB | DA | D9 | D8 |
| Port 6 control status | CSR | E8 | EF | EE | ED | EC | EB | EA | E9 | E8 |

## SPECIAL FUNCTION REGISTER ADDRESSES

Special function register addresses for the 87C451 are identical to those of the 80C51, except for the additional registers listed in Table 1.

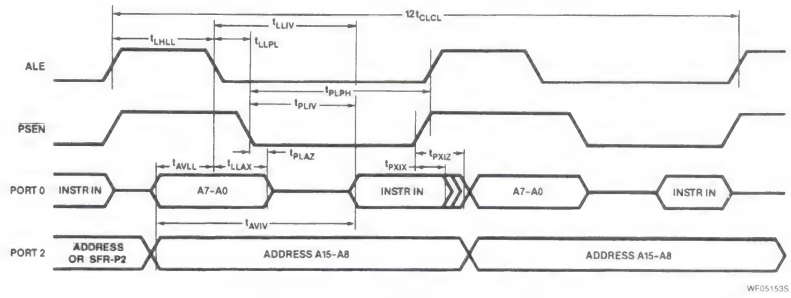



**Figure 2. Program Memory Read Cycle**

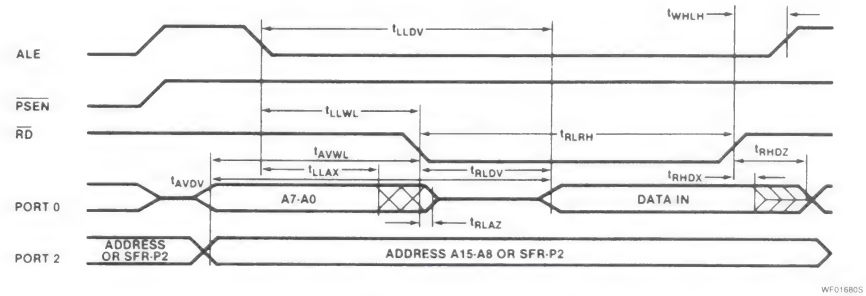



**Figure 3. Data Memory Read Cycle**

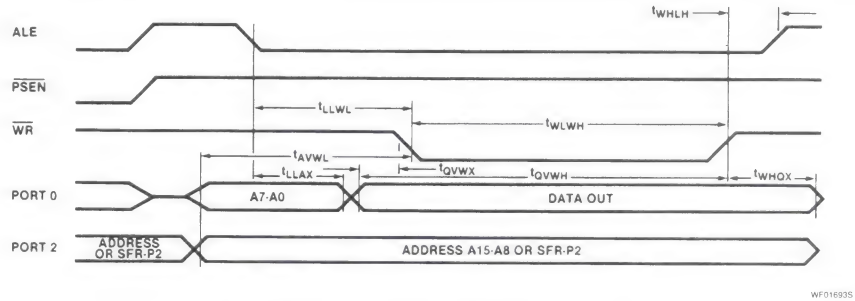



**Figure 4. Data Memory Write Cycle**

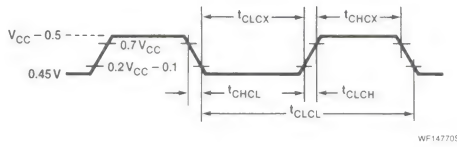
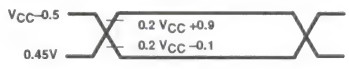



**Figure 5. External Clock Drive Waveform**




**NOTE:**
AC inputs during testing are driven at $V_{CC}$–0.5V for a logic "1" and 0.45 for a logic "0". Timing measurements are made at $V_{IH\,MIN}$ for a logic "1" and $V_{IL\,MAX}$ for a logic "0".

**Figure 6. AC Testing Input, Output Waveforms**

**NOTE:**
For timing purposes a port pin is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OL}/I_{OH} > \pm 20$mA.

**Figure 7. Float Waveforms**

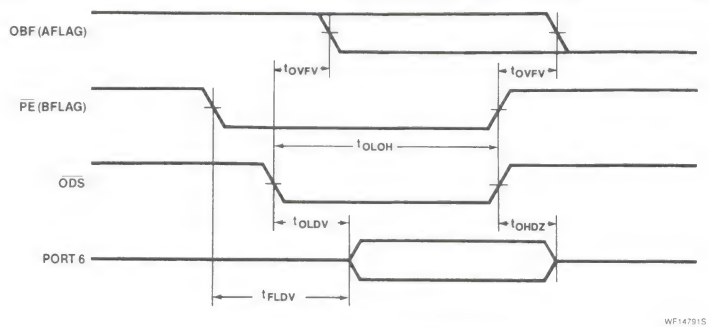



**Figure 8. Port 6. Output Waveforms**

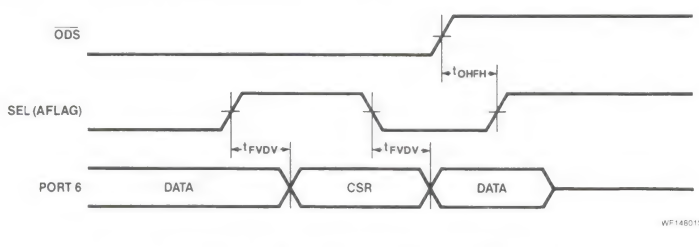



**Figure 9. Port 6 Select Mode Waveforms**

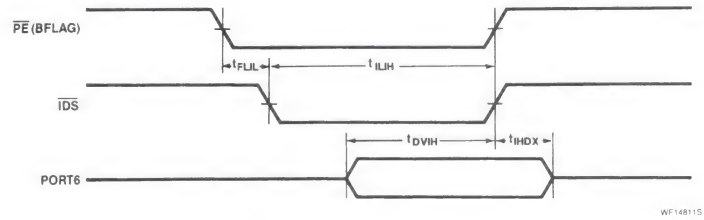



Figure 10. Port 6 Input Waveforms

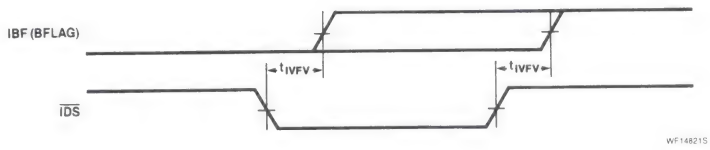
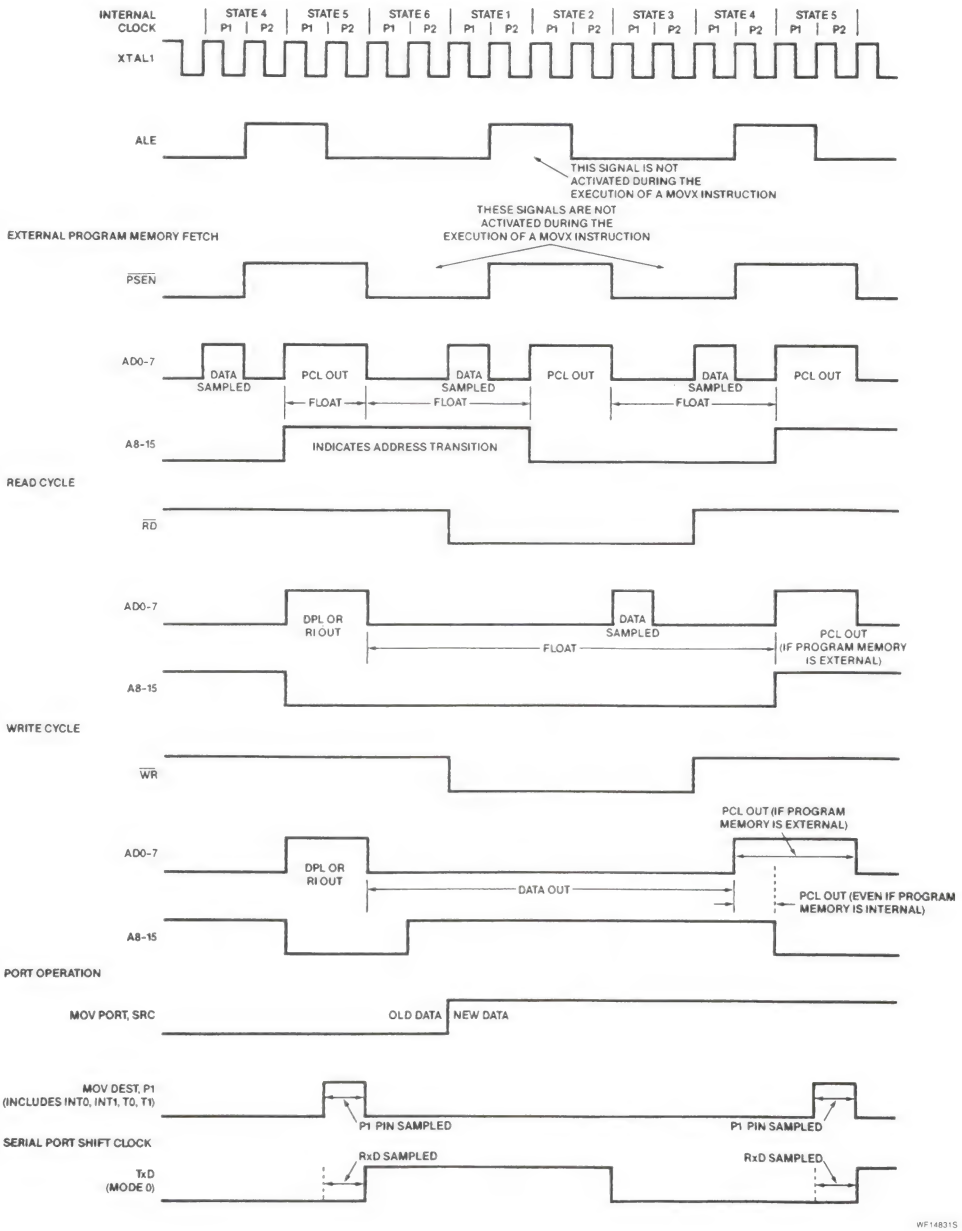



Figure 11. IBF Flag Output Waveforms




NOTE:
This diagram indicates when signals are clocked internally, however, the time it takes the signals to propagate to the pins ranges from 25ns to 125ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically ($T_A$ = 25°C, fully loaded), $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns; propagation delays for other signals are approximately 85ns. These timing delays are incorporated in the AC specifications.

**Figure 12. Timing Waveforms**

# CMOS Single-Chip 8-Bit EPROM Microcontroller | 87C451

## EPROM CHARACTERISTICS

The 87C451 is programmed by a modified quick–pulse programming ™algorithm. It differs from older methods in the value used for $V_{PP}$ (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C451 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C451 manufactured by Signetics.

Table 2 shows the logic levels for reading the signature byte, and for programming the program memory, the Encryption Table, and the lock bits. The circuits configuration and waveforms for quick–pulse programming are shown in Figures 13 and 14. Figure 15 shows the circuit configuration for normal program memory verification.

## QUICK–PULSE PROGRAMMING™

The setup for microcontroller quick–pulse programming is shown in Figure 13. Note that the 87C451 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 13. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of port 2 and 3 specified in Table 2 are held at the "Program Code Data" levels indicated in Table 2. The ALE/$\overline{PROG}$ is pulsed Low 25 times as shown in Figure 14.

To program the Encryption Table, repeat the 25–pulse programming sequence for addresses 0 through 1FH, using the "Pgm Encryption Table" levels. Do not forget that after the Encryption Table is programmed, verify cycles will produce only encrypted data.

To program the lock bits, repeat the 25–pulse programming sequence using the "Pgm Lock Bit" levels. After one lock bit is programmed, further programming of the code memory and Encryption Table is disabled. However, the other lock bit can still be programmed.

Note that the $\overline{EA}$/$V_{PP}$ pin must not be allowed to go above the maximum specified $V_{PP}$ level for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The $V_{PP}$ source should be well regulated and free of glitches and overshoot.

## Program Verification

If Lock Bit 2 has not been programmed, the on–chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 15. The other pins are held at the "Verify Code Data" levels indicated in Table 2. The contents of the addressed location will be emitted on port 0. External pull–ups are required on port 0 for this operation.

If the Encryption Table has been programmed, the data presented at port 0 will be the Exclusive–NOR of the program byte with one of the encryption bytes. The user will have to know the Encryption Table contents in order to correctly decode the verification data. The Encryption Table itself cannot be read out.

## Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic Low. The values are:

(030H) = 89H indicates manufactured by Signetics

(031H) = 57H indicates 87C451

## Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 2, and which satisfies the timing specifications, is suitable.

## Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose of at least 15W–sec/cm$^2$. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm$^2$ rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in all 1s state.

**Table 2. EPROM Programming Modes**

| MODE | RST | $\overline{PSEN}$ | ALE/$\overline{PROG}$ | $\overline{EA}$/$V_{PP}$ | P2.7 | P2.6 | P3.7 | P3.6 |
|---|---|---|---|---|---|---|---|---|
| Read Signature | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| Program Code Data | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 1 |
| Verify Code Data | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| Pgm Encryption Table | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 0 |
| Pgm Lock Bit 1 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 1 | 1 |
| Pgm Lock Bit 2 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 0 | 0 |

**NOTES:**
"1" = Valid High for that pin.
"0" = Valid Low for that pin.
$V_{PP}$ = 12.75V ± 0.25V.
$V_{CC}$ = 5V ± 10% during programming and verification.
* ALE/$\overline{PROG}$ receives 25 programming pulses while $V_{PP}$ is held at 12.75V. Each programming pulse is Low for 100µs (± 10µs) and High for a minimum of 10µs.

™ Quick-pulse programming is a phrase trademark of Intel Corp.

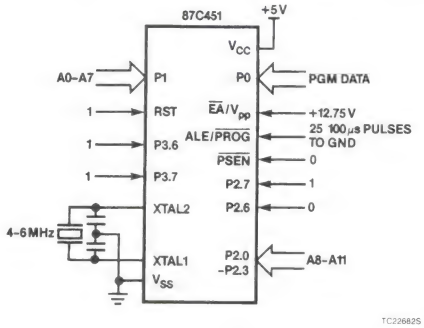



Figure 13. Programming Configuration

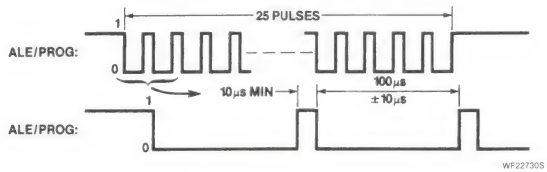



Figure 14. $\overline{PROG}$ Waveforms

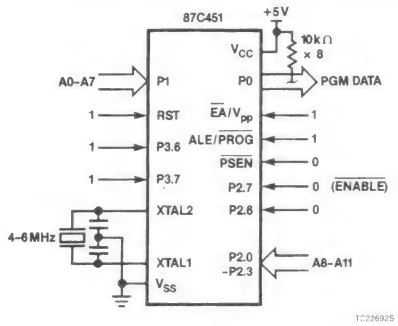
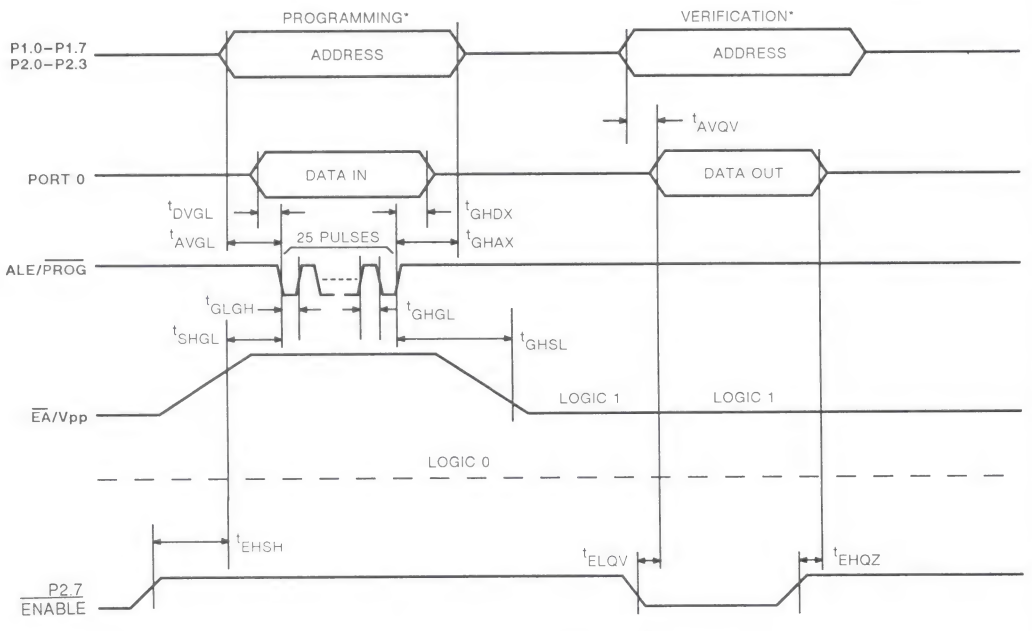



Figure 15. Program Verification

## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS $T_A$ = 21°C to 27°C, $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{PP}$ | Programming supply voltage | 12.5 | 13.0 | V |
| $I_{PP}$ | Programming supply current | | 50 | mA |
| $1/t_{CLCL}$ | Oscillator frequency | 4 | 6 | MHz |
| $t_{AVGL}$ | Address setup to $\overline{PROG}$ Low | $48t_{CLCL}$ | | |
| $t_{GHAX}$ | Address hold after $\overline{PROG}$ | $48t_{CLCL}$ | | |
| $t_{DVGL}$ | Data setup to $\overline{PROG}$ Low | $48t_{CLCL}$ | | |
| $t_{GHDX}$ | Data hold after $\overline{PROG}$ | $48t_{CLCL}$ | | |
| $t_{EHSH}$ | P2.7 ($\overline{ENABLE}$) High to $V_{PP}$ | $48t_{CLCL}$ | | |
| $t_{SHGL}$ | $V_{PP}$ setup to $\overline{PROG}$ Low | 10 | | µs |
| $t_{GHSL}$ | $V_{PP}$ hold after $\overline{PROG}$ | 10 | | µs |
| $t_{GLGH}$ | $\overline{PROG}$ width | 90 | 110 | µs |
| $t_{AVQV}$ | Address to data valid | | $48t_{CLCL}$ | |
| $t_{ELQV}$ | $\overline{ENABLE}$ Low to data valid | | $48t_{CLCL}$ | |
| $t_{EHQZ}$ | Data float after $\overline{ENABLE}$ | 0 | $48t_{CLCL}$ | |
| $t_{GHGL}$ | $\overline{PROG}$ High to $\overline{PROG}$ Low | 10 | | µs |




*FOR PROGRAMMING VERIFICATION SEE FIGURE 18.
FOR VERIFICATION CONDITIONS SEE FIGURE 20.

**Figure 16. EPROM Programming and Verification Waveforms**

**Table 3. Instruction Set**

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Arithmetic operations** | | | | |
| ADD | A,Rn | Add register to accumulator | 1 | 1 |
| ADD | A,direct | Add direct byte to accumulator | 2 | 1 |
| ADD | A,@Ri | Add indirect RAM to accumulator | 1 | 1 |
| ADD | A,R#data | Add immediate data to accumulator | 2 | 1 |
| ADDC | A,Rn | Add register to accumulator with carry | 1 | 1 |
| ADDC | A,direct | Add direct byte to A with carry flag | 2 | 1 |
| ADDC | A,@Ri | Add indirect RAM to A with carry flag | 1 | 1 |
| ADDC | A,#data | Add immediate data to A with carry flag | 2 | 1 |
| SUBB | A,Rn | Subtract register from A with borrow | 1 | 1 |
| SUBB | A,direct | Subtract direct byte from A with borrow | 2 | 1 |
| SUBB | A,@Ri | Subtract indirect RAM from A w/borrow | 1 | 1 |
| SUBB | A,#data | Subtract immed. data from A w/borrow | 2 | 1 |
| INC | A | Increment accumulator | 1 | 1 |
| INC | Rn | Increment register | 1 | 1 |
| INC | direct | Increment direct byte | 2 | 1 |
| INC | @Ri | Increment indirect RAM | 1 | 1 |
| DEC | A | Decrement accumulator | 1 | 1 |
| DEC | Rn | Decrement register | 1 | 1 |
| DEC | direct | Decrement direct byte | 2 | 1 |
| DEC | @Ri | Decrement indirect RAM | 1 | 1 |
| INC | DPTR | Increment data pointer | 1 | 2 |
| MUL | AB | Multiply A & B | 1 | 4 |
| DIV | AB | Divide A by B | 1 | 4 |
| DA | A | Decimal adjust accumulator | 1 | 1 |
| **Logical operations** | | | | |
| ANL | A,Rn | AND register to accumulator | 1 | 1 |
| ANL | A,direct | AND direct byte to accumulator | 2 | 1 |
| ANL | A,@Ri | AND indirect RAM to accumulator | 1 | 1 |
| ANL | A,#data | AND immediate data to accumulator | 2 | 1 |
| ANL | direct,A | AND accumulator to direct byte | 2 | 1 |
| ANL | direct,#data | AND immediate data to direct byte | 3 | 2 |
| ORL | A,Rn | OR register to accumulator | 1 | 1 |
| ORL | A,direct | OR direct byte to accumulator | 2 | 1 |
| ORL | A,@Ri | OR indirect RAM to accumulator | 1 | 1 |
| ORL | A,#data | OR immediate data to accumulator | 2 | 1 |
| ORL | direct,A | OR accumulator to direct byte | 2 | 1 |
| ORL | direct,#data | OR immediate data to direct byte | 3 | 2 |
| XRL | A,Rn | Exclusive–OR register to accumulator | 1 | 1 |
| XRL | A,direct | Exclusive–OR direct byte to accumulator | 2 | 1 |
| XRL | A,@Ri | Exclusive–OR indirect RAM to A | 1 | 1 |
| XRL | A,#data | Exclusive–OR immediate data to A | 2 | 1 |
| XRL | direct,A | Exclusive–OR accumulator to direct byte | 2 | 1 |
| XRL | direct,#data | Exclusive–OR immediate data to direct | 3 | 2 |
| CLR | A | Clear accumulator | 1 | 1 |
| CPL | A | Complement accumulator | 1 | 1 |
| RL | A | Rotate accumulator left | 1 | 1 |
| RLC | A | Rotate A left through the carry flag | 1 | 1 |
| RR | A | Rotate accumulator right | 1 | 1 |
| RRC | A | Rotate A right through carry flag | 1 | 1 |
| SWAP | A | Swap nibbles within the accumulator | 1 | 1 |
| **Data transfer** | | | | |
| MOV | A,Rn | Move register to accumulator | 1 | 1 |
| MOV | A,direct | Move direct byte to accumulator | 2 | 1 |
| MOV | A,@Ri | Move indirect RAM to accumulator | 1 | 1 |
| MOV | A,#data | Move immediate data to accumulator | 2 | 1 |
| MOV | Rn,A | Move accumulator to register | 1 | 1 |
| MOV | Rn,direct | Move direct byte to register | 2 | 2 |
| MOV | Rn,#data | Move immediate data to register | 2 | 1 |
| MOV | direct,A | Move accumulator to direct byte | 2 | 1 |
| MOV | direct,Rn | Move register to direct byte | 2 | 2 |
| MOV | direct,direct | Move direct byte to direct | 3 | 2 |
| MOV | direct,@Ri | Move indirect RAM to direct byte | 2 | 2 |
| MOV | direct,#data | Move immediate data to direct byte | 3 | 2 |
| MOV | @Ri,A | Move accumulator to indirect RAM | 1 | 1 |
| MOV | @Ri,direct | Move direct byte to indirect RAM | 2 | 2 |

**Table 2. Instruction Set** (Continued)

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Data transfer (continued)** | | | | |
| MOV | @Ri,#data | Move immediate data to indirect RAM | 2 | 1 |
| MOV | DPTR,#data16 | Load data pointer with a 16–bit constant | 3 | 2 |
| MOVC | A,@A + DPTR | Move code byte relative to DPTR to A | 1 | 2 |
| MOVC | A,@A + PC | Move code byte relative to PC to A | 1 | 2 |
| MOVX | A,@Ri | Move external RAM (8–bit addr) to A | 1 | 2 |
| MOVX | A,@DPTR | Move external RAM (16–bit addr) to A | 1 | 2 |
| MOVX | @Ri,A | Move A to external RAM (8–bit addr) | 1 | 2 |
| MOVX | @DPTR,A | Move A to external RAM (16–bit addr) | 1 | 2 |
| PUSH | direct | Push direct byte onto stack | 2 | 2 |
| POP | direct | Pop direct byte from stack | 2 | 2 |
| XCH | A,Rn | Exchange register with accumulator | 1 | 1 |
| XCH | A,direct | Exchange direct byte with accumulator | 2 | 1 |
| XCH | A,@Ri | Exchange indirect RAM with A | 1 | 1 |
| XCHD | A,#Ri | Exchange low–order digit ind. RAM w/A | 1 | 1 |
| **Boolean variable manipulation** | | | | |
| CLR | C | Clear carry flag | 1 | 1 |
| CLR | bit | Clear direct bit | 2 | 1 |
| SETB | C | Set carry flag | 1 | 1 |
| SETB | bit | Set direct bit | 2 | 1 |
| CPL | C | Complement carry flag | 1 | 1 |
| CPL | bit | Complement direct bit | 2 | 1 |
| ANL | C,bit | AND direct bit to carry flag | 2 | 2 |
| ANL | C,/bit | AND complement of direct bit to carry | 2 | 2 |
| ORL | C,bit | OR direct bit to carry flag | 2 | 2 |
| ORL | C,/bit | OR complement of direct bit to carry | 2 | 2 |
| MOV | C,bit | Move direct bit to carry flag | 2 | 1 |
| MOV | bit,C | Move carry flag to direct bit | 2 | 2 |
| **Program and machine control** | | | | |
| ACALL | addr11 | Absolute subroutine call | 2 | 2 |
| LCALL | addr16 | Long subroutine call | 3 | 2 |
| RET | | Return from subroutine | 1 | 2 |
| RETI | | Return from interrupt | 1 | 2 |
| AJMP | addr11 | Absolute jump | 2 | 2 |
| LJMP | addr16 | Long jump | 3 | 2 |
| SJMP | rel | Short jump (relative addr) | 2 | 2 |
| JMP | @A + DPTR | Jump indirect relative to the DPTR | 1 | 2 |
| JZ | rel | Jump if accumulator is zero | 2 | 2 |
| JNZ | rel | Jump if accumulator is not zero | 2 | 2 |
| JC | rel | Jump if carry flag is set | 2 | 2 |
| JNC | rel | Jump if no carry flag | 2 | 2 |
| JB | bit,rel | Jump if direct bit set | 3 | 2 |
| JNB | bit,rel | Jump if direct bit not set | 3 | 2 |
| JBC | bit,rel | Jump if direct bit is set & clear bit | 3 | 2 |
| CJNE | A,direct,rel | Compare direct to A & jump if not equal | 3 | 2 |
| CJNE | A,#data,rel | Comp. immed. to A & jump if not equal | 3 | 2 |
| CJNE | Rn,#data,rel | Comp. immed. to reg. & jump if not equal | 3 | 2 |
| CJNE | @Ri,#data,rel | Comp. immed. to ind. & jump if not equal | 3 | 2 |
| DJNZ | Rn,rel | Decrement register & jump if not zero | 2 | 2 |
| DJNZ | direct,rel | Decrement direct & jump if not zero | 3 | 2 |
| NOP | | No operation | 1 | 1 |

**Notes on data addressing modes:**

Rn –Working register R0–R7
direct –128 internal RAM locations, any I/O port, control or status register
@Ri –Indirect internal RAM location addressed by register R0 or R1
#data –8–bit constant included in instruction
#data16 –16–bit constant included as bytes 2 & 3 of instruction
bit –128 software flags, any I/O pin, control or status bit

**Notes on program addressing modes:**

addr16 –Destination address for LCALL & LJMP may be anywhere within the 64–kilobyte program memory address space.
addr11 –Destination address for ACALL & AJMP will be within the same 2–kilobyte page of program memory as the first byte of the following instruction.
rel –SJMP and all conditional jumps include an 8–bit offset byte. Range is + 127 – 128 bytes relative to first byte of the following instruction.

**Table 4. Instruction Opcodes in Hexadecimal Order**

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 00 | 1 | NOP | |
| 01 | 2 | AJMP | code addr |
| 02 | 3 | LJMP | code addr |
| 03 | 1 | RR | A |
| 04 | 1 | INC | A |
| 05 | 2 | INC | data addr |
| 06 | 1 | INC | @R0 |
| 07 | 1 | INC | @R1 |
| 08 | 1 | INC | R0 |
| 09 | 1 | INC | R1 |
| 0A | 1 | INC | R2 |
| 0B | 1 | INC | R3 |
| 0C | 1 | INC | R4 |
| 0D | 1 | INC | R5 |
| 0E | 1 | INC | R6 |
| 0F | 1 | INC | R7 |
| 10 | 3 | JBC | bit addr, code addr |
| 11 | 2 | ACALL | code addr |
| 12 | 3 | LCALL | code addr |
| 13 | 1 | RRC | A |
| 14 | 1 | DEC | A |
| 15 | 2 | DEC | data addr |
| 16 | 1 | DEC | @R0 |
| 17 | 1 | DEC | @R1 |
| 18 | 1 | DEC | R0 |
| 19 | 1 | DEC | R1 |
| 1A | 1 | DEC | R2 |
| 1B | 1 | DEC | R3 |
| 1C | 1 | DEC | R4 |
| 1D | 1 | DEC | R5 |
| 1E | 1 | DEC | R6 |
| 1F | 1 | DEC | R7 |
| 20 | 3 | JB | bit addr, code addr |
| 21 | 2 | AJMP | code addr |
| 22 | 1 | RET | |
| 23 | 1 | RL | A |
| 24 | 2 | ADD | A,#data |
| 25 | 2 | ADD | A,data addr |
| 26 | 1 | ADD | A,@R0 |
| 27 | 1 | ADD | A,@R1 |
| 28 | 1 | ADD | A,R0 |
| 29 | 1 | ADD | A,R1 |
| 2A | 1 | ADD | A,R2 |
| 2B | 1 | ADD | A,R3 |
| 2C | 1 | ADD | A,R4 |
| 2D | 1 | ADD | A,R5 |
| 2E | 1 | ADD | A,R6 |
| 2F | 1 | ADD | A,R7 |
| 30 | 3 | JNB | bit addr, code addr |
| 31 | 2 | ACALL | code addr |
| 32 | 1 | RETI | |
| 33 | 1 | RLC | A |
| 34 | 2 | ADDC | A,#data |
| 35 | 2 | ADDC | A,data addr |
| 36 | 1 | ADDC | A,@R0 |
| 37 | 1 | ADDC | A,@R1 |
| 38 | 1 | ADDC | A,R0 |
| 39 | 1 | ADDC | A,R1 |
| 3A | 1 | ADDC | A,R2, |
| 3B | 1 | ADDC | A,R3 |
| 3C | 1 | ADDC | A,R4 |
| 3D | 1 | ADDC | A,R5 |
| 3E | 1 | ADDC | A,R6 |
| 3F | 1 | ADDC | A,R7 |
| 40 | 2 | JC | code addr |
| 41 | 2 | AJMP | code addr |
| 42 | 2 | ORL | data addr,A |
| 43 | 3 | ORL | data addr,#data |
| 44 | 2 | ORL | A,#data |
| 45 | 2 | ORL | A,data addr |
| 46 | 1 | ORL | A,@R0 |
| 47 | 1 | ORL | A,@R1 |
| 48 | 1 | ORL | A,R0 |
| 49 | 1 | ORL | A,R1 |
| 4A | 1 | ORL | A,R2 |
| 4B | 1 | ORL | A,R3 |
| 4C | 1 | ORL | A,R4 |
| 4D | 1 | ORL | A,R5 |
| 4E | 1 | ORL | A,R6 |
| 4F | 1 | ORL | A,R7 |
| 50 | 2 | JNC | code addr |
| 51 | 2 | ACALL | code addr |
| 52 | 2 | ANL | data addr,A |
| 53 | 3 | ANL | data addr,#data |
| 54 | 2 | ANL | A,#data |
| 55 | 2 | ANL | A,data addr |
| 56 | 1 | ANL | A,@R0 |
| 57 | 1 | ANL | A,@R1 |
| 58 | 1 | ANL | A,R0 |
| 59 | 1 | ANL | A,R1 |
| 5A | 1 | ANL | A,R2 |
| 5B | 1 | ANL | A,R3 |
| 5C | 1 | ANL | A,R4 |
| 5D | 1 | ANL | A,R5 |
| 5E | 1 | ANL | A,R6 |
| 5F | 1 | ANL | A,R7 |
| 60 | 2 | JZ | code addr |
| 61 | 2 | AJMP | code addr |
| 62 | 2 | XRL | data addr,A |
| 63 | 3 | XRL | data addr,#data |
| 64 | 2 | XRL | A,#data |
| 65 | 2 | XRL | A,data addr |
| 66 | 1 | XRL | A,@R0 |
| 67 | 1 | XRL | A,@R1 |
| 68 | 1 | XRL | A,R0 |
| 69 | 1 | XRL | A,R1 |
| 6A | 1 | XRL | A,R2 |
| 6B | 1 | XRL | A,R3 |
| 6C | 1 | XRL | A,R4 |
| 6D | 1 | XRL | A,R5 |
| 6E | 1 | XRL | A,R6 |
| 6F | 1 | XRL | A,R7 |
| 70 | 2 | JNZ | code addr |
| 71 | 2 | ACALL | code addr |
| 72 | 2 | ORL | C,bit addr |
| 73 | 1 | JMP | @A + DPTR |
| 74 | 2 | MOV | A,#data |
| 75 | 3 | MOV | data addr,#data |
| 76 | 2 | MOV | @R0,#data |
| 77 | 2 | MOV | @R1,#data |
| 78 | 2 | MOV | R0,#data |
| 79 | 2 | MOV | R1,#data |
| 7A | 2 | MOV | R2,#data |
| 7B | 2 | MOV | R3,#data |
| 7C | 2 | MOV | R4,#data |
| 7D | 2 | MOV | R5,#data |
| 7E | 2 | MOV | R6,#data |
| 7F | 2 | MOV | R7,#data |

**Table 3. Instruction Opcodes in Hexadecimal Order** (Continued)

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 80 | 2 | SJMP | code addr |
| 81 | 2 | AJMP | code addr |
| 82 | 2 | ANL | C,bit addr |
| 83 | 1 | MOVC | A,@A + PC |
| 84 | 1 | DIV | AB |
| 85 | 3 | MOV | data addr,data addr |
| 86 | 2 | MOV | data addr,@R0 |
| 87 | 2 | MOV | data addr,@R1 |
| 88 | 2 | MOV | data addr,R0 |
| 89 | 2 | MOV | data addr,R1 |
| 8A | 2 | MOV | data addr,R2 |
| 8B | 2 | MOV | data addr,R3 |
| 8C | 2 | MOV | data addr,R4 |
| 8D | 2 | MOV | data addr,R5 |
| 8E | 2 | MOV | data addr,R6 |
| 8F | 2 | MOV | data addr,R7 |
| 90 | 3 | MOV | DPTR,#data |
| 91 | 2 | ACALL | code addr |
| 92 | 2 | MOV | bit addr,C |
| 93 | 1 | MOVC | A,@A + DPTR |
| 94 | 2 | SUBB | A,#data |
| 95 | 2 | SUBB | A,data addr |
| 96 | 1 | SUBB | A,@R0 |
| 97 | 1 | SUBB | A,@R1 |
| 98 | 1 | SUBB | A,R0 |
| 99 | 1 | SUBB | A,R1 |
| 9A | 1 | SUBB | A,R2 |
| 9B | 1 | SUBB | A,R3 |
| 9C | 1 | SUBB | A,R4 |
| 9D | 1 | SUBB | A,R5 |
| 9E | 1 | SUBB | A,R6 |
| 9F | 1 | SUBB | A,R7 |
| A0 | 2 | ORL | C,/bit addr |
| A1 | 2 | AJMP | code addr |
| A2 | 2 | MOV | C,bit addr |
| A3 | 1 | INC | DPTR |
| A4 | 1 | MUL | AB |
| A5 | | reserved | |
| A6 | 2 | MOV | @R0,data addr |
| A7 | 2 | MOV | @R1,data addr |
| A8 | 2 | MOV | R0,data addr |
| A9 | 2 | MOV | R1,data addr |
| AA | 2 | MOV | R2,data addr |
| AB | 2 | MOV | R3,data addr |
| AC | 2 | MOV | R4,data addr |
| AD | 2 | MOV | R5,data addr |
| AE | 2 | MOV | R6,data addr |
| AF | 2 | MOV | R7,data addr |
| B0 | 2 | ANL | C,/bit addr |
| B1 | 2 | ACALL | code addr |
| B2 | 2 | CPL | bit addr |
| B3 | 1 | CPL | C |
| B4 | 3 | CJNE | A,#data,code addr |
| B5 | 3 | CJNE | A,data addr,code addr |
| B6 | 3 | CJNE | @R0,#data,code addr |
| B7 | 3 | CJNE | @R1,#data,code addr |
| B8 | 3 | CJNE | R0,#data,code addr |
| B9 | 3 | CJNE | R1,#data,code addr |
| BA | 3 | CJNE | R2,#data,code addr |
| BB | 3 | CJNE | R3,#data,code addr |
| BC | 3 | CJNE | R4,#data,code addr |
| BD | 3 | CJNE | R5#data,code addr |
| BE | 3 | CJNE | R6,#data,code addr |
| BF | 3 | CJNE | R7,#data,code addr |

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| C0 | 2 | PUSH | data addr |
| C1 | 2 | AJMP | code addr |
| C2 | 2 | CLR | bit addr |
| C3 | 1 | CLR | C |
| C4 | 1 | SWAP | A |
| C5 | 2 | XCH | A,data addr |
| C6 | 1 | XCH | A,@R0 |
| C7 | 1 | XCH | A,@R1 |
| C8 | 1 | XCH | A,R0 |
| C9 | 1 | XCH | A,R1 |
| CA | 1 | XCH | A,R2 |
| CB | 1 | XCH | A,R3 |
| CC | 1 | XCH | A,R4 |
| CD | 1 | XCH | A,R5 |
| CE | 1 | XCH | A,R6 |
| CF | 1 | XCH | A,R7 |
| D0 | 2 | POP | data addr |
| D1 | 2 | ACALL | code addr |
| D2 | 2 | SETB | bit addr |
| D3 | 1 | SETB | C |
| D4 | 1 | DA | A |
| D5 | 3 | DJNZ | data addr,code addr |
| D6 | 1 | XCHD | A,@R0 |
| D7 | 1 | XCHD | A,@R1 |
| D8 | 2 | DJNZ | R0,code addr |
| D9 | 2 | DJNZ | R1,code addr |
| DA | 2 | DJNZ | R2,code addr |
| DB | 2 | DJNZ | R3,code addr |
| DC | 2 | DJNZ | R4,code addr |
| DD | 2 | DJNZ | R5,code addr |
| DE | 2 | DJNZ | R6,code addr |
| DF | 2 | DJNZ | R7,code addr |
| E0 | 1 | MOVX | A,@ DPTR |
| E1 | 2 | AJMP | code addr |
| E2 | 1 | MOVX | A,@R0 |
| E3 | 1 | MOVX | A,@R1 |
| E4 | 1 | CLR | A |
| E5 | 2 | MOV | A,.data addr |
| E6 | 1 | MOV | A,@R0 |
| E7 | 1 | MOV | A,@R1 |
| E8 | 1 | MOV | A,R0 |
| E9 | 1 | MOV | A,R1 |
| EA | 1 | MOV | A,R2 |
| EB | 1 | MOV | A,R3 |
| EC | 1 | MOV | A,R4 |
| ED | 1 | MOV | A,R5 |
| EE | 1 | MOV | A,R6 |
| EF | 1 | MOV | A,R7 |
| F0 | 1 | MOVX | @ DPTR,A |
| F1 | 2 | ACALL | code addr |
| F2 | 1 | MOVX | @R0,A |
| F3 | 1 | MOVX | @R1,A |
| F4 | 1 | CPL | A |
| F5 | 2 | MOV | data addr,A |
| F6 | 1 | MOV | @R0,A |
| F7 | 1 | MOV | @R1,A |
| F8 | 1 | MOV | R0,A |
| F9 | 1 | MOV | R1,A |
| FA | 1 | MOV | R2,A |
| FB | 1 | MOV | R3,A |
| FC | 1 | MOV | R4,A |
| FD | 1 | MOV | R5,A |
| FE | 1 | MOV | R6,A |
| FF | 1 | MOV | R7,A |

Signetics

# 87C552

## Single-Chip 8-Bit Microcontroller With A/D, Capture/Compare Timer, High-Speed Outputs, PWM

*Objective Specification*

**Military**
**Customer Specific Products**

### DESCRIPTION

The 87C552 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C552 has the same instruction set as the 80C51. The 87C552 is an EPROM version of the 83C552.

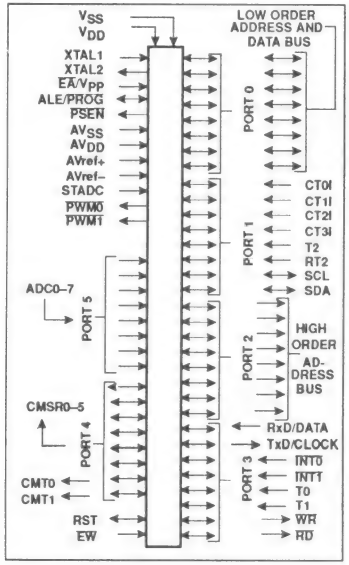
The 87C552 contains an 8K x 8 EPROM program memory, a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51, an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and $I^2C$-bus), a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C552 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1us and 40% in 2us. Multiply and divide instructions require 4us.

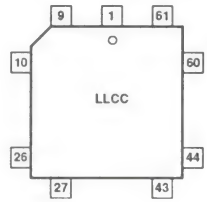
### FEATURES

- **80C51B central processing unit**
- **8K x 8 EPROM expandable externally to 64K bytes**
- **256 x 8 RAM, expandable externally to 64Kbytes**
- **Two standard 16-bit timer/counters**
- **An additional 16-bit timer/counter coupled to four capture registers and three compare registers**
- **Capable of producing 8 synchronized, timed outputs**
- **A 10-bit ADC with 8 multiplexed analog inputs**
- **Two 8-bit resolution, pulse width modulation outputs**
- **Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs**
- **$I^2C$-bus serial I/O port with byte oriented master and slave functions**
- **Full-duplex UART compatible with the standard 80C51**
- **On-chip watchdog timer**

### LOGIC SYMBOL




### PIN CONFIGURATION




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | P5.0/ADC0 | 35 | XTAL1 |
| 2 | $V_{DD}$ | 36 | $V_{SS}$ |
| 3 | STADC | 37 | $V_{SS}$ |
| 4 | $\overline{PWM0}$ | 38 | NC |
| 5 | $\overline{PWM1}$ | 39 | P2.0/A08 |
| 6 | $\overline{EW}$ | 40 | P2.1/A09 |
| 7 | P4.0/CMSR0 | 41 | P2.2/A10 |
| 8 | P4.1/CMRS1 | 42 | P2.3/A11 |
| 9 | P4.2CMSR2 | 43 | P2.3/A12 |
| 10 | P4.3/CMSR3 | 44 | P2.4/A13 |
| 11 | P4.4/CMSR4 | 45 | P2.6/A14 |
| 12 | P4.5/CMSR5 | 46 | P2.7/A15 |
| 13 | P4.6/CMT0 | 47 | $\overline{PSEN}$ |
| 14 | P4.7/CMT1 | 48 | ALE/$\overline{PROG}$ |
| 15 | RST | 49 | $\overline{EA}$/$V_{PP}$ |
| 16 | P1.0/CT01 | 50 | P0.7/AD7 |
| 17 | P1.1/CT1I | 51 | P0.6/AD6 |
| 18 | P1.2/CT2I | 52 | P0.5/AD5 |
| 19 | P1.3/CT3I | 53 | P0.4/AD4 |
| 20 | P1.4/T2 | 54 | P0.3/AD3 |
| 21 | P1.5/RT2 | 55 | P0.2/AD2 |
| 22 | P1.6/SCL | 56 | P0.1/AD1 |
| 23 | P1.7/SDA | 57 | P0.0/AD0 |
| 24 | P3.0/RxD | 58 | AVref– |
| 25 | P3.1TxD | 59 | AVref+ |
| 26 | P3.2/$\overline{INT0}$ | 60 | $AV_{SS}$ |
| 27 | P3.3/$\overline{INT1}$ | 61 | $AV_{DD}$ |
| 28 | P3.4/T0 | 62 | P5.7/ADC7 |
| 29 | P3.5/T1 | 63 | P5.6/ADC6 |
| 30 | P3.6/$\overline{WR}$ | 64 | P5.5/ADC5 |
| 31 | P3.7/$\overline{RD}$ | 65 | P5.4/ADC4 |
| 32 | NC | 66 | P5.3/ADC3 |
| 33 | NC | 67 | P5.2/ADC2 |
| 34 | XTAL2 | 68 | P5.1/ADC1 |

Signetics

# 87C751

## CMOS Single-Chip 8-Bit Microcontroller

*Objective Specification*

**Military**
**Customer Specific Products**

### DESCRIPTION

The Signetics 87C751 offers many of the advantages of the 80C51 architecture in a small package and at low cost.

The 87C751 Microcontroller is fabricated with Signetics high-density CMOS technology. Signetics expitaxial substrate minimizes CMOS latch-up sensitivity.

The 87C751 contains a 2K x 8 EPROM, 64 x 8 RAM, 19 I/O lines, a 16-bit auto-reload counter/timer, a fixed-rate timer, a five-source fixed-priority interrupt structure, a bidirectional Inter-Intergrated Circuit ($I^2C$) serial bus interface, and an on-chip oscillator.

The onboard inter-integrated circuit ($I^2C$) bus interface allows the 87C751 to operate as a master or slave device on the $I^2C$ on the $I^2C$ small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated $I^2C$ peripherals.

### ORDERING INFORMATION

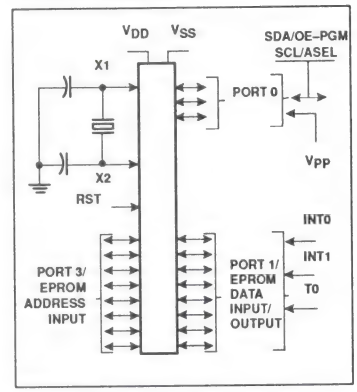
| PACKAGE | ORDER CODE |
|---|---|
| 24–Pin ceramic DIP 300mil-wide with quartz window | 87C751/BLA |
| 24–Pin ceramic DIP 300mil–wide w/o quartz window | 87C751/BLA OT[1] |

NOTE:
1. Erase characteristics do not apply for one time programming (OT).

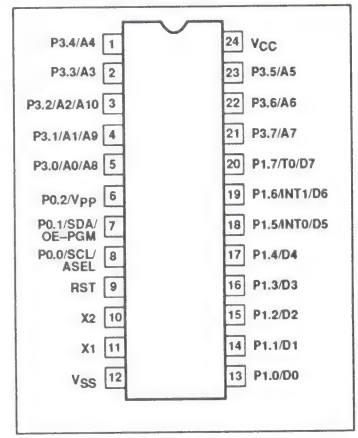
### FEATURES

- **EPROM version of 83C751**
- **80C51 based architecture**
- **Inter-Integrated Circuit ($I^2C$) serial bus interface**
- **Small package sizes**
  - **24 pin DIP (300mil–wide "skinny DIP")**
- **Available in erasable quartz lid or one-time programmable ceramic package**
- **Wide oscillator frequency range**
- **Low power consumption:**
  - **Normal operation: less than 11mA @ 5V, 12MHz**
  - **Idle mode**
  - **Power-down mode**
- **2K x 8 EPROM, 64 x 8 RAM**
- **16-bit auto reloadable counter/timer**
- **Fixed-rate timer**
- **Boolean processor**
- **CMOS and TTL compatible**
- **Well suited for logic replacement, industrial applications, and state machine applications**
- **Field programmable using standard equipment**

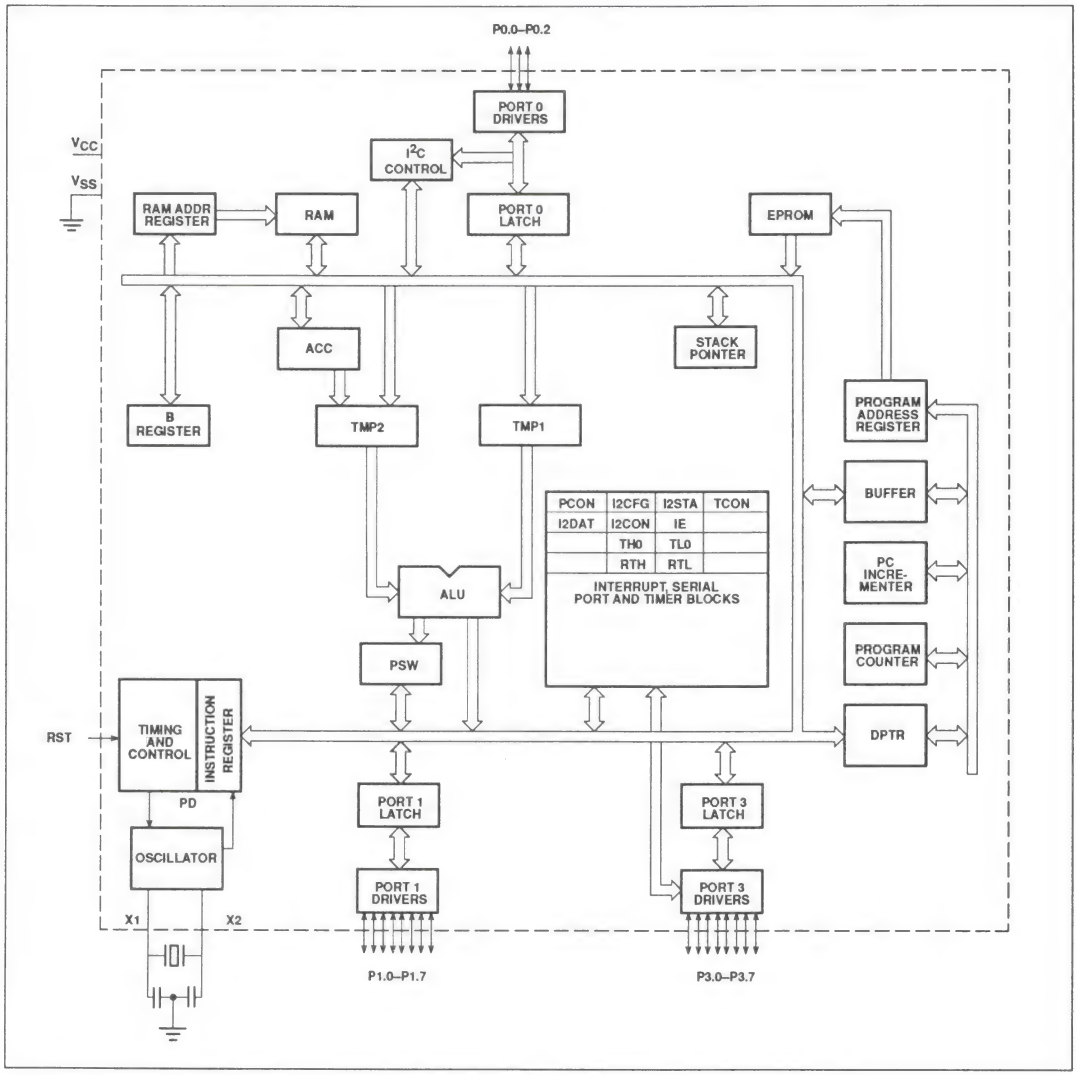
### LOGIC SYMBOL




### PIN CONFIGURATION



## BLOCK DIAGRAM



# CMOS Single-Chip 8-Bit Microcontroller — 87C751

## PIN CONFIGURATION

| MNEMONIC | PIN NO. | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| $V_{SS}$ | 12 | I | **Circuit ground potential.** |
| $V_{CC}$ | 24 | I/O | **Supply voltage during normal, idle, and power-down operation.** |
| P0.0–P0.2 | 8–6 | I/O | **Port 0:** Port 0 is a 3-bit open-drain bidirectional port. Port 0 pins that have ones written to them float, and in that state can be used as high-impedance inputs. Port 0 also serves as the serial $I^2C$ interface as shown in the pinout diagram. When this feature is activated by software, SCL and SDA are driven low in accordance with the 12C protocol. These pins are driven low if the port register bit is written with a 0 or if the $I^2C$ subsystem presents a 0. The state of the pin can always be read from the port register by the program. |
| | 7 | I/O | To comply with the $I^2C$ specification, P0.0 and P0.1 are open drain bidirectional I/O pins with the electrical characteristics listed in the tables that follow. While these differ from 'standard TTL' characteristics, they are close enough for the pins to still be used as general-purpose I/O in non-$I^2C$ applications. |
| | 8 | I/O | **SPA (P0.1)** $I^2C$ data.<br>**SCL (P0.0)** $I^2C$ clock.<br>Port 0 also provides alternate functions for programming the EPROM memory as follows: |
| | 8 | O | **P0.0/ASEL** – output which selects which byte of the EPROM address is to be applied to port 3.<br>P0.0 – 0 presents the low address byte to port 3.<br>P0.0 – 1 presents the high address byte to port 3 (only the three least significant bits are used). |
| | 7 | I | **P0.1/OE/PGM** – input, OE/PGM, which specifies verify mode (output enable) or the program mode.<br>OE/PGM – 1 output enabled (verify mode)<br>OE/PGM – 0 program mode. |
| | 6 | | **P0.2/$V_{PP}$** Programming voltage input. |
| P1.0–P1.7 | 13–20 | I/O | **Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have ones written to them are pulled high by the internal pullups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pullups. (See DC electrical characteristics: $I_{IL}$). Port 1 also serves the special function features of the 80C51 family as listed below: |
| | 18 | | **INT0 (P1.5):** External interrupt |
| | 19 | | **INT1 (P1.6):** External interrupt |
| | 20 | | **T0 (P1.7):** Timer 0 external input |
| | | | Port 1 serves to output the addressed EPROM contents in the verify mode and accepts as inputs the value to program into the selected address during the program mode. |
| P3.0–P3.7 | 5–1<br>23–21 | I/O | **Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have ones written to them are pulled and can be used as inputs. As inputs, port 3 pins that are external ly being pulled low will source current because of the pullups (See DC electrical characteristics: $I_{IL}$). Port 3 also functions as the address input for the EPROM memory location to be programmed (or verified) . The 11-bit address is multiplexed into this port as specified by P0.0. |
| RST | 9 | I | **Reset:** A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on RESET using only an external capacitor to $V_{CC}$. After the device is reset, a 10-bit serial sequence, sent LSB first, applied to RESET places the device in the programming state allowing programming address, data and $V_{PP}$ to be applied for programming or verification purposes. The RESET serial sequence must be synchronized with the X1 input. |
| X1 | 11 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. X1 also serves as the clock to strobe in a serial bit stream into RESET to place the device in the programming state. |
| X2 | 10 | O | **Crystal:** Output from the inverting oscillator amplifier. |

## OSCILLATOR CHARACTERISTIC

X1 and X2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, X1 should be driven while X2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

## IDLE MODE

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

## POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

## DESIGN CONSIDERATIONS

At power-down, the voltage on $V_{CC}$ and RST must come up at the same time for a proper start-up. Before entering the power-down mode, the contents of the carry bit and B.7 must be equal (See Table 1).

### Table 1. External Pin Status During Idle and Power-Down Modes

| Mode | Port 0 | Port 1 | Port 2 |
|---|---|---|---|
| Idle | Data | Data | Data |
| Power-down | Data | Data | Data |

## DIFFERENCES BETWEEN THE 87C751 AND THE 80C51

**Program Memory**

On the 87C751, program memory is 2048 bytes long and is not externally expandable. Program memory can contain 87C751 instructions and constant data. The only fixed locations in program memory are the addresses at which execution is taken up in response to reset and to interrupts, which are as follows:

| Event | Program Memory Address |
|---|---|
| Reset | 000 |
| External INT0 | 003 |
| Counter/timer 0 | 00B |
| External INT1 | 013 |
| Timer I | 01B |
| I²C serial | 023 |

**Counter/Timer Subsystem**

The 87C751 has one counter/timer called timer/counter 0. Its operation is similar to mode 2 operation on the 80C51, but is extended to 16 bits with 16 bits of autoload. The controls for this counter are centralized in a single register called TCON.

A watchdog timer, called Timer I, is for use with the I²C subsystem. In I²C applications, this timer is dedicated to time-generation and bus monitoring of the I²C. In non-I²C applications, it is available for use as a fixed timebase.

**Interrupt Subsytem - Fixed Priority**

The IP register and the 2-level interrupt system of the 80C51 are eliminated. Simultaneous interrupt conditions are resolved by a single-level, fixed priority as follows:

| | |
|---|---|
| Highest priority: | Pin INTO |
| | Counter/timer flag 0 |
| | Pin INT1 |
| | Timer I |
| Lowest priority: | Serial I²C |

**Serial Communications**

The 87C751 contains an I²C serial communications port instead of the 80C51 UART. The I²C serial port is a single bit hardware interface with all of the hardware necessary to support multi-master and slave operations. Also included are receiver digital filters and timer (timer I) for communication watch dog purposes. The I²C serial port is controlled through four special function registers; I²C control, I²C data, I²C status, and I²C configuration.

**Special Function Register Addresses**

Special function register addresses for the 87C751 are identical to those of the 80C51, except for the changes listed below:

80C51 special function registers not present in the 87C751 are TMOD (89), P2 (A0) and IP (B8). The 80C51 registers TH1, TL1, SCON, and SBUF are replaced with the 87C751 registers RTH, RTL, I2CON, and 12DAT, respectively. Additional special function registers are 12CFG-(D8) and 12STA-(FB).

### Table 2. I²C Special Function Register Addresses

| Register Address | | | Bit Address | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Name | Symbol | Address | MSB | | | | | | | LSB |
| I²C control | I2CON | 98 | 9F | 9E | 9D | 9C | 9B | 9A | 99 | 98 |
| I²C data | 12DAT | 99 | – | – | – | – | – | – | – | – |
| I²C configuration | 12CFG | D8 | DF | DE | DD | DC | DB | DA | D9 | D8 |
| I²C status | 12STA | F8 | FF | FE | FD | FC | FB | FA | F9 | F8 |

## ABSOLUTE MAXIMUM RATINGS [1,2]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Operating ambient temperature range[2] | –55 to +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 to + 150 | °C |
| $V_{CC}$ | Voltage from $V_{CC}$ to $V_{SS}$[3], except pin 6 | –0.5 to +6.5 | V |
| $V_{CC}$ | Voltage from Pin 6 to $V_{SS}$[3] | –0.5 to +13.0 | V |
| $V_S$ | Voltage from any pin to $V_{SS}$[3] | –0.5 to $V_{CC}$ +0.5 | V |
| $P_D$ | Power dissipation | 1.0 | W |

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le 125°C$, $4V \le V_{CC} \le 6.0V$, $V_{SS} = 0V$[3].

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IL}$ | Input low voltage, except SDA, SCL | | –0.5 | $0.2V_{CC}$–02.5 | V |
| $V_{IH}$ | Input high voltage, except X1, RST | | $0.2V_{CC}$+1.1 | $V_{CC}$+0.5 | V |
| $V_{IH1}$ | Input high voltage, X1, RST | | $0.7V_{CC}$+.2 | $V_{CC}$+0.5 | V |
| | SDA, SCL: | | | | |
| $V_{IL1}$ | Input low voltage | | –0.5 | $0.3V_{CC}$ | V |
| $V_{IL2}$ | Input high voltage | | $0.7V_{CC}$ | $V_{CC}$+0.5 | V |
| $V_{OL}$ | Output low voltage, ports 1 and 3 | $I_{OL}$ – 1.6mA | | 0.45 | V |
| $V_{OL1}$ | Output low voltage, port 0.2 | $I_{OL}$ – 3.2mA | | | V |
| $V_{OH}$ | Output high voltage, ports 1 and 3 | $I_{OH}$ – 60µA | 2.4 | | V |
| | | $I_{OH}$ – 25µA | $0.75V_{CC}$ | | V |
| | | $I_{OH}$ – 25µA | $0.9V_{CC}$ | | V |
| | Port 0.0 and 0.2 ($I^2C$) – Drivers | | | | |
| $V_{OL2}$ | Output low voltage | $I_{OL}$ – 3mA (over $V_{CC}$ range) | | 0.4 | V |
| | Driver, receiver combined: | | | | |
| C | Capacitance | | | 10 | pF |
| $I_{IL}$ | Logical 0 input current, ports 1 and 3 | $V_{IN}$ – 0.45V | | 75 | µA |
| $I_{TL}$ | Logical 1 to 0 transition current, ports 1 and 3 | $V_{IN}$ – 2V | | –750 | µA |
| $I_{LI}$ | Input leakage current, port 0 | $0.45 < V_{IN} < V_{CC}$ | | ±10 | µA |
| $R_{RST}$ | Reset pull-down resistor | | 25 | 175 | kΩ |
| $C_{IO}$[8] | Pin capacitance | Test freq – 1MHz, $T_A$ – 25°C | | 10 | pF |
| $I_{PD}$ | Power-down current[6] | $V_{CC}$ – 3 to 5.5V | | 50 | µA |
| $V_{PP}$ | $V_{PP}$ program voltage | $V_{SS}$ – 0V<br>$V_{CC}$ – 5V±10%<br>$T_A$ – 21°C–27°C | 12.5 | 13.0 | V |
| $I_{PP}$ | Program current | $V_{PP}$ – 13.0V | | 10 | mA |
| $I_{CC}$ | Supply current | freq – 12MHz | | 15 | mA |

**AC SYMBOL DESIGNATIONS**

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

C – Clock
D – Input data
H – Logic level high
L – Logic level low
Q – Output data
T – Time
V – Valid
X – No longer a valid logic level
Z – Float

## AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq 125°C$, $4.0 \leq V_{CC} \leq 6.0 V_{SS} = 0V$[3, 7]

| SYMBOL | PARAMETER | 12MHz | | VARIABLE CLOCK | | UNIT |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator frequency | | | 0.5 | 12 | MHz |
| | External clock (Figure 1) | | | | | |
| $t_{CHCH}$ | High time | 20 | | | | ns |
| $t_{CHCH}$ | Low time | 20 | | | | ns |
| $t_{CHCH}$ | Rise time | | 20 | | | ns |
| $t_{CHCH}$ | Fall time | | 20 | | | ns |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages with respect to $V^{SS}$ unless otherwise noted.
4. Power-down Icc is measured with all output pins disconnected; port 0 = $V_{CC}$; X2, X1 n.c.; RST = $V_{SS}$.
5. $I_{CC}$ is measured with all output pins disconnected; X1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; X2 n.c.; RST = port 0 = Vcc. Icc will be slightly higher if a crystal is used.
6. Idle $I_{CC}$ is measured with all output pins disconnected; X1 driven with $t_{CLCH}$, $t_{CHCL}$ = 5ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; X2 n.n; port 0 = $V_{CC}$; RST = $V_{SS}$.
7. Load capacitance for ports = 80pF.
8. $C_{IO}$ is tested initially and after each design or process changes which may effect capacitance.

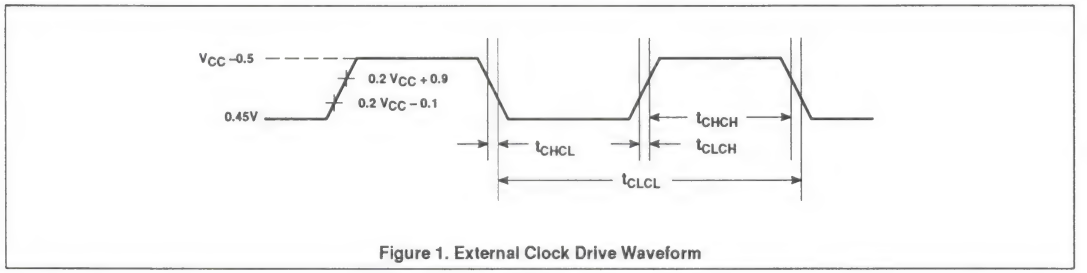



**Figure 1. External Clock Drive Waveform**

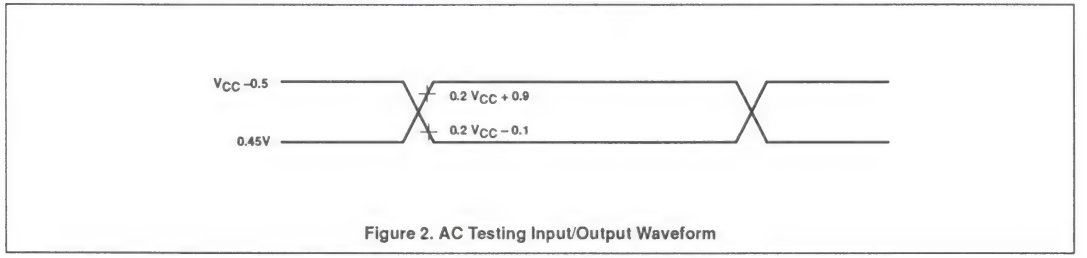



**Figure 2. AC Testing Input/Output Waveform**

## PROGRAMMING CONSIDERATIONS

### EPROM Characteristics

The 87C751 is programmed by using a modified Quick-Pulse Programming algorithm similar to that used for devices such as the 87C451 and 87C51. It differs from these devices in that a serial data stream is used to place the 87C751 in the programming mode.

Figure 3 shows a block diagram of the programming configuration for the 87C751. Port pin PO.2 is used as the programming voltage supply input ($V_{PP}$ signal). Port pin PO.1 is used as the program (PCM/) signal. This pin is used for the 25 programming pulses.

Port 3 is used as the address input for the byte to be programmed and accepts both the high and low components of the eleven bit address. During one portion of the programming cycle, Port 3 will accept the low component of the address (bits A0 - A7) and during another portion of the cycle, the high component of the address (bits A8 - A10). The timing of the high and low components is derived internal to the 87C751 and P0.0 is provided as an address select signal (ASEL) to indicate when the device is ready to accept which portion of the address. By using tri-statable drivers as shown in Figure 3, this multiplexing of the address components is transparent to the user. P0.0 is an open drain output and a pullup resistor is required. P0.0 is low for the lower byte of the address and high for the high order bits of the address.

Port 1 is used as a bidirectional data bus during programming mode, it accepts the byte to be programmed. During verify mode, it provides the contents of the EPROM location specified by the address which has been supplied to Port 3.

The XTAL1 pin is the ocsillator input and receives the master system clock. This clock should be between 4 and 6 MHz.

The RESET pin is used to accept the serial data stream that places the 87C751 into various programming modes. This pattern consists of a 10-bit code with the LSB sent first. Each bit is synchronized to the clock input, X1.

### Programming Operation

Figures 4 and 5 show the timing diagrams for the program/verify cycle. RESET should initially be held high for at least two machine cycles. P0.1 (PGM/) and P0.2 ($V_{PP}$) will be at $V_{OH}$ as a result of the RESET operation. At this point, these pins function as normal quasi-bidirectional I/O ports and the programming equipment may pull these lines low. However, prior to sending the 10 bit code on the reset pin, the programming equipment should drive these pins high ($V_{IH}$). The RESET pin may now be used as the serial data input for the data stream which places the 87C751 in the programming mode. Data bits are sampled during the clock high time and thus should only change during the time that the clock is low. Following transmission of the last data bit, the RESET pin should be held low.

Next the address information for the location programmed is placed at the inputs of the buffers used to perform the address multiplexing function. At this time Port 1 functions as an output.

A high voltage $V_{PP}$ level is then applied to the $V_{PP}$ input (P0.2). (This sets Port 1 as an input port.) The data to be programmed into the EPROM array is then placed on Port 1. This is followed by a series of programming pulses applied to the PGM/ pin (P0.1). These pulses are created by driving P0.1 low and then high. This pulse is repeated until a total of twenty-five programming pulses have occurred. At the conclusion of the last pulse, the PGM/ signal should remain high.

The $V_{PP}$ signal may now be driven to the $V_{OH}$ level, placing the 87C751 in the verify mode. (Port 1 is now used as an output port.) After 4 machine cycles (48 clock periods) the contents of the addressed location in the EPROM array will appear on Port 1.

The next programming cycle may now be initiated by placing the address information at the inputs of the multiplexed buffers, driving the $V_{PP}$ pin to the $V_{PP}$ voltage level, providing the byte to be programmed to Port 1 and issuing the 25 programming pulses on the PGM/ pin, bringing $V_{PP}$ back down to the $V_{CC}$ level and verifying the byte.

### Programming Modes

The 87C751 has four programming features incorporated within its EPROM array. These include the USER EPROM for storage of the application's code, a sixteen byte encryption KEY array and two security bits. Programming and verification of the these four elements are selected by a combination of the serial data stream applied to the RESET pin and the voltage levels applied to port pins P0.1 and P0.2. The various combinations are shown in Table 1.

### Encryption Key Table

The 87C751 includes a 16 byte EPROM array that is programmable by the end user. The contents of this array can then be used to encrypt the program memory contents during a program memory verify operation. When a program memory verify operation is performed, the contents of the program memory location is XNOR'ed with one of the bytes in the 16 byte encryption table. The resulting data pattern is then provided to port 1 as the verify data. The encryption mechanism can be disabled, in essence, by leaving the bytes in the encryption table in their erased state (FFH) since the XNOR product of a bit with a logical one will result in the original bit. The encryption bytes are mapped with the code memory in 16 byte groups. The first byte in code memory will be encrypted with the first byte in the encryption table; the second byte in code memory will be encrypted with the second byte in the encryption table and so forth up to and including the sixteenth byte. The encryption repeats in 16 byte groups; the seventeenth byte in code memory will be encrypted with the first byte in the encryption table, and so forth.

### Security Bits

Two security bits, security bit 1 and security bit 2, are provided to limit access to the USER EPROM and encryption key arrays, Security bit 1 is the program inhibit bit, and once programmed performs the following functions:

1. Additional programming of the USER EPROM is inhibited.
2. Additional programming of the encryption is inhibited.
3. Verification of the encryption key is inhibited.
4. Verification of the USER EPROM and the security bit levels may still be performed.

(If the encryption key array is being used, the security bit should be programmed by the user to prevent unauthorized parties from reprogramming the encryption key to all logical zero bits. Such programming would provide data during a verify cycle that is the logical compliment of he USER EPROM contents.)

Security bit 2, the verify inhibit bit, prevents verification of both the USER EPROM array and the encryption key arrays. The security bit levels may still be verified.

### Programming and Verifying Security Bits

Security bits are programmed employing the same techniques used to program the USER EPROM and KEY arrays using serial data streams and logic levels on port pins indicated in Table 3. When programming either security bit, it is not necessary to provide address or data information to the 87C751 on ports 1 and 3.

Verification occurs in a similar manner using the RESET serial stream shown in Table 1. Port 3 is not required to be driven and the results of the verify operation will appear on ports 1.6 and 1.7.

Port 1.7 contains the security bit 1 data and is a logical one if programmed and logical zero i erased. Likewise, P1.6 contains the security bit

2 data and is a logical one if programmed and a logical zero if erased.

## Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature of solvent environments, use Kapton tape Fluorglas part number 2345–5 or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose at least 15W–sec/cm$^2$. Exposing the EPROM to and ultraviolet lamp of 12,000^W/cm$^2$ rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

### Table 3. Implementing Program/Verify Modes

| Operation | Serial Code | P0.1 (PGM/) | P0.2 ($V_{PP}$) |
|---|---|---|---|
| Program user EPROM | 296H | ~* | $V_{PP}$ |
| Verify user EPROM | 296H | $V_{IH}$ | $V_{IH}$ |
| Program key EPROM | 292H | ~* | $V_{PP}$ |
| Verify key EPROM | 292H | $V_{IH}$ | $V_{IH}$ |
| Program security bit 1 | 29AH | ~* | $V_{PP}$ |
| Program security bit 2 | 298H | ~* | $V_{PP}$ |
| Verify security bits | 29AH | $V_{IH}$ | $V_{IH}$ |

**NOTE:**
Pulsed from $V_{IH}$ to $V_{IL}$ and returned to $V_{IH}$.

### EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS $T_A$ = 21°C to +27°C, $V_{CC}$ = 5V±10, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $1/t_{CLCL}$ | Oscillator/clock frequency | 4 | 6 | MHz |
| $t_{AVGL}$* | Address setup to P0.1 (PROG–) Low | 10µs + 24$t_{CLCL}$ | | |
| $t_{GHAX}$ | Address hold after P0.1 (PROG–) High | 48$t_{CLCL}$ | | |
| $t_{DVGL}$ | Data setup to P0.1 (PROG–) Low | 38$t_{CLCL}$ | | |
| $t_{GHDX}$ | Data hold after P0.1 (PROG–) High | 36$t_{CLCL}$ | | |
| $t_{SHGL}$ | $V_{PP}$ setup to P0.1 (PROG–) Low | 10 | | µs |
| $t_{GHSL}$ | $V_{PP}$ hold after P0.1 (PROG–) | 10 | | µs |
| $t_{GLGH}$ | P0.1 (PROG–) width | 90 | 110 | µs |
| $t_{AVQV}$** | $V_{PP}$ Low ($V_{CC}$) to data valid | | 48$t_{CLCL}$ | |
| $t_{GHGL}$ | P0.1 (PROG–) High to P0.1 (PROG–) Low | 10 | | µs |
| $t_{SYNL}$ | P0.0 (sync pulse) Low | 4$t_{CLCL}$ | | |
| $t_{SYNH}$ | P0.0 (sync pulse) High | 8$t_{CLCL}$ | | |

**NOTES:**
* Address should be valid at least 24 $t_{CLCL}$ before rising edge of P0.2 ($V_{PP}$).
** For a pure verify mode, i.e., no program mode in between, $t_{AVQV}$ is 14 $t_{CLCL}$ maximum.

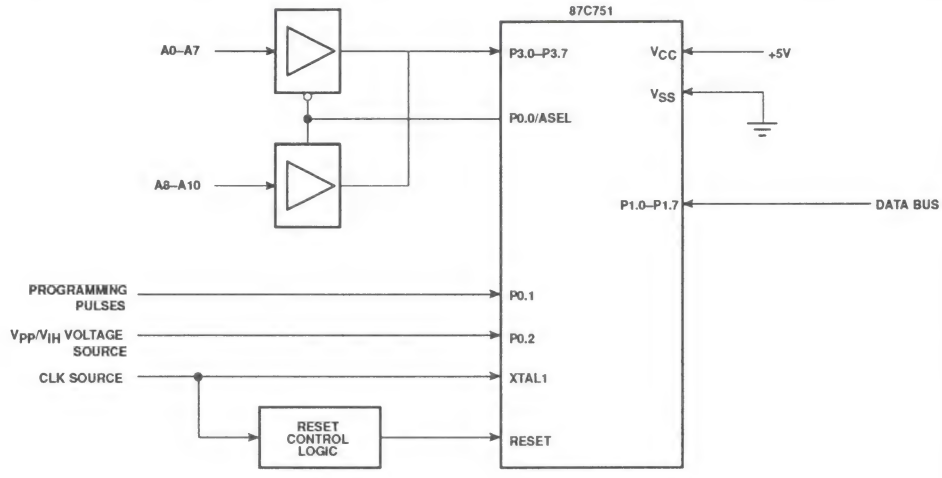



Figure 3. Programming Configuration

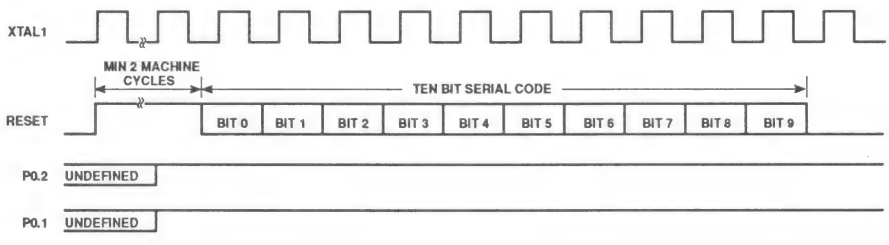
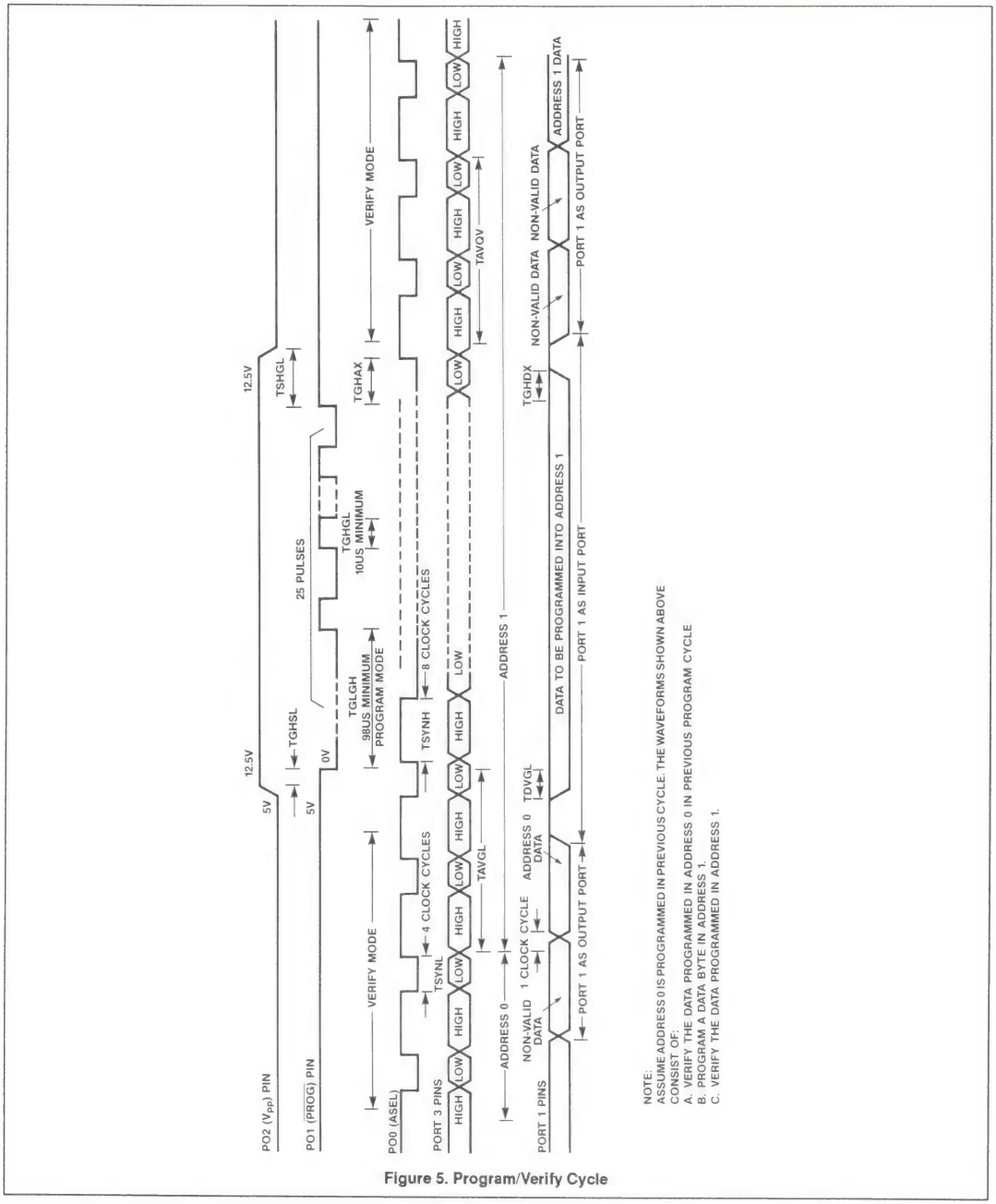



Figure 4. Entry Into Program/Verify Modes




NOTE:
ASSUME ADDRESS 0 IS PROGRAMMED IN PREVIOUS CYCLE. THE WAVEFORMS SHOWN ABOVE CONSIST OF:
A. VERIFY THE DATA PROGRAMMED IN ADDRESS 0 IN PREVIOUS PROGRAM CYCLE
B. PROGRAM A DATA BYTE IN ADDRESS 1.
C. VERIFY THE DATA PROGRAMMED IN ADDRESS 1.

**Figure 5. Program/Verify Cycle**

## INSTRUCTION SET

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Arithmetic Operations** | | | | |
| ADD | A,Rn | Add register to accumulator | 1 | 1 |
| ADD | A,direct | Add direct byte to accumulator | 2 | 1 |
| ADD | A,@Ri | Add indirect RAM to accumulator | 1 | 1 |
| ADD | A,#data | Add immediate data to accumulator | 2 | 1 |
| ADDC | A,Rn | Add register to accumulator with carry | 1 | 1 |
| ADDC | A,direct | Add direct byte to A with carry flag | 2 | 1 |
| ADDC | A,@Ri | Add indirect RAM to A with carry flag | 1 | 1 |
| ADDC | A,#data | Add immediate data to A with carry flag | 2 | 1 |
| SUBB | A,Rn | Subtract register from A with borrow | 1 | 1 |
| SUBB | A,direct | Subtract direct byte from A with borrow | 2 | 1 |
| SUBB | A,@Ri | Subtract indirect RAM from A w/borrow | 1 | 1 |
| SUBB | A,#data | Subtract immediate data from A w/borrow | 2 | 1 |
| INC | A | Increment accumulator | 1 | 1 |
| INC | Rn | Increment register | 1 | 1 |
| INC | direct | Increment direct byte | 2 | 1 |
| INC | @Ri | Increment indirect RAM | 1 | 1 |
| DEC | A | Decrement accumulator | 1 | 1 |
| DEC | Rn | Decrement register | 1 | 1 |
| DEC | direct | Decrement direct byte | 2 | 1 |
| DEC | @Ri | Decrement indirect RAM | 1 | 1 |
| INC | DPTR | Increment data pointer | 1 | 2 |
| MUL | AB | Multiply A & B | 1 | 4 |
| DIV | AB | Divide A by B | 1 | 4 |
| DA | A | Decimal adjust accumulator | 1 | 1 |
| **Logical Operations** | | | | |
| ANL | A,Rn | AND register to accumulator | 1 | 1 |
| ANL | A,direct | AND direct byte to accumulator | 2 | 1 |
| ANL | A,@Ri | AND indirect RAM to accumulator | 1 | 1 |
| ANL | A,#data | AND immediate data to accumulator | 2 | 1 |
| ANL | direct,A | AND accumulator to direct byte | 2 | 1 |
| ANL | direct,#data | AND immediate data to direct byte | 3 | 2 |
| ORL | A, Rn | OR register to accumulator | 1 | 1 |
| ORL | A,direct | OR direct byte to accumulator | 2 | 1 |
| ORl | A,@Ri | OR indirect RAM to accumulator | 1 | 1 |
| ORl | A,#data | OR immediate data to accumulator | 2 | 1 |
| ORL | direct,A | OR accumulator to direct byte | 2 | 1 |
| ORL | direct,#data | OR immediate data to direct byte | 3 | 2 |
| XRL | A,Rn | Exclusive–OR register to accumulator | 1 | 1 |
| XRL | A,direct | Exclusive–OR direct byte to accumulator | 2 | 1 |
| XRL | A,@Ri | Exclusive–OR indirect RAM to A | 1 | 1 |
| XRL | A,#data | Exclusive–OR immediate data to A | 2 | 1 |
| XRL | direct,A | Exclusive–OR accumulator to direct byte | 2 | 1 |
| XRL | direct,#data | Exclusive–OR immediate data to direct byte | 3 | 2 |
| CLR | A | Clear accumulator | 1 | 1 |
| CPL | A | Complement accumulator | 1 | 1 |
| RL | A | Rotate accumulator left | 1 | 1 |
| RLC | A | Rotate A left through the carry flag | 1 | 1 |
| RR | A | Rotate accumulator right | 1 | 1 |
| RRC | A | Rotate A right through carry flag | 1 | 1 |
| SWAP | A | Swap nibbles within the accumulator | 1 | 1 |
| **Data Transfer** | | | | |
| MOV | A,Rn | Move register to accumulator | 1 | 1 |
| MOV | A,direct | Move direct byte to accumulator | 2 | 1 |
| MOV | A,@Ri | Move indirect RAM to accumulator | 1 | 1 |
| MOV | A,#data | Move immediate data to accumulator | 2 | 1 |

## INSTRUCTION SET (Continued)

| MNEMONIC | | DESCRIPTION | BYTE | CYCLES |
|---|---|---|---|---|
| **Data Transfer (cont)** | | | | |
| MOV | Rn,A | Move accumulator to register | 1 | 1 |
| MOV | Rn,direct | Move direct byte to register | 2 | 2 |
| MOV | Rn,#data | Move immediate data to register | 2 | 1 |
| MOV | direct,A | Move accumulator to direct byte | 2 | 1 |
| MOV | direct,Rn | Move register to direct byte | 2 | 2 |
| MOV | direct,direct | Move direct byte to direct byte | 3 | 2 |
| MOV | direct,@Ri | Move indirect RAM to direct byte | 2 | 2 |
| MOV | direct,#data | Move immediate data to direct byte | 3 | 2 |
| MOV | @Ri,A | Move accumulator to indirect RAM | 1 | 1 |
| MOV | @Ri,direct | Move direct byte to indirect RAM | 2 | 2 |
| MOV | @Ri,#data | Move immediate data to indirect RAM | 2 | 1 |
| MOV | DPTR,#data16 | Load data pointer with a 16–bit constant | 3 | 2 |
| MOVC | A,@A + DPTR | Move code byte relative to DPTR to A | 1 | 2 |
| MOVC | A,@A + PC | Move code byte relative to PC to A | 1 | 2 |
| PUSH | direct | Push direct byte onto stack | 2 | 2 |
| POP | direct | Pop direct byte from stack | 2 | 2 |
| SCH | A,Rn | Exchange register with accumulator | 1 | 1 |
| XCH | A,direct | Exchange direct byte with accumulator | 2 | 1 |
| XCH | A,@Ri | Exchange indirect RAM with A | 1 | 1 |
| XCHD | A,@Ri | Exchange low–order digit indirect RAM with A | 1 | 1 |
| **Boolean variable manipulation** | | | | |
| CLR | C | Clear carry flag | 1 | 1 |
| CLR | bit | Clear direct bit | 2 | 1 |
| SETB | C | Set carry flag | 1 | 1 |
| SETB | bit | Set direct bit | 2 | 1 |
| CPL | C | Complement carry flag | 1 | 1 |
| CPL | bit | Complement direct bit | 2 | 1 |
| ANL | C,bit | AND direct bit to carry flag | 2 | 2 |
| ANL | C,/bit | AND complement of direct bit to carry | 2 | 2 |
| ORL | C,bit | OR direct bit to carry flag | 2 | 2 |
| ORL | C,/bit | OR complement of direct bit to carry | 2 | 2 |
| MOV | C,bit | Move direct bit to carry flag | 2 | 1 |
| MOV | bit,C | Move carry flag to direct bit | 2 | 2 |
| **Program and machine control** | | | | |
| ACALL | addr11 | Absolute subroutine call | 2 | 2 |
| RET | | Return from subroutine | 1 | 2 |
| RETI | | Return from interrupt | 1 | 2 |
| AJMP | addr11 | Absolute jump | 2 | 2 |
| LJMP* | addr16 | Long jump | 3 | 2 |
| SJMP | rel | Short jump (relative addr) | 2 | 2 |
| JMP | @A + DPTR | Jump indirect relative to the DPTR | 1 | 2 |
| JZ | rel | Jump if accumulator is zero | 2 | 2 |
| JNZ | rel | Jump if accumulator is not zero | 2 | 2 |
| JC | rel | Jump if carry flag is set | 2 | 2 |
| JNC | rel | Jump if carry flag not set | 2 | 2 |
| JB | bit,rel | Jump if direct bit set | 3 | 2 |
| JNB | bit,rel | Jump if direct bit not set | 3 | 2 |
| JBC | bit,rel | Jump if direct bit is set and clear bit | 3 | 2 |
| CJNE | A,direct,rel | Compare direct to A and jump if not equal | 3 | 2 |
| CJNE | A,#data,rel | Compare immediate to A and jump if not equal | 3 | 2 |
| CJNE | Rn,#data,rel | Compare immediate to register and jump if not equal | 3 | 2 |
| CJNE | @Ri,#data,rel | Compare immediate to indirect and jump if not equal | 3 | 2 |
| DJNZ | Rn,rel | Decrement register and jump if not zero | 2 | 2 |
| DJNZ | direct,rel | Decrement direct and jump if not zero | 3 | 2 |
| NOP | | No operation | 1 | 1 |

**Notes on following page.**

**Notes on data addressing modes:**

| | |
|---|---|
| Rn | Working register R0–R7. |
| direct | 64 internal RAM locations, any I/O port, control or status register. |
| @Ri | indirect internal RAM location addressed by register R0 or R1. |
| #data | 8-bit constant included in instruction. |
| #data16 | 16-bit constant included as bytes 2 and 3 of instruction. |
| bit | 128 software flags, any I/O pin, control or status bit. |

**Notes on program addressing modes:**

| | |
|---|---|
| addr16 | Destination address for LJMP. Only 11 bits of this 16-bit field are used. |
| addr11 | Destination address for ACALL and AJMP will be within the same 2Kbyte page of program memory as the first byte of the following instruction. |
| rel | SJMP and all conditional jumps include an 8-bit offset byte. Range is +127 – 128 bytes relative to first byte of the following instruction. |

## INSTRUCTION OPCODES IN HEXADECIMAL ORDER

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 00 | 1 | NOP | |
| 01 | 2 | AJMP | code addr |
| 02 | 3 | LJMP* | |
| 03 | 1 | RR | A |
| 04 | 1 | INC | A |
| 05 | 2 | INC | data addr |
| 06 | 1 | INC | @R0 |
| 07 | 1 | INC | @R1 |
| 08 | 1 | INC | R0 |
| 09 | 1 | INC | R1 |
| 0A | 1 | INC | R2 |
| 0B | 1 | INC | R3 |
| 0C | 1 | INC | R4 |
| 0D | 1 | INC | R5 |
| 0E | 1 | INC | R6 |
| 0F | 1 | INC | R7 |
| 10 | 3 | JBC | bit addr,code addr |
| 11 | 2 | ACALL | code addr |
| 12 | 3 | LCALL* | |
| 13 | 1 | RRC | A |
| 14 | 1 | DEC | A |
| 15 | 2 | DEC | data addr |
| 16 | 1 | DEC | @R0 |
| 17 | 1 | DEC | @R1 |
| 18 | 1 | DEC | R0 |
| 19 | 1 | DEC | R1 |
| 1A | 1 | DEC | R2 |
| 1B | 1 | DEC | R3 |
| 1C | 1 | DEC | R4 |
| 1D | 1 | DEC | R5 |
| 1E | 1 | DEC | R6 |
| 1F | 1 | DEC | R7 |
| 20 | 3 | JB | bit addr,code addr |
| 21 | 2 | AJMP | code addr |
| 22 | 1 | RET | |
| 23 | 1 | RL | A |
| 24 | 2 | ADD | A,#data |
| 25 | 2 | ADD | A,data addr |
| 26 | 1 | ADD | A,@R0 |
| 27 | 1 | ADD | A,@R1 |
| 28 | 1 | ADD | A,R0 |
| 29 | 1 | ADD | A,R1 |
| 2A | 1 | ADD | A,R2 |
| 2B | 1 | ADD | A,R3 |
| 2C | 1 | ADD | A,R4 |
| 2D | 1 | ADD | A,R5 |
| 2E | 1 | ADD | A,R6 |
| 2F | 1 | ADD | A,R7 |
| 30 | 3 | JNB | bit addr,code addr |
| 31 | 2 | ACALL | code addr |
| 32 | 1 | RETI | |
| 33 | 1 | RLC | A |
| 34 | 2 | ADDC | A,#data |
| 35 | 2 | ADDC | A,data addr |
| 36 | 1 | ADDC | A,@R0 |
| 37 | 1 | ADDC | A,@R1 |
| 38 | 1 | ADDC | A,R0 |
| 39 | 1 | ADDC | A,R1 |
| 3A | 1 | ADDC | A,R2 |
| 3B | 1 | ADDC | A,R3 |
| 3C | 1 | ADDC | A,R4 |
| 3D | 1 | ADDC | A,R5 |
| 3E | 1 | ADDC | A,R6 |
| 3F | 1 | ADDC | A,R7 |
| 40 | 2 | JC | code addr |
| 41 | 2 | AJMP | code addr |
| 42 | 2 | ORL | data addr,A |
| 43 | 3 | ORL | data addr,#data |
| 44 | 2 | ORL | A,#data |
| 45 | 2 | ORL | A,data addr |
| 46 | 1 | ORL | A,@R0 |
| 47 | 1 | ORL | A,@R1 |
| 48 | 1 | ORL | A,R0 |
| 49 | 1 | ORL | A,R1 |
| 4A | 1 | ORL | A,R2 |
| 4B | 1 | ORL | A,R3 |
| 4C | 1 | ORL | A,R4 |
| 4D | 1 | ORL | A,R5 |
| 4E | 1 | ORL | A,R6 |
| 4F | 1 | ORL | A,R7 |
| 50 | 2 | JNC | code addr |
| 51 | 2 | ACALL | code addr |
| 52 | 2 | ANL | data addr,A |
| 53 | 3 | ANL | data addr,#data |
| 54 | 2 | ANL | A,#data |
| 55 | 2 | ANL | A,data addr |
| 56 | 1 | ANL | A,@R0 |
| 57 | 1 | ANL | a,@r1 |
| 58 | 1 | ANL | A,R0 |
| 59 | 1 | ANL | A,R1 |
| 5A | 1 | ANL | A,R2 |
| 5B | 1 | ANL | A,R3 |
| 5C | 1 | ANL | A,R4 |
| 5D | 1 | ANL | A,R5 |
| 5E | 1 | ANL | A,R6 |
| 5F | 1 | ANL | A,R7 |
| 60 | 2 | JZ | code addr |
| 61 | 2 | AJMP | code addr |
| 62 | 2 | XRL | data addr,A |
| 63 | 3 | XRL | data addr,#data |
| 64 | 2 | XRL | A,#data |
| 65 | 2 | XRL | A,data addr |
| 66 | 1 | XRL | A,@R0 |
| 67 | 1 | XRL | A,@R1 |
| 68 | 1 | XRL | A,R0 |
| 69 | 1 | XRL | A,R1 |
| 6A | 1 | XRL | A,R2 |
| 6B | 1 | XRL | A,R3 |
| 6C | 1 | XRL | A,R4 |
| 6D | 1 | XRL | A,R5 |
| 6E | 1 | XRL | A,R6 |
| 6F | 1 | XRL | A,R7 |
| 70 | 2 | JNZ | code addr |
| 71 | 2 | ACALL | code addr |

## INSTRUCTION OPCODES IN HEXADECIMAL ORDER (Cont.)

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| 72 | 2 | ORL | C,bit addr |
| 73 | 1 | JMP | @A + DPTR |
| 74 | 2 | MOV | A,#data |
| 75 | 3 | MOV | data addr,#data |
| 76 | 2 | MOV | @R0,#data |
| 77 | 2 | MOV | @R1,#data |
| 78 | 2 | MOV | R0,#data |
| 79 | 2 | MOV | R1,#data |
| 7A | 2 | MOV | R2,#data |
| 7B | 2 | MOV | R3,#data |
| 7C | 2 | MOV | R4,#data |
| 7D | 2 | MOV | R5,#data |
| 7E | 2 | MOV | R6,#data |
| 7F | 2 | MOV | R7,#data |
| 80 | 2 | SJMP | code addr |
| 81 | 2 | AJMP | code addr |
| 82 | 2 | ANL | C,bit addr |
| 83 | 1 | MOVC | A,@A + PC |
| 84 | 1 | DIV | AB |
| 85 | 3 | MOV | data addr,data addr |
| 86 | 2 | MOV | data addr,@R0 |
| 87 | 2 | MOV | data addr,@R1 |
| 88 | 2 | MOV | data addr,R0 |
| 89 | 2 | MOV | data addr,R1 |
| 8A | 2 | MOV | data addr,R2 |
| 8B | 2 | MOV | data addr,R3 |
| 8C | 2 | MOV | data addr,R4 |
| 8D | 2 | MOV | data addr,R5 |
| 8E | 2 | MOV | data addr,R6 |
| 8F | 2 | MOV | data addr,R7 |
| 90 | 3 | MOV | DPTR,#data |
| 91 | 2 | ACALL | code addr |
| 92 | 2 | MOV | bit addr,C |
| 93 | 1 | MOVC | A,@A + DPTR |
| 94 | 2 | SUBB | A,#data |
| 95 | 2 | SUBB | A,data addr |
| 96 | 1 | SUBB | A,@R0 |
| 97 | 1 | SUBB | A,@R1 |
| 98 | 1 | SUBB | A,R0 |
| 99 | 1 | SUBB | A,R1 |
| 9A | 1 | SUBB | A,R2 |
| 9B | 1 | SUBB | A,R3 |
| 9C | 1 | SUBB | A,R4 |
| 9D | 1 | SUBB | A,R5 |
| 9E | 1 | SUBB | A,R6 |
| 9F | 1 | SUBB | A,R7 |
| A0 | 2 | ORL | C,/bit addr |
| A1 | 2 | AJMP | code addr |
| A2 | 2 | MOV | C,bit addr |
| A3 | 1 | INC | DPTR |
| A4 | 1 | MUL | AB |
| A5 | | reserved | |
| A6 | 2 | MOV | @R0,data addr |
| A7 | 2 | MOV | @R1,data addr |
| A8 | 2 | MOV | R0,data addr |
| A9 | 2 | MOV | R1,data addr |
| AA | 2 | MOV | R2,data addr |
| AB | 2 | MOV | R3,data addr |
| AC | 2 | MOV | R4,data addr |
| AD | 2 | MOV | R5,data addr |
| AE | 2 | MOV | R6,data addr |
| AF | 2 | MOV | R7,data addr |
| B0 | 2 | ANL | C,/bit addr |
| B1 | 2 | ACALL | code addr |
| B2 | 2 | CPL | bit addr |
| B3 | 1 | CPL | C |
| B4 | 3 | CJNE | A,#data,code addr |
| B5 | 3 | CJNE | A,data addr,code addr |
| B6 | 3 | CJNE | @R0,#data,code addr |
| B7 | 3 | CJNE | @R1,#data,code addr |
| B8 | 3 | CJNE | R0,#data,code addr |
| B9 | 3 | CJNE | R1,#data,code addr |
| BA | 3 | CJNE | R2,#data,code addr |
| BB | 3 | CJNE | R3,#data,code addr |
| BC | 3 | CJNE | R4,#data,code addr |
| BD | 3 | CJNE | R5,#data,code addr |
| BE | 3 | CJNE | R6,#data,code addr |
| BF | 3 | CJNE | R7,#data,code addr |
| C0 | 2 | PUSH | data addr |
| C1 | 2 | AJMP | code addr |
| C2 | 2 | CLR | bit addr |
| C3 | 1 | CLR | C |
| C4 | 1 | SWAP | A |
| C5 | 2 | XCH | A,data addr |
| C6 | 1 | XCH | A,@R0 |
| C7 | 1 | XCH | A@R1 |
| C8 | 1 | XCH | A,R0 |
| C9 | 1 | XCH | A,R1 |
| CA | 1 | XCH | A,R2 |
| CB | 1 | XCH | A,R3 |
| CC | 1 | XCH | A,R4 |
| CD | 1 | XCH | A,R5 |
| CE | 1 | XCH | A,R6 |
| CF | 1 | XCH | A,R7 |
| D0 | 2 | POP | data addr |
| D1 | 2 | ACALL | code addr |
| D2 | 2 | SETB | bit addr |
| D3 | 1 | SETB | C |
| D4 | 1 | DA | A |
| D5 | 3 | DJNZ | data addr,code addr |
| D6 | 1 | XCHD | A,@R0 |
| D7 | 1 | XCHD | A,@R1 |
| D8 | 2 | DJNZ | R0,code addr |
| D9 | 2 | DJNZ | R1,code addr |
| DA | 2 | DJNZ | R2,code addr |
| DB | 2 | DJNZ | R3,code addr |
| DC | 2 | DJNZ | R4,code addr |
| DD | 2 | DJNZ | R5,code addr |
| DE | 2 | DJNZ | R6,code addr |
| DF | 2 | DJNZ | R7,code addr |
| E0 | 1 | MOVX* | |
| E1 | 2 | AJMP | code addr |
| E2 | 1 | MOVX* | |
| E3 | 1 | MOVX* | |
| E4 | 1 | CLR | A |
| E5 | 2 | MOV | A,data addr |

## INSTRUCTION OPCODES IN HEXADECIMAL ORDER (Cont.)

| HEX CODE | NUMBER OF BYTES | MNEMONIC | OPERANDS |
|---|---|---|---|
| E6 | 1 | MOV | A,@R0 |
| E7 | 1 | MOV | A,@R1 |
| E8 | 1 | MOV | A,R0 |
| E9 | 1 | MOV | A,R1 |
| EA | 1 | MOV | A,R2 |
| EB | 1 | MOV | A,R3 |
| EC | 1 | MOV | A,R4 |
| ED | 1 | MOV | A,R5 |
| EE | 1 | MOV | A,R6 |
| EF | 1 | MOV | A,R7 |
| F0 | 1 | MOVX* | |
| F1 | 2 | ACALL | code addr |
| F2 | 1 | MOVX* | |
| F4 | 1 | CPL | A |
| F5 | 2 | MOV | data addr,A |
| F6 | 1 | MOV | @R0,A |
| F7 | 1 | MOV | @R1,A |
| F3 | 1 | MOVX* | |
| F8 | 1 | MOV | R0,A |
| F9 | 1 | MOV | R1,A |
| FA | 1 | MOV | R2,A |
| FB | 1 | MOV | R3,A |
| FC | 1 | MOV | R4,A |
| FD | 1 | MOV | R5,A |
| FE | 1 | MOV | R6,A |
| FF | 1 | MOV | R7,A |

**NOTE:**

* Missing 80C51 instructions are not applicable to the 87C751. Should these instructions be executed, the appropriate number of ROM bytes will be fetched, but no operation will take place. The use of these codes is not recommended.

The addr16 field is allowed for compatibility with existing software tools, however only the least significant 11 bits of the address field will be used.

Signetics

# 87C752

## CMOS Single-Chip 8-Bit Microcontroller

*Objective Specification*

**Military**
**Customer Specific Products**

### DESCRIPTION

The Signetics 87C752 offers many of the advantages of the 80C51 architecture in a small package and at low cost.

The 87C752 Microcontroller is fabricated with Signetics high-density CMOS technology. Signetics epitaxial substrate minimizes CMOS latch-up sensitivity.

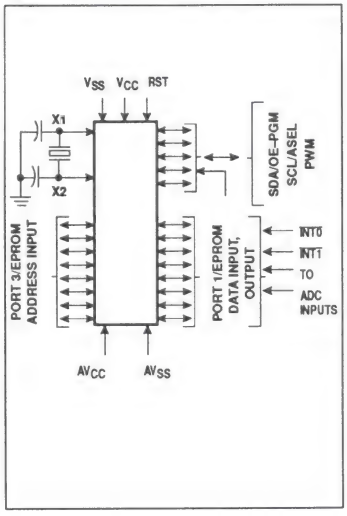
The 87C752 contains a 2K × 8 EPROM, a 64 × 8 RAM, 21 I/O lines, a 16-bit auto-reload counter/timer, a fixed-rate timer, a seven-source fixed-priority interrupt structure, a bidirectional Inter-Integrated Circuit ($I^2C$) serial bus interface, an on-chip oscillator, a five channel multiplexed 8-bit A/D converter, and an 8-bit PWM output.

The onboard inter-integrated circuit ($I^2C$) bus interface allows the 87C752 to operate as a master or slave device on the $I^2C$ small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated $I^2C$ peripherals.

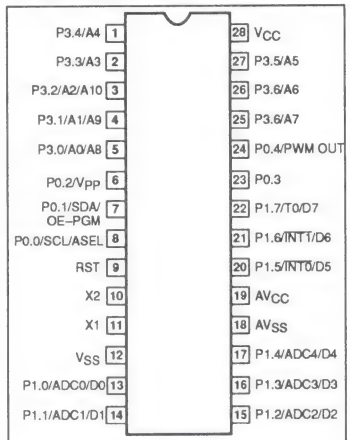
### FEATURES

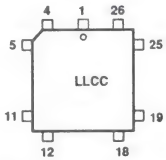
- **EPROM version of 83C752**
- **Available in erasable quartz lid or One-Time Programmable packages**
- **80C51 based architecture**
- **Inter-Integrated Circuit ($I^2C$) serial bus interface**
- **Small package sizes**
  - **28-pin DIP**
  - **28-pin LLCC**
- **Wide oscillator frequency range**
- **Low power consumption:**
  - **Normal operation: less than 11mA @ 5V, 12MHz**
  - **Idle mode**
  - **Power-down mode**
- **2K × 8 EPROM, 64 × 8 RAM**
- **16-bit auto reloadable counter/timer**
- **5 channel 8-bit A/D converter**
- **8-bit PWM output/timer**
- **Fixed-rate timer**
- **Boolean processor**
- **CMOS and TTL compatible**
- **Well suited for logic replacement applications**

### LOGIC SYMBOL




### PIN CONFIGURATION




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | P3.4/A4 | 15 | P1.2/ADC2/D2 |
| 2 | P3.3/A3 | 16 | P1.3/ADC3/D3 |
| 3 | P3.2/A2/A10 | 17 | P1.4/ADC4/D4 |
| 4 | P3.1/A1/A9 | 18 | $AV_{SS}$ |
| 5 | P3.0/A0/A8 | 19 | $AV_{CC}$ |
| 6 | $P0.2/V_{PP}$ | 20 | P1.5/INT0/D5 |
| 7 | P0.1/SDA/OE–PGM | 21 | P1.6/INT1/D6 |
| 8 | P0.0/SCL/ASEL | 22 | P1.7/T0/D7 |
| 9 | RST | 23 | P0.3 |
| 10 | X2 | 24 | P0.4/PWM OUT |
| 11 | X1 | 25 | P3.7/A7 |
| 12 | $V_{SS}$ | 26 | P3.6/A6 |
| 13 | P1.0/ADC0/D0 | 27 | P3.5/A5 |
| 14 | P1.1/ADC1/D1 | 28 | $V_{CC}$ |

NOTE:
A0–A10 and D0–D7 available for EPROM verify only.

Signetics

# 8X60
## FIFO RAM Controller (FRC)

***Product Specification***

**Military**
**Customer Specific Products**

### FEATURES

- **12-Bit FIFO address generator**
- **Data rate exceeding 8MHz**
- **Asynchronous Read/Write operations**
- **3-State address outputs**
- **User-defined word width**
- **Specifically designed for use with high-speed bipolar RAMs (adaptable for use with MOS RAMs)**
- **TTL input and output**
- **16mA Address-drive capability**

### USE AND APPLICATION

- **Interface between independently-clocked systems**
- **Buffer memories for disk and/or tape**
- **Data communication concentrators**
- **CPU/terminal buffering**
- **DMA applications**
- **CRT terminals**

### FUNCTIONAL OPERATION

The FRC operates in either of two basic modes — **write** into the FIFO buffer memory or **read** from the FIFO buffer memory. These two operations are described in subsequent paragraphs and the complete sequence is summarized in Table 1. Typical Write/Read timing relationships, arbitration logic, and chip-enable control are shown in the Timing Diagrams.

### PRODUCT DESCRIPTION

The Signetics 8X60 FIFO RAM Controller (FRC) is an address and status generator designed to implement a high-speed/high-capacity First-In/First-Out (FIFO) stack utilizing standard off-the-shelf RAMs — see **Applications** on the last page of this data sheet. The FRC can control up to 4096 words of buffer memory; intermediate buffer sizes can be selected — refer to the memory length table on the next page. Built-in arbitration logic handles read/write operations on a first-come/first-serve basis.

As shown in Figure 1, the FRC consists of:

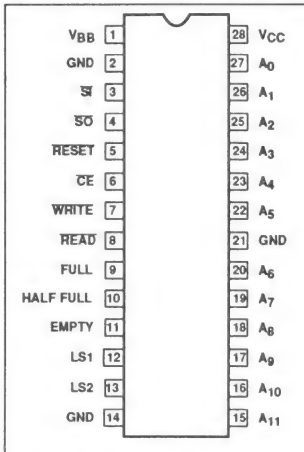
- A 12-bit write address generation counter (counter #1) and a 12-bit read address generation counter (counter #2).
- A 12-bit up/down status counter (counter #3).
- Twelve 3-State address drivers.
- Control logic.

The two address counters, #1 and #2, respectively, are used to generate write and read addresses; the outputs of these counters are multiplexed to the 3-State address drivers. Counter #3 generates **full, empty**, and **half full** status.

### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 28–Pin DIP 600mil–wide | 8X60/BXA |
| 28–Pin LLCC | 8X60/B3A |

### PIN CONFIGURATION




| PIN NO. | IDENTIFIER | FUNCTION |
|---|---|---|
| 1 | $V_{BB}$ | Supply voltage for internal circuits. |
| 2, 14, 21 | GND | Circuit ground. |
| 3 | $\overline{SI}$ | Shift-In request for write cycle; active-low input. |
| 4 | $\overline{SO}$ | Shift-Out request for read cycle; active-low input. |
| 5 | RESET | Active-low master reset input. |
| 6 | $\overline{CE}$ | Active-low chip enable input. |
| 7 | WRITE | Write cycle address valid; active-low output. |
| 8 | READ | Read cycle address valid; active-low output. |
| 9 | FULL | Memory full status output; also, override input capability. Active when high. |
| 10 | HALF FULL | Memory half-full status output; active-high. |
| 11 | EMPTY | Memory empty status output; also, override input capability. Active when high. |
| 12 | LS1 | Least significant bit (LSB) of the memory length select input. |
| 13 | LS2 | Most significant bit (MSB) of the memory length select input. |
| 15–20 22–27 | $A_{11}$–$A_0$ | 3-State address outputs; $A_0$ = LSB. |
| 28 | $V_{CC}$ | Supply voltage. |

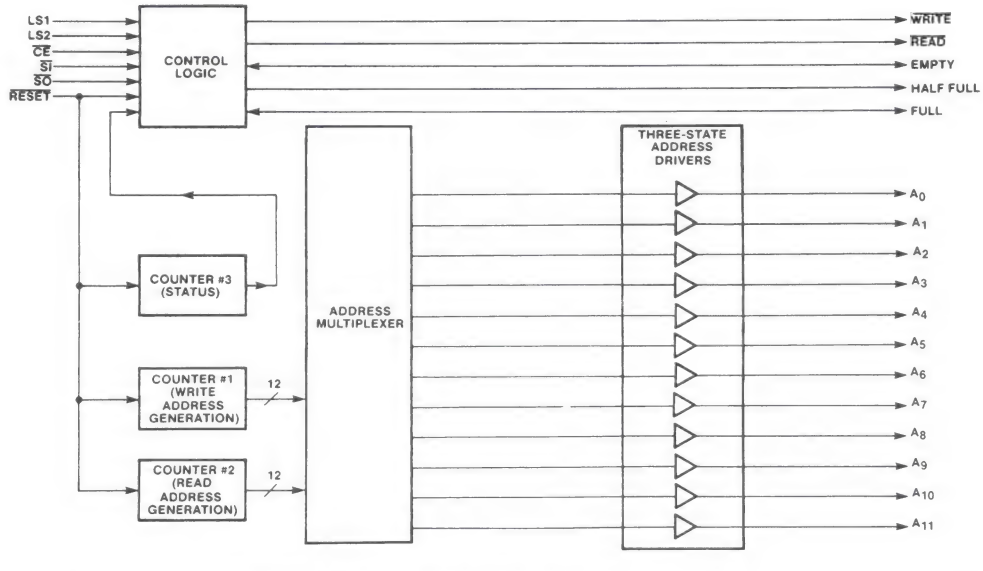



**Figure 1. Functional Block Diagram of FIFO RAM Controller**

## FIFO BUFFER MEMORY — WRITE CYCLE

To perform a write operation, $\overline{SO}$ must be High and SI must be Low. When these conditions exist and other control parameters (Table 1) are satisfied, the write address in Counter #1 (Figure 1) is output to the address bus via the multiplexer and $\overline{WRITE}$ output goes Low. (**Note**. Normally, the $\overline{WRITE}$ output goes Low after the address output becomes state — refer to **WRITE Cycle Timing Diagram**. The $\overline{WRITE}$ output may then act as a **write** or **chip** enable for the RAMs that are used to implement the memory.

When the **write** cycle is ended ($\overline{SI}$ is forced High), the $\overline{WRITE}$ output goes High, the address output buffers return to a High- impedance state. Counter #1 (Write Address Generation) and Counter #3 (Status) are both incremented, and Counter #2 (Read Address Generation) remains unchanged.

## FIFO BUFFER MEMORY — READ CYCLE

To perform a read operation, $\overline{SI}$ must be High and $\overline{SO}$ must be Low. When these conditions exist and other control parameters (Table 1) are satisfied, the read address contained in Counter #2 (Figure 1) is output to the address bus and the $\overline{READ}$ output goes Low. When the **read** cycle is ended ($\overline{SO}$ is forced High) the $\overline{READ}$ output goes High, the output buffers return to a High-impedance state. Counter #2 (Read Address Generation) is incremented. Counter #3 (Status) is decremented, and Counter #1 (Write Address Generation) remains unchanged.

## MEMORY LENGTH

| LS1 | LS2 | HALF LENGTH | FULL LENGTH |
|---|---|---|---|
| L | L | 2048 | 4096 |
| H | L | 32 | 64 |
| L | H | 512 | 1024 |
| H | H | 128 | 256 |

## CONTROL LOGIC

To prevent the possibility of operational conflicts, $\overline{SI}$ and $\overline{SO}$ are treated on a first-come/ first-served basis; these two input signals are controlled by internal arbitration logic — refer to the applicable **Timing Diagrams** and **AC Characteristics** for functional and timing relationships. If one cycle is requested while the other cycle is in progress, the requested cycle will commence as soon as the current-cycle is complete (provided other control parameters are satisfied).

As shown in the accompanying diagram, the buffer length of the FIFO memory can be hardware-selected via the Length Select (LS1, LS2) Inputs. When less than the maximum length is selected, the unused High-order bits of the address outputs are held in the High-impedance state.

Generation of the status output signals (HALF FULL, FULL and EMPTY) is a function of the Length Select (LS1, LS2) inputs and the current state of Status Counter #3. In general, the status outputs reflect the conditions that follow:

- **HALF FULL** — this status output signals goes High on the positive-going edge of $\overline{SI}$ if the MSB of the selected length of Counter #3 becomes a "1". The HALF FULL signal will go from High-to-Low on the positive-going edge of $\overline{SO}$ when, after the **read** cycle, the selected length of Counter #3 changes from "100 ... 00" to "011 ... 11". For example, if the selected memory length is 256 words (FULL = 256), then HALF FULL = 128 words; hence, on the positive-going edge of $\overline{SO}$ when Counter #3 reaches a count of 127, the HALF FULL output will go from High-to-Low.
- **FULL** — this signal serves both as a status output and as an override input. The FULL signal goes High on the negative-going edge of $\overline{SI}$ if all bits of Counter #3 for se-

lected length are equal to "1". The FULL output goes from High-to-Low on the negative-going edge of $\overline{SO}$.

- **EMPTY** — this signal also serves as a status output and as an override input. On the negative-going edge of $\overline{SO}$, the EMPTY output is driven High if Status Counter #3 contains a value of "1"; on the positive-going edge of $\overline{SO}$, the counter is decremented to "0". The EMPTY output goes from High-to-Low on the negative-going edge of $\overline{SI}$.

Once the FULL signal is High, further Write Cycle Requests ($\overline{SI}$ = low) are ignored; similarly, once the EMPTY signal is High, further Read Cycle requests ($\overline{SO}$ = low) are ignored. However, to accommodate diversified applications, the FULL and EMPTY outputs are open-collector with on-chip 4.7K passive pull-up resistors. If either the FULL or EMPTY pins are forced Low via external control, the corresponding **write** or **read** cycle may resume (provided external FULL or EMPTY input is held Low until the corresponding $\overline{WRITE}$ or $\overline{READ}$ output goes Low) and the address/status counters will continue normal operation* — refer to Table 1.

The user must force the $\overline{RESET}$ input Low to initialize the chip. (**Note**. If the $\overline{RESET}$ signal is driven Low during a **write** or **read** cycle, the address output may have a short period of uncertainty before assuming a high-impedance state.) The following actions occur when $\overline{RESET}$ is active:

- All internal counters are set to "0".
- All address output lines are forced to the high-impedance state.
- HALF FULL and FULL outputs are forced Low.
- $\overline{WRITE}$, $\overline{READ}$, and EMPTY outputs are forced high.

When $\overline{CE}$ is High, the address output lines are forced to the high-impedance state, further **write** or **read** cycle requests are ignored, and all counters remain unchanged. If $\overline{CE}$ switches from Low-to-High during a **write** or **read** cycle, the cycle in progress is always completed before the disabled state is entered. For details of these operations, refer to the timing information shown later in this data sheet.

* Refer to **Note** on inside back cover

## Table 1. Summary of Operation

| INPUTS | | | | INITIAL | RESULTING OUTPUTS | | | COMMENTS |
|---|---|---|---|---|---|---|---|---|
| $\overline{RESET}$ | $\overline{CE}$ | $\overline{SI}$ | $\overline{SO}$ | CONDITIONS | $\overline{WRITE}$ | $\overline{READ}$ | Address Bus | |
| L | X | X | X | | H | H | Hi-Z | Reset all counters to 0. |
| H | X | H | H | | H | H | Hi-Z | No action |
| H | L | L | H | FULL = L | L | L | Write address from Ctr #1 | Shift into FIFO stack (Write Cycle) |
| H | L | L | H | FULL = H | H | H | Hi-Z | Stack full (write inhibited) |
| H | L | H | L | EMPTY = L | H | L | Read address from Ctr #2 | Shift out of FIFO stack (Read Cycle) |
| H | L | H | L | EMPTY = H | H | H | Hi-Z | Stack empty (read inhibited) |
| H | L | L | ↓ | Write cycle in progress | L | H | Write address from Ctr #1 | Continue write cycle (until $\overline{SI}$ goes high) |
| H | L | ↓ | L | Read cycle in progress | H | L | Read address from Ctr #2 | Continue read cycle (until $\overline{SO}$ goes high) |
| H | L | L | L | EMPTY = H | L | H | Write address from Ctr #1 | Shift in (read inhibited) |
| H | L | L | L | FULL = H | H | L | Read address from Ctr #2 | Shift out (write inhibited) |
| H | L | ↑ | H | Write cycle in progress | ↑ | H | Goes to Hi-Z | Increment write address counter #1 and status counter #3 |
| H | L | H | ↑ | Read cycle in progress | H | ↑ | Goes to Hi-Z | Increment read address counter #2; decrement status counter #3 |
| H | L | ↑ | L | Write cycle in progress[1] | ↑ | ↓ | Changes to read address from Ctr #2 | Increment write address counter #1 and status counter #3 |
| H | L | L | ↑ | Read cycle in progress[2] | ↓ | ↑ | Changes to write address from Ctr #1 | Increment read address counter #2; decrement status counter #3 |
| H | H | ↓ | H | | H | H | Hi-Z | Chip disabled |
| H | H | H | ↓ | | H | H | Hi-Z | Chip disabled |
| H | ↑ | L | X | FULL = L; write cycle begun[1] | L | H | Write address from Ctr #1 | Continue write cycle (until $\overline{SI}$ goes high) |
| H | ↑ | L | X | EMPTY = L; read cycle begun[2] | H | L | Read address from Ctr #2 | Continue read cycle (until $\overline{SO}$ goes high) |
| H | ↓ | L | L | FULL = L; EMPTY = L | – | – | – | This set of conditions should be avoided |

**NOTES:**
1. Write cycle will occur if either SI goes Low before $\overline{SO}$ goes Low or EMPTY = H when $\overline{SO}$ goes Low.
2. Read cycle will occur if either $\overline{SO}$ goes Low before $\overline{SI}$ goes Low or FULL = H when $\overline{SI}$ goes Low.

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +7 | $V_{DC}$ |
| $V_{BB}$ | Supply voltage for internal circuits | +4 | $V_{DC}$ |
| $V_I$ | Input voltage | +5.5 | $V_{DC}$ |
| $V_O$ | Off-state output voltage | +5.5 | $V_{DC}$ |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V, -55°C \leq T_C \leq +125°C$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| $V_{IH}$ | High level input voltage[3] | | 2.0 | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.8 | V |
| $V_{OH}$ | High level output voltage: All outputs except FULL and EMPTY | $V_{CC}$ = MIN; $I_{OH}$ = –2.6mA | 2.5 | | | V |
| $V_{OL}$ | Low level output voltage: Address Bus, $\overline{WRITE}$, $\overline{READ}$ | $V_{CC}$ = MIN; $I_{OL}$ = 16mA | | 0.38 | 0.5 | V |
| $V_{OL}$ | HALF FULL, FULL, and EMPTY | $V_{CC}$ = MIN; $I_{OL}$ = 8mA | | 0.35 | 0.5 | V |
| $V_{IK}$ | Diode clamp voltage: All inputs except FULL and EMPTY | $V_{CC}$ = MIN; $I_{IK}$ = –18mA | | –0.8 | –1.5 | V |
| $I_{IH}$ | High level input current: All inputs except FULL and EMPTY | $V_{CC}$ = MAX; $V_{IH}$ = 2.7V | | 0.1 | 20 | µA |
| $I_{IH}$ | FULL and EMPTY | $V_{CC}$ = MAX; $V_{IH}$ = 2.7V; stack FULL or stack EMPTY[3] | | –470 | –900 | µA |
| $I_{IL}$ | Low level input current: All inputs except FULL and EMPTY | $V_{CC}$ = MAX; $V_{IL}$ = 0.4V | | –0.17 | –0.4 | mA |
| $I_{IL}$ | FULL and EMPTY | $V_{CC}$ = MAX; $V_{IL}$ = 0.4V; Stack FULL or Stack EMPTY | | –1.12 | –1.8 | mA |
| $I_{OH}$ | High level output current: FULL, EMPTY | $V_{CC}$ = MIN; $V_{OH}$ = $V_{CC}$ (MIN) | | 15 | 100 | µA |
| $I_{OZH}$ | Hi-Z output current (HIGH); address bus (3-State) | $V_{CC}$ = MAX; $V_{OUT}$ – 2.4V | | 0.9 | 20 | µA |
| $I_{OZL}$ | Hi-Z output current (LOW); address bus (3-State) | $V_{CC}$ = MAX; $V_{OUT}$ = 0.5V | | –0.6 | –20 | µA |
| $I_I$ | Input leakage current: All inputs except FULL and EMPTY | $V_{CC}$ = MAX; $V_{IN}$ = 5.5V | | 0.03 | 0.1 | mA |
| $I_{OS}$ | Short-circuit output current: address bus and HALF FULL | $V_{CC}$ = MAX; $V_{OH}$ = 0V | –15 | –68 | –100 | mA |
| $I_{OS}$ | $\overline{WRITE}$, $\overline{READ}$ | $V_{CC}$ = MAX; $V_{OH}$ = 0V | –40 | –73 | –100 | mA |
| $I_{CC}$ | Supply current from $V_{CC}$ | $V_{CC}$ = MAX; Address Bus = Hi-Z; –55°C → | | 81 | 140 | mA |
| | | +25°C → | | 81 | 122 | mA |
| | | +125°C → | | 81 | 100 | mA |
| $I_{BB}$ | Supply current from $V_{BB}$ | $V_{BB}$ = MAX; –55°C → | | 63 | 100 | mA |
| | | +25°C → | | 63 | 95.5 | mA |
| | | +125°C → | | 63 | 90 | mA |

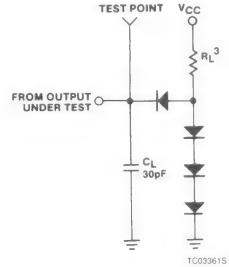
## AC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq +125°C$

| SYMBOL | PARAMETERS | REFERENCES | | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | From | To | | Min | Typ | Max | |
| **Pulse Widths** | | | | | | | | |
| $T_{LH}$ | $\overline{SI}$ high | ↑$\overline{SI}$ | ↓$\overline{SI}$ | Stack approaching FULL[4] | 30 | 13 | | ns |
| $T_{DH}$ | $\overline{SO}$ high | ↑$\overline{SO}$ | ↓$\overline{SO}$ | Stack approaching EMPTY[4] | 30 | 16 | | ns |
| **Write Cycle Timing** | | | | | | | | |
| $T_{LA}$ | Address stable delay | ↓$\overline{SI}$ | An | FULL = Low; $\overline{SO}$ = High | | 40 | 60 | ns |
| $T_{AW}$ | Address lead time | An | ↓$\overline{WRITE}$ | | 0 | | | ns |
| $T_{LAW}$ | $\overline{WRITE}$ output active delay | ↓$\overline{SI}$ | ↓$\overline{WRITE}$ | FULL = Low; $\overline{SO}$ = High | 40 | 51 | 77 | ns |
| $T_{LW}$ | $\overline{WRITE}$ output inactive delay | ↑$\overline{SI}$ | ↑$\overline{WRITE}$ | | | 3 | 10 | ns |
| $T_{WA}$ | Address lag time | ↑$\overline{WRITE}$ | An | | 20 | 34 | | ns |
| $T_{LT}$ | Address output disable | ↑$\overline{SI}$ | An (Hi-Z) | | | 37 | 65 | ns |
| $T_{LF}$ | FULL status active delay | ↓$\overline{SI}$ | ↑FULL | Stack approaching FULL: $\overline{SO}$ = High | | 39 | 70 | ns |
| $T_{LE}$ | EMPTY status inactive delay | ↓$\overline{SI}$ | ↓EMPTY | Stack = EMPTY | | 40 | 70 | ns |
| $T_{HFH}$ | HALF-FULL status active delay | ↑$\overline{SI}$ | ↑HALF FULL | Stack approaching HALF-FULL | | 30 | 50 | ns |
| $T_{DW}$ | $\overline{WRITE}$ output active after read | ↑$\overline{SO}$ | ↓$\overline{WRITE}$ | Both $\overline{SI}$ & $\overline{READ}$ = Low | | 74 | 110 | ns |
| **Read Cycle Timing** | | | | | | | | |
| $T_{DA}$ | Address stable delay | ↓$\overline{SO}$ | An | EMPTY = Low; $\overline{SI}$ = High | | 40 | 60 | ns |
| $T_{AR}$ | Address lead time | An | ↓$\overline{READ}$ | | –5 | | | ns |
| $T_{DAR}$ | $\overline{READ}$ output active delay | ↓$\overline{SO}$ | ↓$\overline{READ}$ | EMPTY – Low; $\overline{SI}$ – High | | 48 | 75 | ns |
| $T_{DR}$ | $\overline{READ}$ output inactive delay | ↑$\overline{SO}$ | ↑$\overline{READ}$ | | | 5 | 10 | ns |
| $T_{RA}$ | Address lag time | ↑$\overline{READ}$ | An | | 10 | 32 | | ns |
| $T_{DT}$ | Address output disable | ↑$\overline{SO}$ | An (Hi-Z) | | | 37 | 70 | ns |
| $T_{DE}$ | EMPTY status active delay | ↓$\overline{SO}$ | ↑EMPTY | Stack approaching EMPTY; $\overline{SI}$ = High | | 38 | 50 | ns |
| $T_{DF}$ | FULL status inactive delay | ↓$\overline{SO}$ | ↓FULL | Stack = FULL | | 38 | 65 | ns |
| $T_{HFL}$ | HALF-FULL status inactive delay | ↑$\overline{SO}$ | ↓HALF FULL | Stack exactly HALF-FULL | | 54 | 85 | ns |
| $T_{LR}$ | $\overline{READ}$ output active after write | ↑$\overline{SI}$ | ↓$\overline{READ}$ | Both $\overline{SO}$ & $\overline{WRITE}$ = Low | | 70 | 100 | ns |
| **Chip Enable Timing (Write)** | | | | | | | | |
| $T_{HEW}$ | Chip enable hold time[5] | ↓$\overline{SI}$ | ↑$\overline{CE}$ | FULL = Low; $\overline{SO}$ = High | | 1 | 10 | ns |
| $T_{SEW}$ | Chip disable set-up time[6] | ↑$\overline{CE}$ | ↓$\overline{SI}$ | FULL = Low; $\overline{SO}$ = High | 10 | 1 | | ns |
| $T_{PEW}$ | Chip enable delay time | ↓$\overline{CE}$ | ↓$\overline{WRITE}$ | FULL = Low; $\overline{SI}$ = Low; $\overline{SO}$ - High | | 69 | 110 | ns |
| **Chip Enable Timing (Read)** | | | | | | | | |
| $T_{HER}$ | Chip enable hold time[5] | ↓$\overline{SO}$ | ↑$\overline{CE}$ | EMPTY = Low; $\overline{SI}$ = High | | 1 | 12 | ns |
| $T_{SER}$ | Chip disable set-up time[6] | ↑$\overline{CE}$ | ↓$\overline{SO}$ | EMPTY = Low; $\overline{SI}$ = High | 10 | 1 | | ns |
| $T_{PER}$ | Chip enable delay time | ↓$\overline{CE}$ | ↓$\overline{READ}$ | EMPTY = Low; $\overline{SO}$ = Low; $\overline{SI}$ = High | | 64 | 105 | ns |
| **Reset Timing** | | | | | | | | |
| $T_{RR}$ | $\overline{RESET}$ recovery | ↑$\overline{RESET}$ | ↓$\overline{WRITE}$ | $\overline{SI}$ = Low | | 57 | 85 | ns |
| $T_{RL}$ | $\overline{RESET}$ pulse width (low) | ↓$\overline{RESET}$ | ↑$\overline{RESET}$ | | 25 | 8 | | ns |
| **Full/Empty Override Timing** | | | | | | | | |
| $T_{FW}$ | Override recovery for FULL | ↓FULL | ↓$\overline{WRITE}$ | Stack = Full; $\overline{SI}$ = Low; $\overline{SO}$ = High | | 70 | 110 | ns |
| $T_{ER}$ | Override recovery for EMPTY | ↓EMPTY | ↓$\overline{READ}$ | Stack = EMPTY; $\overline{SO}$ = Low; $\overline{SI}$ = High | | 65 | 105 | ns |

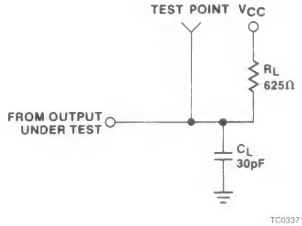
**NOTES:**
1. $V_{BB}$ should be obtained from a regulated 1.5V supply.
2. Typical limits are: $V_{CC}$ = 5.0V; $T_A$ = 25°C.
3. Because of the internal pull-up resistor on the FULL and EMPTY pins, a negative current is required to force the required voltage.
4. Such that write/read request is inhibited after stack becomes full/empty.
5. The earliest rising edge of $\overline{CE}$ such that the $\overline{WRITE}$ or $\overline{READ}$ output always occurs.
6. The latest rising edge of $\overline{CE}$ such that the $\overline{WRITE}$ or $\overline{READ}$ output never occurs.

## AC TEST CIRCUITS

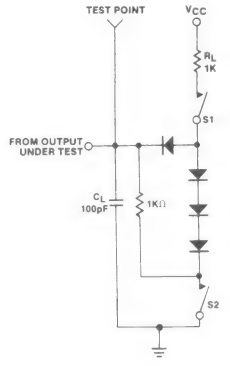
**APPLICABLE PINS: $\overline{\text{WRITE}}$ (7), $\overline{\text{READ}}$ (8), HALF FULL (10)**




**APPLICABLE PINS: FULL (8) AND EMPTY (11)**



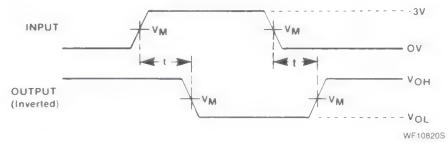

**APPLICABLE PINS: $A_n$ (15 – 20, 22 – 27)**




| OUTPUT STATE | | SWITCH POSITION | |
|---|---|---|---|
| FROM | TO | S1 | S2 |
| Low | High | Closed | Closed |
| High | Low | Closed | Closed |
| High | HI-Z | Closed | Closed |
| Low | HI-Z | Closed | Closed |
| HI-Z | High | Open | Closed |
| HI-Z | Low | Closed | Open |

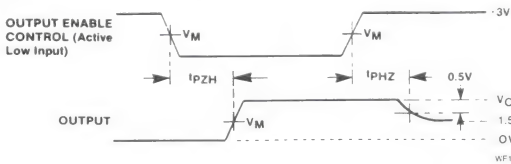
**NOTES:**
1. In all cases $C_L$ includes probe and jig capacitance
2. All diodes are 1N916, 1N3064, or equivalent.
3. For $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ outputs, $R_L$ = 280 ohms; for HALF FULL output, $R_L$ = 2K ohms.

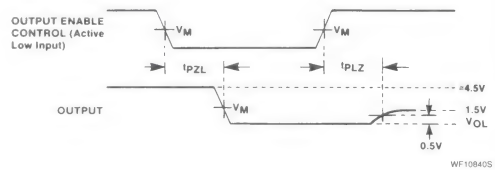
## AC TEST WAVEFORMS




**Propagation Delay**
(Typical Example)

**NOTE:**
Pulse widths and Setup/Hold times are measured using the same reference points as above waveform.



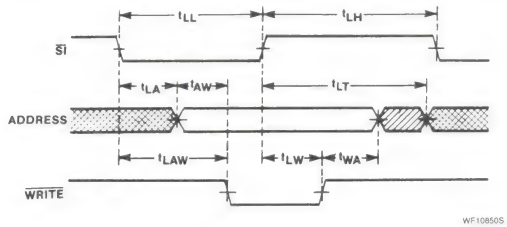




For all waveforms, $V_M$ = 1.5V.

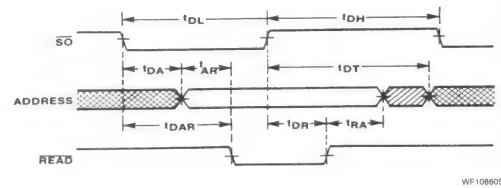
**3-State Enable Time to LOW Level and Disable Time From LOW Level**

**3-State Enable Time to HIGH Level and Disable Time From HIGH Level**

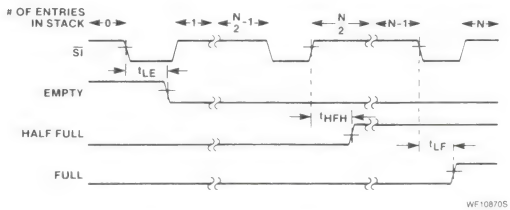
## TIMING DIAGRAMS



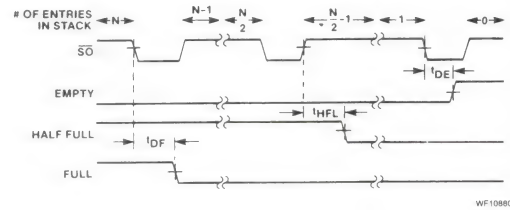

Write Cycle Timing



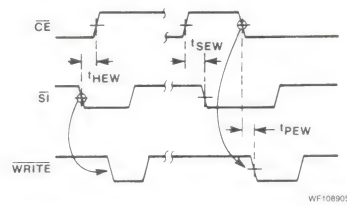

Read Cycle Timing



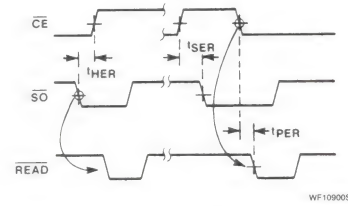

Status Output Timing-Write




Status Output Timing-Read



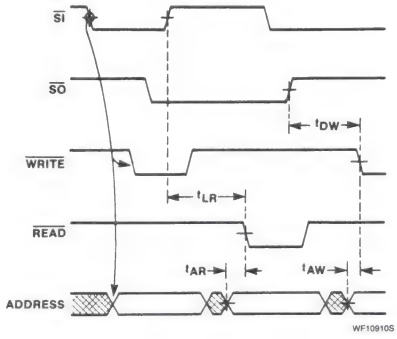

Chip Enable Timing Write*



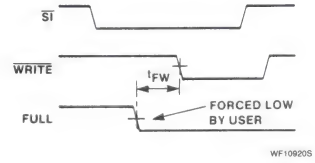

Chip Enable Timing Read[1]

NOTE:
The rising edge of $\overline{CE}$ should not occur within 10-nanoseconds before or after a falling edge of $\overline{SI}$ or $\overline{SO}$.

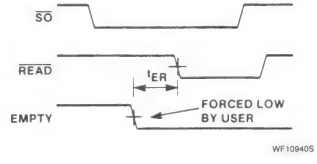
## TIMING DIAGRAMS (Continued)



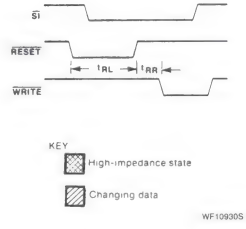

Change of Cycle Timing




Full Override Timing

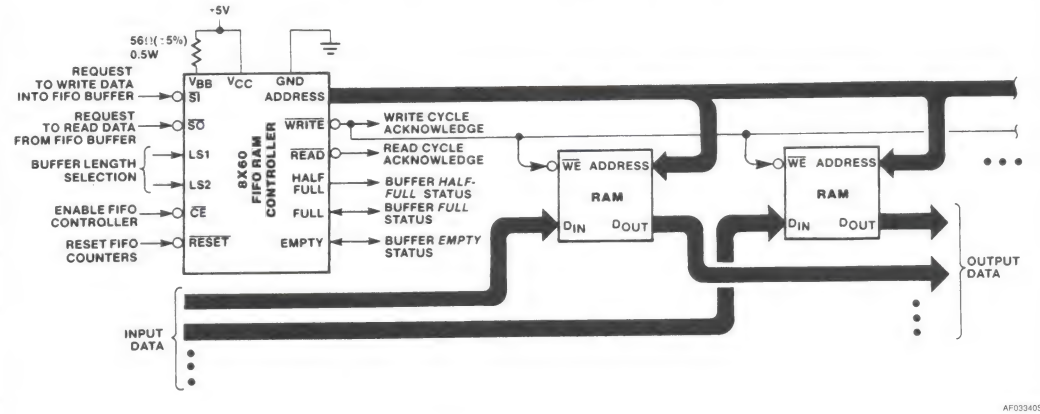



Empty Override Timing

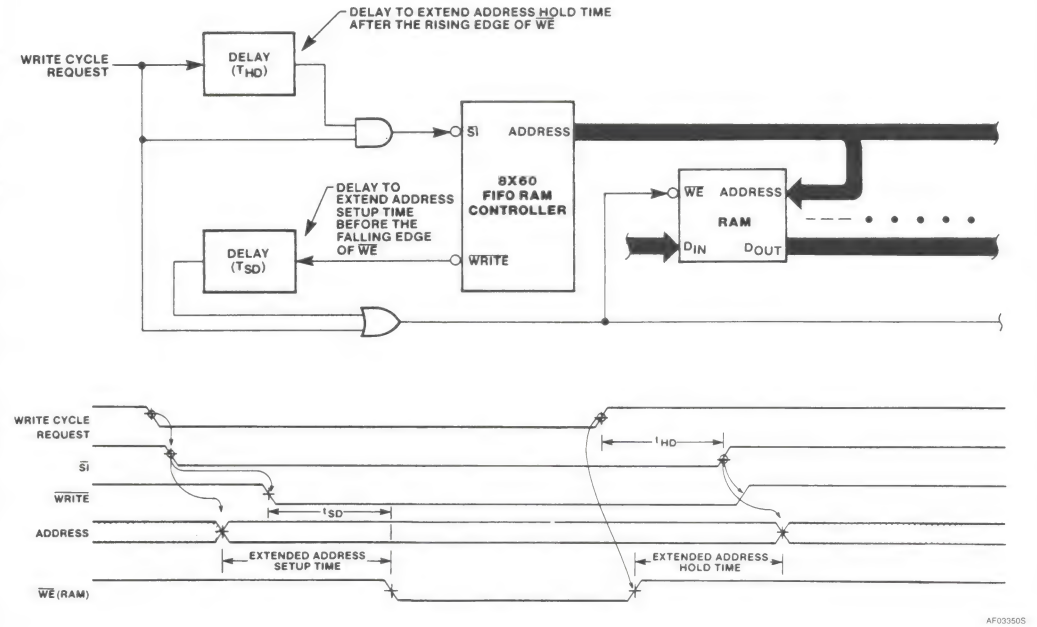



Reset Timing

## APPLICATIONS




Implementation of a FIFO Buffer Using the 8X60 and High-Speed RAM




Using 8X60 With High-Density MOS RAMs

Signetics

# 8X305
## Microcontroller

***Product Specification***

**Military**
**Customer Specific Products**

### FEATURES

- **Fetch, Decode, and Execute a 16-bit Instruction in a minimum of 200ns (one machine cycle)**
- **Bit-oriented Instruction set (addressable single- or multiple-bit subfields)**
- **Separate buses for Instruction, Instruction Address and 3-State I/O**
- **Thirteen 8-bit general-purpose working registers**
- **Source/destination architecture**
- **Bipolar low-power Schottky technology/TTL inputs and outputs**
- **On-chip oscillator and timing generation**
- **Single +5V supply**
- **Multiple package options**

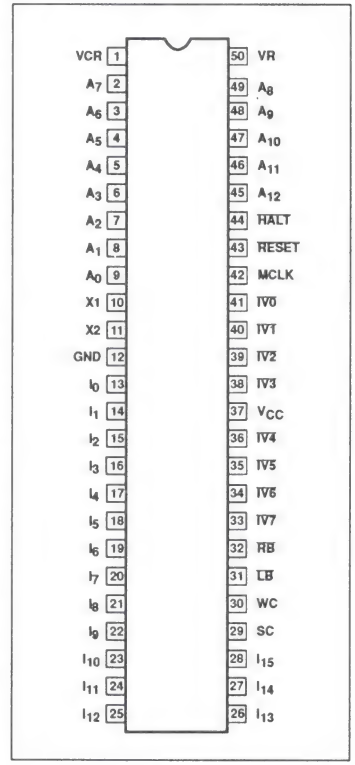
### PRODUCT DESCRIPTION

The Signetics 8X305 Microcontroller is a high-speed bipolar micro-processor implemented with low- power Schottky technology. In a single chip, the 8X305 combines speed, flexibility, and a bit-oriented instruction set. These features and other basic characteristics of the chip combine to provide cost-effective solutions for a broad range of applications. The 8X305 is particularly useful in systems that require high-sped bit manipulations — sophisticated controllers, data communications, very fast interface control, and other applications of a similar nature.

The 8X305 can fetch, decode, and execute a 16-bit instruction word in a minimum of 200ns. Within one instruction cycle, the 8-bit data-processing path can be programmed to rotate, mask, shift, and/or merge single or multiple bit subfields and, in addition, perform an ALU operation; in the same instruction, an external data field can be input, processed, and output to a specified destination — likewise, single or multiple bit data fields can be fetched, processed, operated on by the ALU, and moved to a different location — all in a timeframe of 200ns. To interface with I/O and program memory, the 8X305 uses a 13-bit instruction address bus, a 16-bit instruction bus, an 8-bit bidirectional multiplexed I/O data/address bus and a 5-bit I/O control bus.

A wide selection of I/O devices, interface chips, and special-purpose parts are available for systems use. In most applications, the more powerful 8X305 is functionally interchangeable with its predecessor — the 8X300.

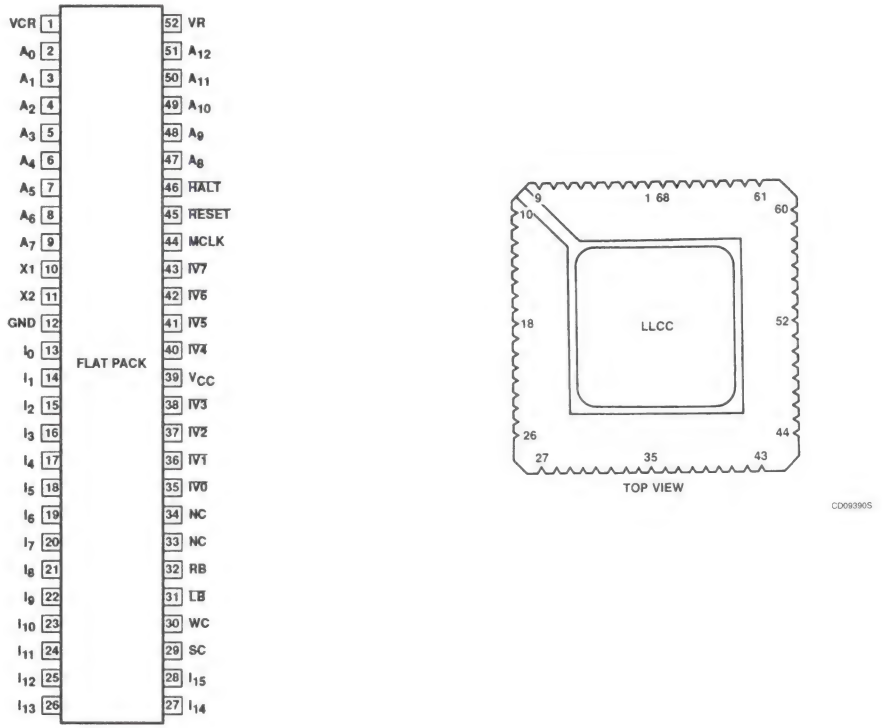
### PIN CONFIGURATION




### ORDERING INFORMATION

| PACKAGES | CLOCK FREQUENCY | ORDER CODE |
|---|---|---|
| 50–Pin DIP 0.9in | 10MHz | 8X305–10/BXA |
| 68–Pin LLCC | 10MHz | 8X305–10/BUA |
| 52–Pin FLAT PACK | 10MHz | 8X305–10/BYA |
| 50–Pin DIP 0.9in | 8MHz | 8X305/BXA |
| 68–Pin LLCC | 8MHz | 8X305/BUA |
| 52–Pin FLAT PACK | 8MHz | 8X305/BYA |

## PIN CONFIGURATIONS




## PIN DESCRIPTION

| FLATPACK PIN NO. | LLCC PIN NO. | DIP PIN NO. | IDENTIFIER | FUNCTION |
|---|---|---|---|---|
| 1 | 1, 68 | 1 | VCR | Regulated voltage input from series-pass transistor (2N5320 or equivalent). |
| 2–9, 47–51 | 4–11, 62–66 | 2–9, 45–49 | $A_0 - A_{12}$ | Program Address Lines: These active-high outputs permit direct addressing of up to 8192 words of program storage; $A_{12}$ is Least Significant Bit. |
| 10–11 | 12, 13 | 10, 11 | X1, X2 | Timing generator connections for a capacitor, a series resonant crystal, or an external clock source with complementary outputs. |
| 12 | 2,3, 14–16 | 12 | GND | Ground. |
| 13–28 | 17–23, 28–36 | 13–28 | $I_0 - I_{15}$ | Instruction Lines: These active-high input lines receive 16-bit instructions from program storage; $I_{15}$ is Least Significant Bit. |
| 29 | 37 | 29 | SC | Select Command: When high (binary 1), an address is being output on pins $\overline{IV0}$ through $\overline{IV7}$. |
| 30 | 38 | 30 | WC | Write Command: When high (binary 1), data is being output on pins $\overline{IV0}$ through $\overline{IV7}$. |
| 31 | 39 | 31 | $\overline{LB}$ | Left Bank Control: When low (binary 0), devices connected to the Left Bank are accessed. (Note: Typically the $\overline{LB}$ signal is tied to the $\overline{ME}$ input pin of I/O peripherals.) |

| FLATPACK PIN NO. | LLCC PIN NO. | DIP PIN NO. | IDENTIFIER | FUNCTION |
|---|---|---|---|---|
| 32 | 45 | 32 | RB | Right Bank Control: When low (binary 0), devices connected to the Right Bank are accessed. (Note: Typically, the $\overline{RB}$ signal is tied to the $\overline{ME}$ input pin of I/O peripherals.) |
| 35–38, 40–43 | 46–49, 55–58 | 33–36, 38–41 | $\overline{IV0}$ – $\overline{IV7}$ | Interface Vector (Input/Output Bus) — these bidirectional active-low 3-State lines communicate data and/or addresses to I/O devices and memory locations. A low voltage level equals a binary "1"; $\overline{IV7}$ is Least Significant Bit. |
| 39 | 50–52 | 37 | $V_{CC}$ | +5V power supply. |
| 44 | 59 | 42 | MCLK | Master Clock: This active-high output signal is used for clocking I/O devices and/or synchronization of external logic. |
| 45 | 60 | 43 | $\overline{RESET}$ | When $\overline{RESET}$ input is low (binary 0), the 8X305 is initialized — sets Program Counter/Address Register to zero and inhibits MCLK. For the period of time $\overline{RESET}$ is low, the Left Bank/Right Bank ($\overline{LB}$/$\overline{RB}$) signals are forced high asynchronously. |
| 46 | 61 | 44 | $\overline{HALT}$ | When $\overline{HALT}$ input is low (binary 0), internal operation of the 8X305 stops at the start of next instruction; MCLK is not inhibited nor is any internal register affected; however, both the Left Bank/Right Bank ($\overline{LB}$/$\overline{RB}$) signals are synchronously driven high during the first quarter of the instruction cycle time and remain high during the time HALT is low. |
| 52 | 67 | 50 | VR | Internally-generated reference output voltage for external series-pass regulator transistor. |
| 33, 34 | 24–27, 40–44, 53, 54 | – | No Connect | |

**NOTE:** Multiple $V_{CC}$, GND, and $V_{CR}$ pins must be externally connected.

## ELECTRICAL PERFORMANCE CHARACTERISTICS AND TEST REQUIREMENTS

For Absolute Maximum Ratings, Recommended Operating Conditions, and Electrical Test Requirements, refer to Military Drawing 85502.
For Detail Application Notes, contact Signetics Military Marketing at (408) 991–2722.

Signetics

# 8X310
## Interrupt Control Coprocessor

***Product Specification***

**Military**
**Customer Specific Products**

### FEATURES

- **Three prioritized interrupts**
- **Subroutine handling capabilities**
- **4-level LIFO stack for return address storage**
- **Interrupt masking by software and hardware**
- **Stack full flag**
- **Directly compatible with 8X305 Microcontroller**
- **Bipolar ISL (Integrated Schottky Logic) and low-power Schottky technology**
- **Single +5V power supply**
- **0.6", 40-pin DIP**

### PRODUCT DESCRIPTION

The Signetics 8X310 Interrupt Control Coprocessor (ICC) supports the 8X305 Microcontroller in systems that are interrupt driven and those that require subroutine handling capabilities.

As shown in Figure 1, the ICC provides three prioritized interrupt request lines, INT 0 (highest priority), INT 1 and INT 2. A Low-to-High transition applied to any of these input lines latches in an interrupt request which may be serviced when sampled by the ICC once each instruction cycle of the Microcontroller. When an interrupt request is serviced, the ICC forces the Microcontroller to jump to one of three fixed locations in program memory; instruction addresses 4, 5, and 6 correspond to INT 0, INT 1, and INT 2. At each of these addresses, the user programs a JMP instruction to another address where the user's interrupt service routine begins.

During interrupt servicing, the ICC also stores the proper return address into a four deep, Last-In-First-Out (LIFO) stack. At the conclusion of the interrupt service routine, the user program instructs the ICC to return to the main program at the location previously stored in the stack. The return operation is implemented by coding a special RETURN instruction which is decoded directly off the instruction bus by the ICC. There are five such special instructions relating to interrupt and subroutine handling functions performed by the ICC. These instruction codes are all treated as non-operational instructions (NOPs) by the Microcontroller.

An internal one-bit mask is used to inhibit interrupt servicing. Whenever the mask is set, the ICC does not respond to any pending interrupt requests; however, any requests remain latched for future servicing. The mask can be set and cleared either by the user program or automatically during certain ICC functions. The special instructions SET MASK and CLEAR MASK are provided for user control. The Interrupt Disable input also inhibits interrupt request servicing.

### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 40–Pin DIP | 8X310/BQA |

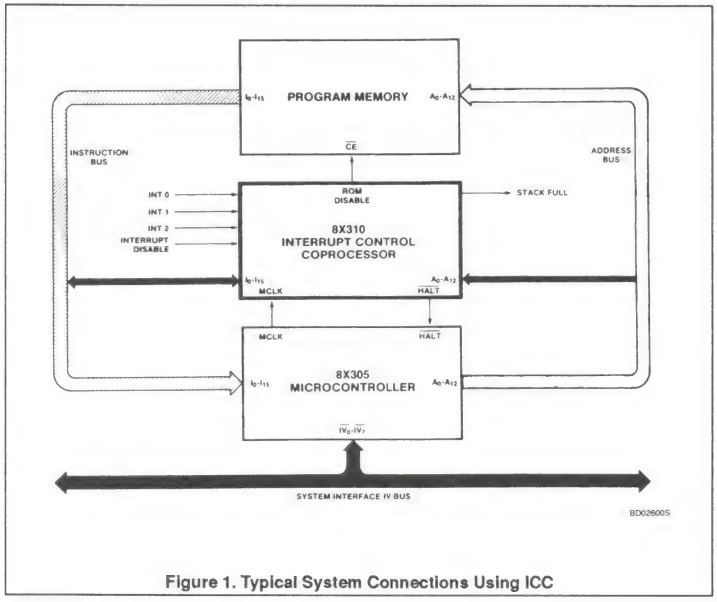
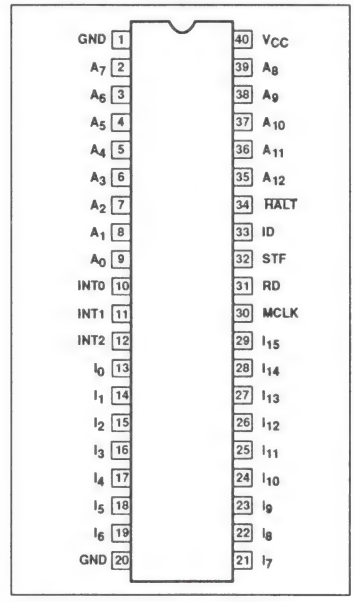



**Figure 1. Typical System Connections Using ICC**

### PIN CONFIGURATION



## PIN DESCRIPTION

| PIN NO. | IDENTIFIER | FUNCTION |
|---|---|---|
| 1, 20 | GND | Ground. (Note: The printed circuit board should not use the ICC as a bridge for external ground.) |
| 2 – 9, 35 – 39 | $A_7$, $A_0$, $A_{12} - A_8$ | Program address input lines from Microcontroller. Active High. $A_0$ is MSB. |
| 10 – 12 | INT 0 – INT 2 | Interrupt request input pins. INT 0 has the highest priority and INT 2 the lowest — Edge-triggered on a Low-to-High transition. |
| 13 – 19 | $I_0 - I_6$, | Bidirectional instruction bus; $I_0$ is MSB. When acting as an input, the ICC decodes the instruction flow (binary pattern on $I_0 - I_{15}$) between program storage and the Microcontroller. During an interrupt or return cycle, the ICC outputs a JMP instruction to the Microcontroller via these lines — refer to FUNCTIONAL OPERATION of ICC. |
| 30 | MCLK | MasterCLocK — Active-High input from 8X305 Microcontroller used for a timing reference and system synchronization. |
| 31 | RD | ROM (or PROM) Disable — Active-High output used to disable normal program storage so that the ICC can force an instruction to the Microcontroller. |
| 32 | STF | STack Full — Active-High output. When the LIFO stack if full, STF goes High and remains High until at least one register in the 4-level stack is empty. |
| 33 | ID | Interrupt Disable — Active-High. When this input pin is driven High, servicing of all interrupt requests is suspended. |
| 34 | $\overline{HALT}$ | Active-Low output. Suspends all processing operations of the Microcontroller during period when the source of instruction data is changing between the ICC and program storage. |
| 40 | $V_{CC}$ | +5V power supply. |

The ICC provides a facility for implementing subroutines in the user program. A special PUSH instruction directs the ICC to store the return address into the stack in a manner similar to interrupt servicing. The jump to the subroutine, however, is performed by the user program. Subroutines may be nested (called from within other subroutines) depending on remaining vacancies in the four deep stack.

In general, the ICC adds some useful and very flexible facilities to the 8X305-based system. It offers both hardware and software capabilities that can improve efficiency and decrease program size. These features, from both a chip and system aspect, are described in subsequent paragraphs.

## FUNCTIONAL OPERATION

### Basic Functions

The ICC performs the three general functions indicated below.

**Function 1:** Provides a means for the 8X305 Microcontroller to respond to interrupt requests by diverting the program flow of the 8X305 Microcontroller to the proper interrupt service routine or, in the case of a subroutine, the IC stores the return address in the 4-level LIFO stack (Figure 2.)

**Function 2:** Returns the user to the proper point in the man program for both interrupt and subroutine activities.

**Function 3:** Provides both automatic and programmed masking capabilities.

### Interrupt Requests and Priority Considerations

An interrupt is requested when any one of the ICC input pins INT 0, INT 1, or INT 2 undergoes a Low-to-High transition; this request is temporarily stored in an internal edge-triggered latch that corresponds to the affected interrupt input. The interrupt request latches are part of the Priority and Mask Logic shown in Figure 2. Unless masked or otherwise disabled, the ICC samples these latches once each instruction cycle. Any or all of the latches may be set when sampled by the ICC; however, only the interrupt of highest priority will be serviced — the remaining interrupts will be held in queue. Thus, if INT 0, INT 1 and INT 2 simultaneously compete for service, INT 0 is the first to be serviced followed, in order, by INT 1 and INT 2; likewise, if INT 1 and INT 2 compete for service, INT 1, being of higher priority will be serviced first. The CLEAR INTERRUPT instruction resets all interrupt request latches without affecting an interrupt service routine that is already in progress.

The highest priority interrupt request will be serviced when sampled by the ICC provided interrupts in general are not inhibited and a previous interrupt of equal or higher priority is not currently being serviced. The general masking of interrupts is discussed later. To determine priorities, the ICC keeps track of any interrupt that is serviced until the corresponding service routine returns. A subsequent interrupt request may interrupt a service routine in progress only if it is of a higher priority than that of the current interrupt being serviced. If, for example, INT 1 is requested and serviced, then before its service routine finishes, a request on INT 0 can be serviced as a second level interruption. However, a request on INT 2 or a second request on INT 1 must wait until the original INT 1 service routine returns. The interrupt service routine that was interrupted will resume execution at the point of interruption when the higher priority service routine returns (i.e., in the same manner as when returning to the main program).

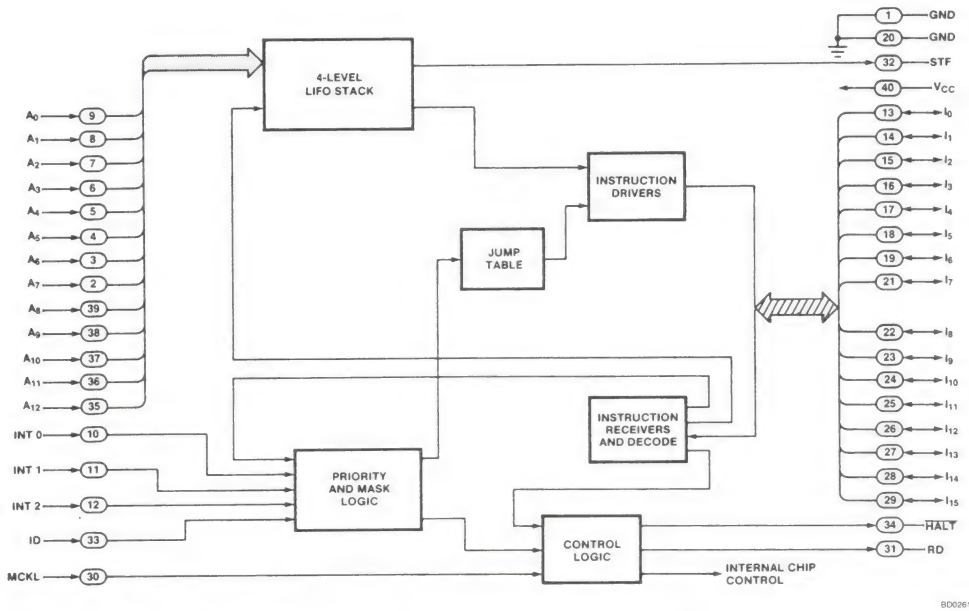



**Figure 2. 8X310 Interrupt/Control Coprocessor — Functional Block Diagram**

## Interrupt Servicing

Interrupts are sampled only at the conclusion of an instruction cycle while the next instruction is being fetched from Program Memory.

When an interrupt request is serviced, the following general steps are performed:

- Address of the instruction that would normally be executed next is pushed into the 4-level LIFO Stack (Figure 2) for subsequent return to the main program.
- The ICC disables program storage and forces a JMP instruction onto the Instruction bus of the 8X305 Microcontroller. (Note: because of timing considerations, the HALT signal is driven low to suspend operation of the Microcontroller for one instruction cycle; this permits the source of instruction data to change from program storage to the ICC without conflict.) The JMP instruction from the ICC transfers the Microcontroller to one of the three fixed program locations shown below. In each of these addresses, the user will normally store a JMP instruction to the interrupt service routine for that particular interrupt. Details of these operations are described later.

INT 0 . . . . . Address 4

INT 1 . . . . . Address 5

INT 2 . . . . . Address 6

## Return from Interrupt Service Routine

Upon completion of the interrupt service routine, the user codes the special RETURN instruction. When executed, the ICC performs the following steps:

- The return address is popped from the LIFO stack
- The ICC disables program storage and forces a JMP instruction onto the Microcontroller instruction bus with the return address from the stack. (The HALT signal is driven low for one instruction cycle.)
- The JMP instruction from the ICC transfers the Microcontroller to the instruction that was about to execute at the time the interrupt was taken.

A typical structure for a user program which handles interrupts is shown in the following example:

| ADDRESS | INSTRUCTION | | COMMENT |
|---|---|---|---|
| 0 | | (any) | First instruction executed after system reset |
| • | | • | |
| • | | • | |
| 3 | | JMP MAIN | Jump around interrupt vector locations. |
| 4 | | JMP SERV0 | Service INT 0 interrupt. |
| 5 | | JMP SERV1 | Service INT 1 interrupt. |
| 6 | | JMP SERV2 | Service INT 2 interrupt. |
| 7 | MAIN | (any) | Continue main program. |
| • | | • | |
| • | | • | |
| | SERV0 | (any) | Begin INT 0 service routine. |
| • | | • | |
| • | | • | |
| | | MAIN R6,R6 | ICC RETURN instruction. End INT 0 service routine (resume main program execution). |
| | SERV1 | (any) | Begin INT 1 service routine. |
| • | | • | |
| • | | • | |
| | | MOVE R6,R6 | RETURN from INT 1 service routine. |
| | SERV2 | (any) | Begin INT 2 service routine. |
| • | | • | |
| • | | • | |
| | | MOVE R6,R6 | RETURN from INT 2 service routine. |

**Table 1. Instruction Set For ICC**

| INSTRUCTION | INSTRUCTION CODES | | 8X305 OPERATION | DESCRIPTION OF ICC OPERATION |
|---|---|---|---|---|
| | Assembler | Binary | | |
| | | $I_0$ = MSB $I_{15}$ = LSB ↓ ↓ | | |
| SET MASK | MOVE R5,R5 | 000 00101 000 00101 | NOP | When executed, sets interrupt mask, thus inhibiting all interrupt servicing. |
| CLEAR MASK | MOVE R4,R4 | 000 00100 000 00100 | NOP | When executed, clears interrupt mask for all interrupts. |
| RETURN | MOVE R6,R6 | 000 00110 000 00110 | NOP | When executed returns program to address at top of LIFO stack. |
| PUSH | MOVE R3,R3 | 000 00011 000 00011 | NOP | Pushes "address + 2" onto stack if PUSH is programmed on odd address in program memory and "address + 1" if PUSH is programmed on even address. |
| CLEAR INTERRUPT | MOVE R2,R2 | 000 00010 000 00010 | NOP | Clears all interrupt requests; an interrupt service routine that is in progress is unaffected. |

## Instruction Set

The five instructions shown in Table 1 allow the user to efficiently manage both the interrupt and subroutine capabilities of the ICC in an 8X310/8X305-based system. When an ICC instruction appears in the program, it is interpreted as a NOP by the 8X305 but is captured and decoded by the ICC to perform the desired function. The capture-and-decode functions of the chip are automatic. Assembly and object codes for each ICC instruction are shown in Table 1.

## Interrupt Masking Operations

Certain operations performed by the ICC and also some system considerations require that program execution not be interrupted for a specified interval of time. The servicing of interrupts by the ICC can be inhibited in a number of ways. Any time interrupts are inhibited, the ICC ignores any latched interrupt requests. However, the interrupt request latches are not cleared so that any previously pending requests remain latched. Also, during an interval when interrupt servicing is inhibited, any new interrupt signals received will get latched. As soon as interrupt servicing is enabled, any latched requests can be serviced on a priority basis.

The primary means of inhibiting interrupt servicing is the internal one-bit mask (latch). This mask can be set (to inhibit interrupts) or cleared under control of the user program using the special ICC instructions SET MASK and CLEAR MASK — See Table 1. With these instructions, segments of the user program can be isolated so as to proceed without interruptions. Frequently, uninterruptable segments are needed at the very beginning of the user program (initialization routine) and at the beginning of, or throughout an interrupt service routine. To facilitate this, the ICC automatically sets the mask whenever the Microcontroller executes address zero (typically resulting from a system reset) and whenever the ICC services an interrupt. The ICC also automatically clears the mask after performing a RETURN operation from an interrupt service routine; a RETURN from a subroutine does not affect the status of the interrupt mask.

The Interrupt Disable (ID) input pin may also be used to inhibit interrupt servicing. Interrupt servicing remains disabled as long as a high level is applied to the input. The ID input has no effect, however, on the status of the internal interrupt mask.

To ensure proper program flow, the ICC suspends interrupt servicing momentarily during certain situations. During the cycle in which the Microcontroller encounters and XEC (Execute) instruction an interrupt will not be serviced. This is because the XEC causes the Microcontroller to issue an address of an instruction to be executed out of the sequence of normal program flow. This would not be a valid address.

Interrupts are also suspended during execution of a PUSH or RETURN instruction and the instruction immediately following. This ensures proper operation of the LIFO stack. In addition, no interrupts are latched or serviced and no special ICC instructions are decoded at address zero which resets the ICC.

## Subroutine Calling

The ICC provides for subroutine calling by storing the proper return address into the LIFO stack under control of the user program. Two instructions are required to implement a subroutine call — a PUSH instruction executed by the ICC and a JMP to the subroutine executed by the Microcontroller. The PUSH instruction is normally programmed at an odd-numbered address in program memory immediately followed by the JMP. When the PUSH instruction is executed, the ICC finds the address of the next instruction (JMP to subroutine) on the Microcontroller's address bus, internally changes the least-significant bit to one (effectively adds one to the address) and stores this into the stack. Program execution proceeds normally and the Microcontroller makes the jump to the beginning of the subroutine. The subroutine may be located at any convenient place in program memory.

Upon completion of the subroutine, the user codes the RETURN instruction in the same manner as for an interrupt service routine. At that point, the ICC forces the Microcontroller to resume execution of the main program at the instruction immediately following the JMP-to-subroutine instruction.

The code for a typically subroutine call-and-return is shown in the following example.

| ADDRESS | INSTRUCTION | COMMENT |
|---|---|---|
| X (any odd-numbered address) | MOVE R3,R3 | PUSH instruction initiates subroutine call by causing ICC to push the address X + 2 onto the stack. (The PUSH instruction is interpreted as a NOP by the Microcontroller.) |
| X + 1 (even) | JMP SUBR | The Microcontroller JMPs to the beginning of the subroutine. |
| X + 2 (odd) | (any instruction) | Main program execution resumes here after RETURN from subroutine. |
| • | • | |
| • | • | |
| • | • | |
| SUBR (any address) | (any instruction) | Execution of subroutine starts here. |
| • | • | |
| • | • | |
| • | • | |
| (any address) | MOVE R6,R6 | RETURN instruction causes ICC to transfer program back to X + 2. |

### Stack Operation

The LIFO stack holds up to four 13-bit program addresses which allows the ICC to return from a subroutine or interrupt service routine. When all four stack locations are filled, the STack Full (STF) output pin is driven high and remains high until a RETURN (or reset) operation occurs. If an additional interrupt is serviced or subroutine called while the stack is full, the stack will overflow and the oldest return address will be overwritten and lost. That is, the stack retains the four most recent entries. After an overflow, the status of the STF output is not valid (until a reset operation occurs).

To prevent an interrupt from overflowing the stack, the user can connect the STF output directly to the Interrupt Disable (ID) input of the ICC. Then, even if the internal mask and priorities permit interrupt servicing, the interrupt request must still wait for the most recent service routine or subroutine to return.

Because subroutine calling is controlled explicitly by the user software, the user can always ensure that subroutine nesting alone could not overflow the stack. However, care must be taken whenever calling a subroutine from within an interrupt service routine since the number of remaining stack locations may vary at the time the interrupt is taken. If, for example, three stack locations are already filled (STF is low) at the time an interrupt is serviced, then a subroutine call executed within the interrupt service routine would cause the stack to overflow and the earliest return address to be lost.

As mentioned earlier, whenever a RETURN operation is performed from an interrupt service routine, the internal interrupt mask is automatically cleared. A RETURN from a subroutine, however, does not affect the status of the mask. To accomplish this, a flag bit is added to each of the four stack locations which records whether each address pushed into the stack is caused by an interrupt or a subroutine call. This flag is read during a RETURN operation to determine whether or not the interrupt mask is cleared. This allows interrupt servicing and subroutine calls to be intermixed in any order.

### Initialization

The ICC decodes address zero as a reset command to perform certain initialization functions. (Zero is the first address generated after the Microcontroller is reset.) Specifically, the instruction-bus drivers are placed in a high-impedance state, HALT output is set high, RD output is set low, and all interrupt request latches are cleared. The interrupt mask is set so that any initialization routine by the user will not be interrupted until a CLEAR MASK instruction (MOVE R4,R4) is executed. The LIFO stack is reset to an empty state and the STF output is set Low.

## SYSTEM TIMING RELATIONSHIPS

### Interrupt Servicing

Interrupt servicing begins at the end of the Microcontroller instruction cycle when the 8X305's MCLK signal goes from Low-to-High. Starting from this point, processing of the interrupt proceeds as follows:

From the rising edge of MCLK 1:

- Interrupt mask is set to inhibit other interrupts.
- HALT output is driven low to stop internal operation of the 8X305 Microcontroller for one instruction cycle; MCLK is unaffected. ROM Disable (RD) output is driven high to disable program memory.

From the falling edge of MCLK 1:

- Takes address of next instruction from address bus and pushes it onto the top of stack to be used as the return address to the main program.

From the rising edge of MCLK 2:

- The ICC forces a JMP onto the instruction bus to one of three fixed vector addresses:

| | |
|---|---|
| INT 0 | Address 4 |
| INT 1 | Address 5 |
| INT 2 | Address 6 |

- Releases HALT (High) which allows the Microcontroller to complete the JMP to the above specified vector location in program memory.

From the rising edge of MCLK 3:

- Instruction-bus drivers of the ICC are disabled.
- ROM Disable (RD) pin is cleared (Low) enabling the program memory which resumes control of the instruction bus.

### Return Operation

When the interrupt service routine or subroutine is completed, the RETURN instruction initiates the following sequence of events:

From the rising edge of MCLK 1:

- Interrupts are temporarily inhibited through third MCLK cycle.
- HALT output is driven low to stop Microcontroller for one instruction cycle.
- RD output is set high to disable program memory.

From the rising edge of MCLK 2:

- HALT output is driven high (cleared).
- A JMP instruction to address stored at top of LIFO stack is forced onto the instruction bus by the ICC. (The stack is popped.)

From the rising edge of MCLK 3:

- Instruction-bus drivers of the ICC are disabled.
- RD is cleared enabling the program memory.
- If returning from an interrupt service routine (condition recorded in extra stack bit) the interrupt mask is cleared; otherwise the mask remains unaffected.

Once the preceding return actions are completed, the 8X305 Microcontroller will resume execution of the instruction at the return address.

## APPLICATION HINTS

- When programming an interrupt service routine or subroutine, certain system operations typically need to be considered. In many interrupt-driven systems, a handshake signal is required to acknowledge the servicing of an interrupt request. The acknowledge signal may be transmitted by the interrupt service routine using a standard I/O port from the 8X300 Family.
- If the user wants to allow a higher priority interrupt request to interrupt a service routine, then the CLEAR MASK instruction should be programmed (perhaps after completing any critical operations).
- For both service routines and subroutines, the user may need to save the contents of some or all of the working registers of the Microcontroller so that operation of the main program is not upset. Registers may be written out to a working storage RAM such as 8X350 near the beginning of the routine, and restored from RAM just before returning to the main program.
- Certain subroutine calling techniques may be used to increase the efficiency of the user program. As shown in the following examples, a subroutine can automatically be repeated two, three or four times, if desired, without programming a loop.

| SUBROUTINE AUTOMATICALLY EXECUTES TWICE | | | |
|---|---|---|---|
| **Address** | | | **Instruction** |
| X(even) | SUBR2 | MOVE R3,R3 | Push X + 1 onto stack. |
| X + 1(odd) | | (start of subroutine) | |
| • | | • | |
| • | | • | |
| | | MOVE R6,R6 | RETURN—First time jumps to X+1; second time jumps back to main program. |
| **SUBROUTINE AUTOMATICALLY EXECUTES THREE TIMES** | | | |
| X(odd) | SUBR3 | MOVE R3,R3 | Push X + 2 onto stack. |
| X + 1(even) | | MOVE R3,R3 | Push X + 2 onto stack. |
| X + 2(odd) | | (start of subroutine) | |
| • | | • | |
| • | | • | |
| **SUBROUTINE AUTOMATICALLY EXECUTES FOUR TIMES** | | | |
| X(even) | SUBR4 | MOVE R3,R3 | Push X + 1 onto stack. |
| X + 1(odd) | | MOVE R3,R3 | Push X + 3 onto stack. |
| X + 2(even) | | NOP | |
| X + 3(odd) | | (start of subroutine) | |
| • | | • | |
| • | | • | |

- In a manner similar to the Microcontroller multi–way branch technique, one of several subroutines can be selected according to an index value.

| SUBROUTINE CALL SELECTED BY VALUE IN R1 | | | |
|---|---|---|---|
| **Address** | | | **Instruction** |
| X(ODD) | | MOVE R3,R3 | Push X + 2 onto stack. |
| X + 1(even) | | XEC TABLE(R1) | Execute JMP at TABLE + (R1) |
| X + 2(odd) | | (any) | Subroutine returns here. |
| • | | • | |
| • | | • | |
| (any) | TABLE | JMP SUB0 | Call SUB0 if R1 = 0. |
| | | JMP SUB1 | Call SUB1 if R1 = 1. |
| | | • | |
| | | • | |

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +7 | $V_{DC}$ |
| $V_I$ | Input voltage | +5.5 | $V_{DC}$ |
| $V_O$ | Off–state output voltage | +5.5 | $V_{DC}$ |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq +125°C$

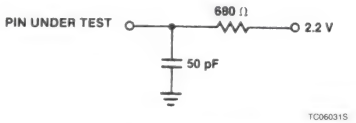
| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | High level input voltage | | 2.0 | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.8 | V |
| $V_{OH}$ | High level output voltage | $V_{CC}$ = MIN.; $I_{OH} = -1.0mA$ | 2.5 | | | V |
| $V_{OL}$ | Low level output voltage | $V_{CC}$ = MIN.; $I_{OL} = 2.5mA$ | | | 0.4 | V |
| $V_{IK}$ | Input clamp–diode voltage | $V_{CC}$ = MIN.; $I_{IL} = -18mA$ | | | –1.5 | V |
| $I_{IH}$ | High level input current | $V_{CC}$ = MAX; $V_{IH} = 2.7V$ | | | 100 | µA |
| $I_{IL}$ | Low level input current | $V_{CC}$ = MAX; $V_{IL} = 0.4V$ | | | –700 | µA |
| $I_{OS}$ | Short circuit output current | $V_{CC}$ = MAX.; $V_O = 0V$ | –15 | | –100 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX.; $I_0 - I_{15}$ = Hi–Z | | | | mA |
| | | $T_A = 25°C$ | | | 205 | |
| | | $T_A = -55°C$[2] | | | 230 | |
| | | $T_C = 125°C$ | | | 170 | |

## AC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq +125°C$

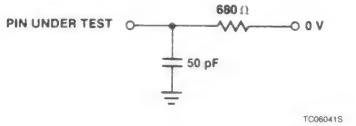
| SYMBOL | PARAMETER | REFERENCES | | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | From | To | | Min | Typ | Max | |
| **Pulse Widths:** | | | | | | | | |
| $t_{WIH}$ | Interrupt High | $\uparrow INT_i$ | $\downarrow INT_i$ | | 30 | | | ns |
| $t_{WIL}$ | Interrupt Low | $\downarrow INT_i$ | $\uparrow INT_i$ | | 35 | | | ns |
| $t_{WMH}$ | MCLK High | $\uparrow$MCLK | $\downarrow$MCLK | For all Functions | 47 | | | ns |
| **Propagation Delays:** | | | | | | | | |
| $t_{PRH}$ | RD High | $\uparrow$MCLK | $\uparrow$RD | Interrupt or Return | | | 75 | ns |
| $t_{PRL}$ | RD Low | $\uparrow$MCLK | $\downarrow$RD | Interrupt or Return | | | 17 | ns |
| $t_{PHL}$ | HALT Low | $\uparrow$MCLK | $\downarrow$HALT | Interrupt or Return | | | 87 | ns |
| $t_{PHH}$ | HALT High | $\uparrow$MCLK | $\uparrow$HALT | Interrupt or Return | | | 75 | ns |
| $t_{PSH}$ | Stack full High | $\downarrow$MCLK | $\uparrow$STF | Interrupt or Subroutine Call | | | 105 | ns |
| $t_{PSL}$ | Stack full Low | $\downarrow$MCLK | $\downarrow$STF | Return or Reset | | | 115 | ns |
| **Setup Times:** | | | | | | | | |
| $t_{SIH}$ | Interrupt input setup[3] | $\uparrow INT_i$ | $\uparrow$MCLK | | 35 | | | ns |
| $t_{SA}$ | Address setup | $A_0 - A_{13}$ | $\uparrow$MCLK | Interrupt, Subroutine, Call, or Reset | 0 | | | ns |
| $t_{SC}$ | Instruction setup[5] | $I_{0-15}$ | $\downarrow$MCLK | All Commands | Note 5 | | | ns |
| $t_{SD}$ | Interrupt disable setup[3] | ID | $\uparrow$MCLK | | 30 | | | ns |
| **Hold and Reset Recovery Times:** | | | | | | | | |
| $t_{HIL}$ | Interrupt low input hold[3] | $\uparrow$MCLK | $\uparrow INT_i$ | | | | 15 | ns |
| $t_{HA}$ | Address hold | $\downarrow$MCLK | $A_{0-13}$ | Subroutine Call or Reset | | | 90 | ns |
| $t_{HC}$ | Instruction hold | $\downarrow$MCLK | $I_{0-15}$ | All Commands | | | 55 | ns |
| $t_{HD}$ | Interrupt disable hold[3] | $\uparrow$MCLK | ID | | | | 25 | ns |
| $t_{RI}$ | Interrupt reset recovery[4] | $\downarrow$MCLK | $\uparrow INT_i$ | Reset or Cancel Command | 70 | | | ns |
| **Output Enable/Disable Delays:** | | | | | | | | |
| $t_{OEC}$ | Instruction output enable | $\uparrow$MCLK | $I_{0-15}$ | Interrupt or Return | | | 87 | ns |
| $t_{ODC}$ | Instruction output disable | $\uparrow$MCLK | $I_{0-15}$ | Interrupt or Return | | | 47 | ns |

**NOTES:**
1. All electrical characteristics re guaranteed after power is applied and thermal equilibrium has been reached.
2. The 230mA value is worst case over the entire temperature range.
3. Parameters $t_{SIH}$, $t_{HIL}$, $t_{SD}$, and $t_{HD}$ are used only to determine whether an interrupt request will be serviced during the current or a subsequent instruction cycle. the $INT_i$ and ID inputs are asynchronous and transitions on either input may safely occur at any time with respect to MCLK. A low–to–high transition on $INT_i$ occurring after $t_{SIH}$ and before $t_{HIL}$ means only that it cannot be determined for sure whether or not the interrupt request will be honored during the current instruction cycle. Similarly, transitions on ID between $t_{SD}$ and $t_{HD}$ make it uncertain as to whether or not masking applies during the current instruction cycle.
4. When clearing interrupt requests (including a reset operation), any new low–to–high transitions appearing at the $INT_i$ inputs that occur before $t_{RI}$ risk being cleared and therefore ignored; however, any transition after $t_{RI}$ is certain to be latched.
5. $t_{SC}$ (minimum) = 17ns — $t_{PRL}$ (actual).
(The required instruction enable time for the program memory depends on the sum of the $t_{PRL}$ and $t_{SC}$.)

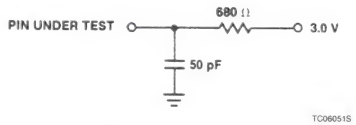
## AC TEST CIRCUITS




RD, STF, and $\overline{\text{HALT}}$ Outputs



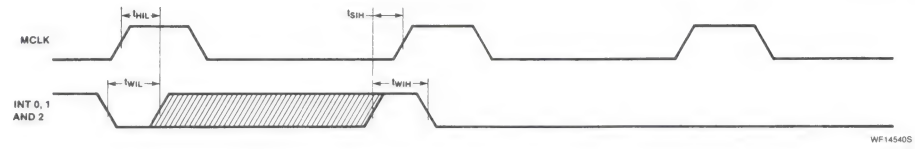

$I_0 - I_{15}$ Outputs ($t_{OEC}$ and $t_{ODC}$) $t_{PZH}$ and $t_{PHZ}$



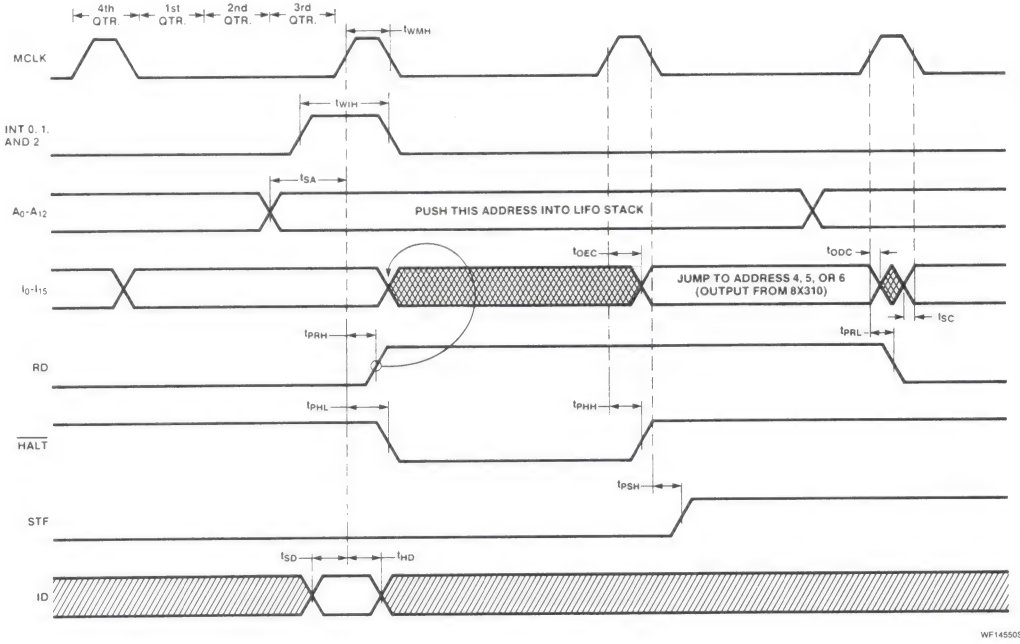

$t_{PZL}$ and $t_{PLZ}$

**NOTES:**
1. $V_M = 1.5V$ for all input signals and RD, STF, and HALT outputs.
2. For $I_0 - I_{15}$ ($t_{OEC}$): $V_M = 1.5V$
   For $I_0 - I_{15}$ ($t_{ODC}$): $V_M$ ($t_{PLZ}$) = $V_{OL} + 0.5V$
   $V_M$ ($t_{PHZ}$) = $V_{OH} - 0.5V$

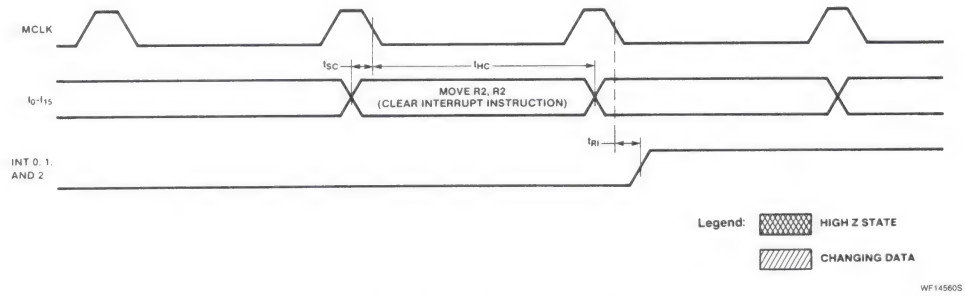
## TIMING DIAGRAMS




Interrupt Request Timing

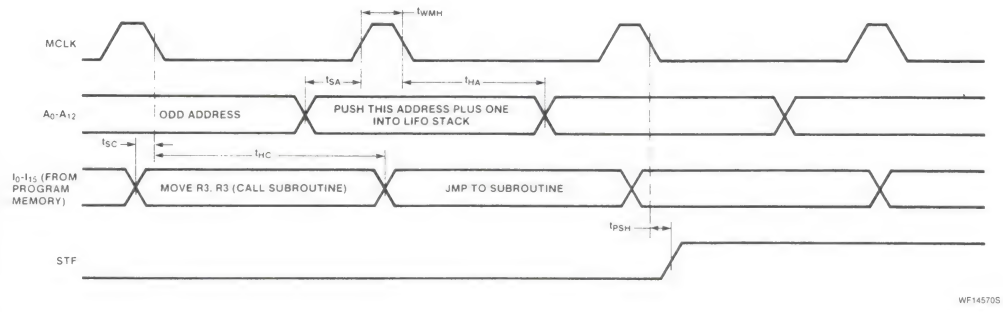



Interrupt Service Timing

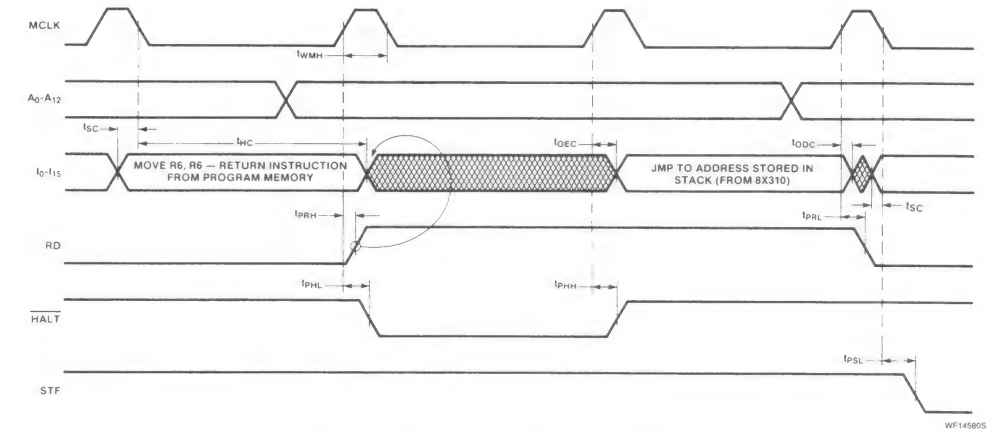



Clear Interrupt Instruction Timing

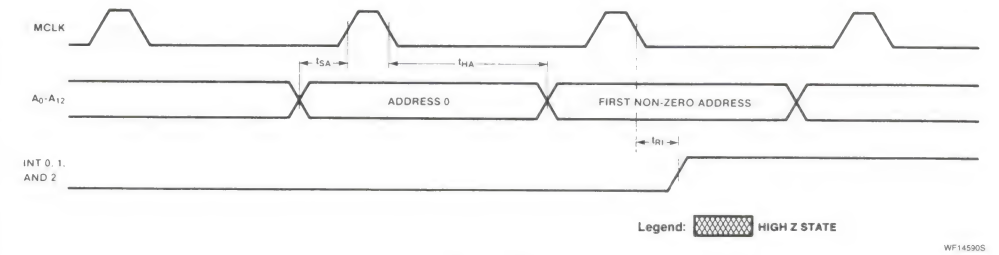
## TIMING DIAGRAMS (Continued)




Call Subroutine Timing




Return Timing (From Interrupt or Subroutine)




Reset Timing

Signetics

# 8X320
## Bus Interface Register Array

***Product Specification***

**Military**
**Customer Specific Products**

### FEATURES

- **16-byte/2-port interface**
- **8- or 16-bit primary port (Host) interface (User selectable)**
- **8-bit secondary port interface**
- **Two 8-bit flag registers (handshake control)**
- **DMA or programmed I/O operation**
- **Two 3-State bidirectional ports**
- **Secondary port is bus compatible with 8X305**
- **Single 5V supply**
- **0.6", 40-pin package**

### ARCHITECTURAL OVERVIEW

The Signetics 8X320 Bus Interface Register Array (Figure 1) is a dual-port RAM memory designed for use between a host processor and a peripheral processor. Specifically, the register array provides a convenient and economical interface between the 8X305 Microcontroller (secondary port) and User's Host System (primary port); the host can be almost any bus-oriented device — another processor, a minicomputer, or a mainframe computer. The host has 8-bit (byte) or 16-bit (word) access to the primary port; data can be read-from or written-into any memory location as determined by the primary-port address and control lines. The secondary port (8X305 bus) consists of eight input/output lines and four bus control lines. To implement the secondary-port interface, an 8-bit memory location is addressed during one machine cycle and, during another cycle, data is read or written under control of the secondary (8X305) processor. Both primary and secondary ports feature 3-State outputs and both ports are bidirectional.

### BLOCK DIAGRAM

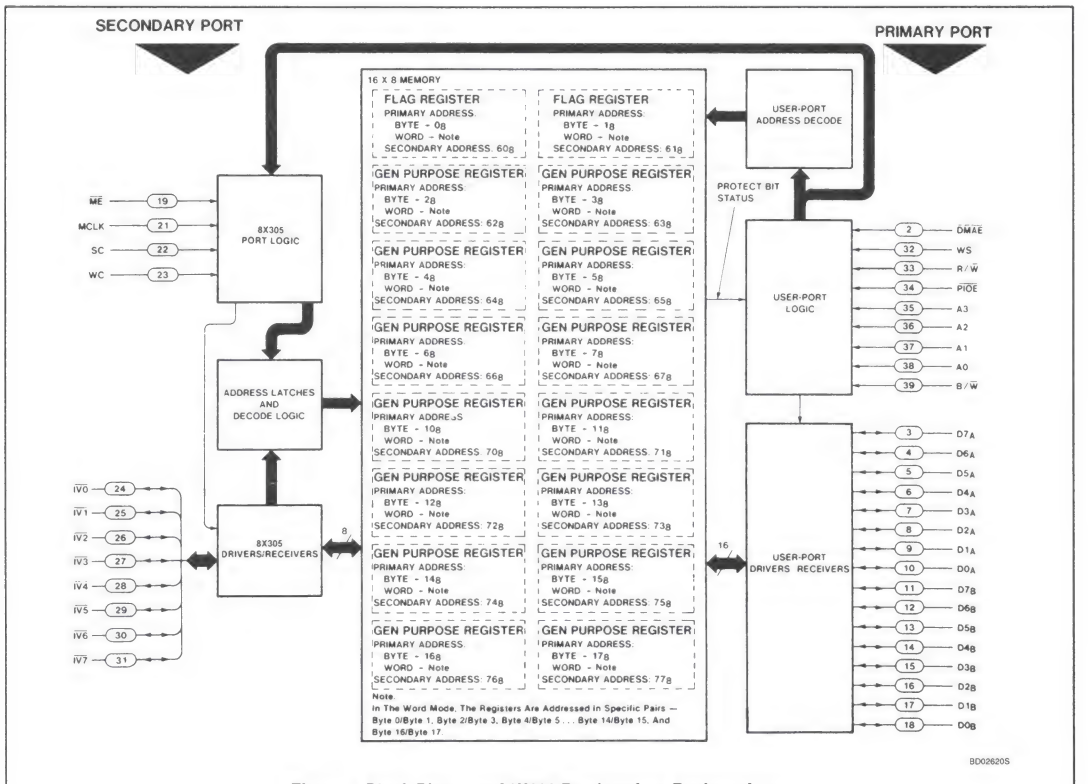
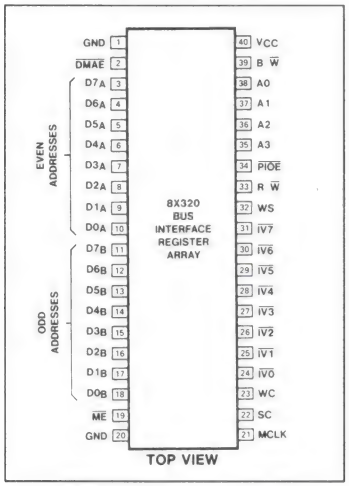



**Figure 1. Block Diagram of 8X320 Bus Interface Register Array**

# Bus Interface Register Array | 8X320

## PIN CONFIGURATION




## ORDERING INFORMATION

| PACKAGE | ORDER CODE |
|---|---|
| 40-Pin DIP | 8X320/BQA |

Besides the convenience and economy of a two-port memory, the array also provides simple handshake control via two 8-bit flag registers, logic to facilitate DMA transfers, and a write-protect feature for the primary port in both byte and word modes of operation.

## PIN DESCRIPTION

| PIN NO. | IDENTIFIER | FUNCTION |
|---|---|---|
| 1, 20 | GND | **Ground:** Circuit ground. |
| 2 | $\overline{DMAE}$ | **Direct Memory Access Enable:** Enables primary port to facilitate DMA transfers; does not affect secondary port. |
| 3 – 18 | $D0_A - D7_A$/ $D0_B - D7_B$ | **Primary Data Port:** Sixteen 3-State lines used for data transfers to-and-from the primary data port; most significant bit is $D0_B$ and least significant bit is $D7_A$. |
| 19 | $\overline{ME}$ | **Master Enable:** Enables secondary port when active low ($\overline{ME}$). |
| 21 | MCLK | **Master Clock:** When MCLK is high, and 8X320 is enabled ($\overline{ME}$ = Low), a register location may be either selected or written-into under control of SC and WC. |
| 22 | SC | **Select Command:** With SC high, WC low, MCLK high and $\overline{ME}$ low, data on $\overline{IV0}$ through $\overline{IV7}$ is interpreted as an address. If any one of the 16 register addresses ($60_B - 77_B$) matches that on the I/O (IV) bus, that particular register is selected and remains selected until another address on the same bank (i.e. $\overline{ME}$ = low) is output on the I/O bus — at which time, the old register is deselected and a new register may or may not be selected. |
| 23 | WC | **Write Command:** With WC high, SC low, MCLK high, and $\overline{ME}$ low, the selected register stores contents of $\overline{IV0} - \overline{IV7}$ as data. |
| 24 – 31 | $\overline{IV0} - \overline{IV7}$ | **Secondary Data Port:** Eight 3-State lines used to transfer data or I/O address to-and-from the secondary data port; most significant bit is $\overline{IV0}$ and least significant bit is $\overline{IV7}$. |
| 32 | WS | **Write Strobe:** When active high, data appearing at the primary port ($D0_A$ - $D7_A$/$D0_B$ - $D7_B$) is stored in the register array if the primary port is in the *write* mode. |
| 33 | R/$\overline{W}$ | **Read/Write Control:** When this signal is high, primary port is in *read* mode; when signal is low, primary port is in *write* mode. |
| 34 | $\overline{PIOE}$ | **Programmed I/O Enable:** When active low, primary port operates in programmed input/output mode with register to be read-from or written-into selected by A0 – A3. |
| 35–38 | A0 –A3 | **Primary Port Address Select:** Select register or register-pair that primary port is read-from or write-into. Most significant bit is A3; least significant bit is A0. |
| 39 | B/$\overline{W}$ | **Byte/Word:** When signal is high, the primary port operates in the byte (8-bit) mode; when signal is low, the primary port operates in the word (16-bit) mode. |
| 40 | $V_{CC}$ | **Power:** +5V. |

**NOTE:**
All barred symbols ($\overline{DMAE}$, etc.) denote signals that are asserted (or active) when low (logical 0); signals that are not barred are asserted in the high state (logical 1).

## OPERATING CHARACTERISTICS

### Memory Organization

Memory and address correlation for the 16-register array is shown in Figure 2. From the primary port, the sixteen 8-bit registers can be addressed in either (8-bit) or word (16-bit) format; in the word mode, the registers are addressed in pairs — $0_8/1_8$, $2_8/3_8$, $4_8/5_8$,... $14_8/15_8$, and $16_8/17_8$. From the secondary port, all registers are addressed in byte format — $60_8$ through $77_8$. The memory consists of two 8-bit flag registers and fourteen 8-bit general-purpose registers. The flag registers facilitate information transfers between the two ports and, in addition, they protect certain registers from being written into from the primary port.

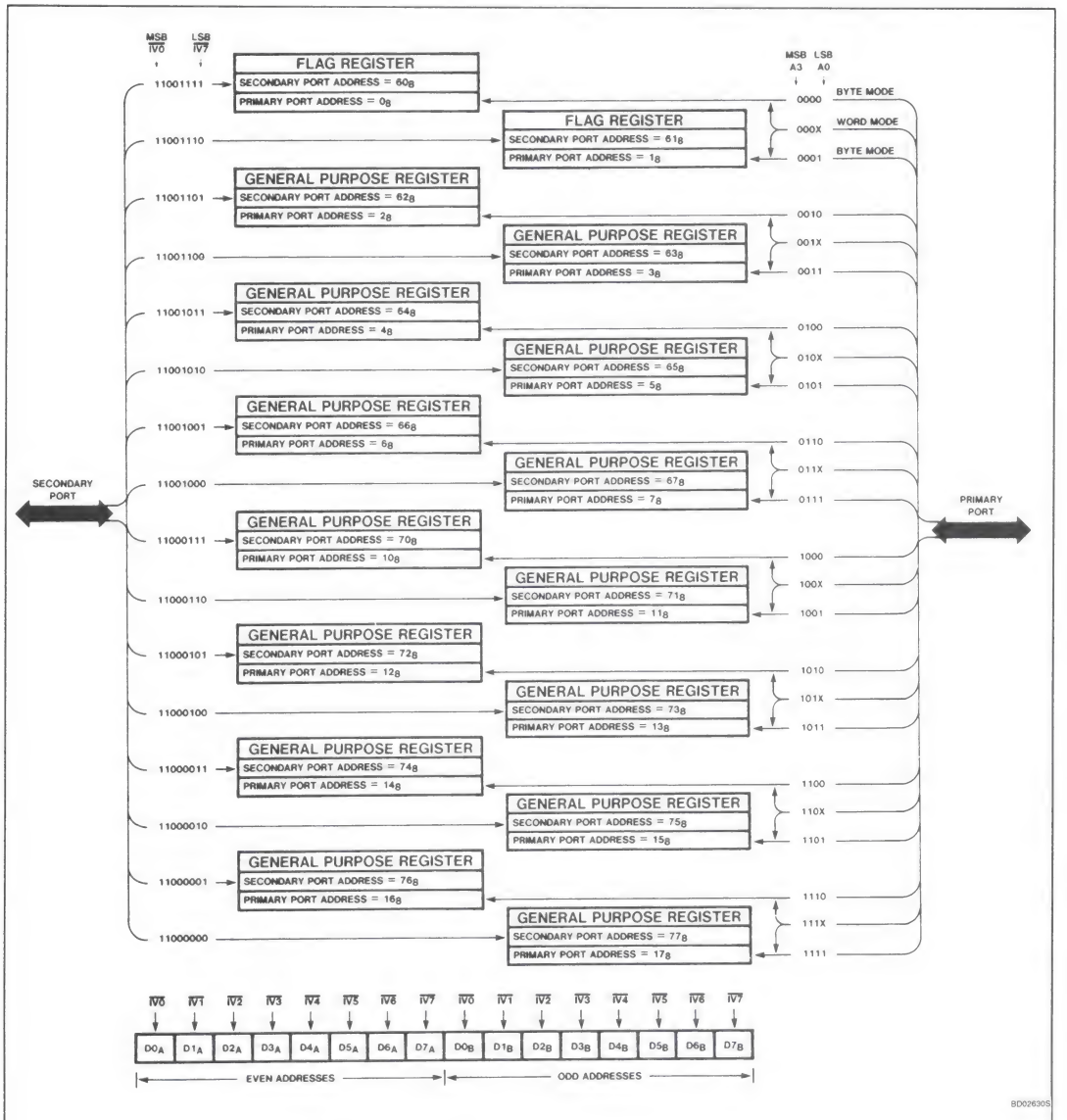
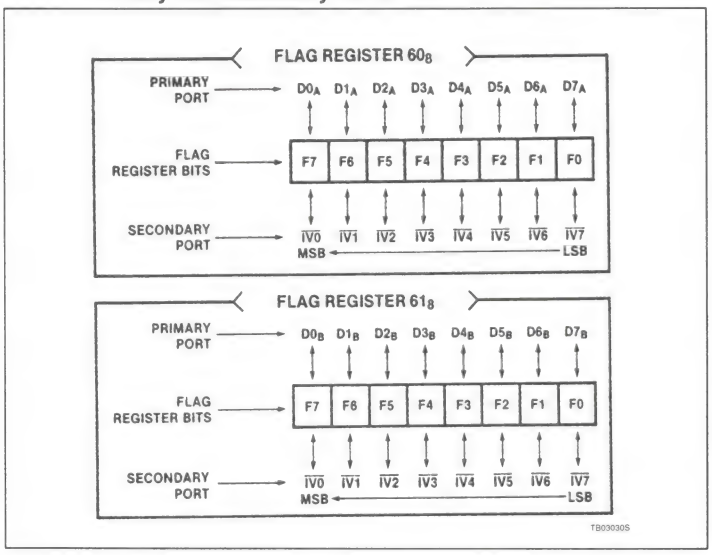



**Figure 2. Memory and Address Organization for the 8X320**

### Table 1. Control Of The Two Flag Register

| FLAG REGISTERS | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $60_8$ ($0_8$) | F2 | F3 | F4 | F5 | F6 | F7 | | | | | | | | |
| | $61_8$ ($1_8$) | | | | | | | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 |
| OCTAL ADDRESS OF CONTROLLING BYTE | Primary | 2 | 3 | 4 | 5 | 6 | 7 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
| | Secondary | 62 | 63 | 64 | 65 | 66 | 67 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 |

### Table 2. Relationship Between Flag Register Bits And Those Of Primary And Secondary Ports




### Table 3. Mode Control Of Primary Port

| MODE | PIOE | DMAE |
|---|---|---|
| Disabled (output) | 1 | 1 |
| Programmed I/O | 0 | 1 |
| DMA | X | 0 |

**NOTE:**
X = Don't Care

### Table 4. Primary Port Operating In Programmed I/O Mode

| MODE | B/W | A0 | $D0_A - D7_A$ (EVEN ADDRESSES) | $D0_B - D7_B$ (ODD ADDRESSES) |
|---|---|---|---|---|
| Read | 0 (Word) | X | Stored Data | Stored Data |
| Read | 1 (Byte) | 0 | Stored Data | Hi-Z |
| Read | 1 (Byte) | 1 | Hi-Z | Stored Data |
| Write | 0 (Word) | X | Write | Write |
| Write | 1 (Byte) | 0 | Write | No Change |
| Write | 1 (Byte) | 1 | No Change | Write |

**NOTE:**
X = Don't Care

In either byte or word mode, the write-protect logic, implemented by bits F0 and F1 of register $60_8$, inhibits the primary port from writing into addresses $16_8$ and $17_8$, respectively. Both write-protect bits (F0 and F1) can be read or written from the secondary port; the bits are read-only from the primary port.

As shown in Table 1, flag bits F2 through F7 of $60_8$ and F0 through F7 of $61_8$ are controlled by the fourteen general-purpose registers. When any one of these registers is written into by either port, the corresponding flag bit for that register is automatically set by internal logic of the 8X320. When information is read from any register, the corresponding flag bit must be reset by user software Except for the write-protect bits, all other flag bits can be read or reset from the primary or the secondary port.

Table 2 shows the relationship between bits of the flag registers and bits of the primary and secondary ports.

## FUNCTION AND CONTROL OF PRIMARY PORT

The primary port provides an 8-bit (byte) or 16-bit (word) interface between the 16-byte memory and the user's host system. If the host is an 8-bit system (or 16-bit system operating in Byte mode), the sixteen bidirectional I/O lines must be tied together ($D0_A$ to $D0_B$, $D1_A$ to $D1_B$, ... and $D7_A$ to $D7_B$); when data is input or output on $D0_A$ to $D7_A$, the remaining eight lines ($D0_B$ through $D7_B$) are Hi-Z and vice-versa.

Other than the Byte/$\overline{\text{Word}}$ control line, specific operating characteristics of the primary port are controlled by two signals — $\overline{\text{PIOE}}$ (Programmed I/O Enable) and $\overline{\text{DMAE}}$ (Direct Memory Access Enable). When $\overline{\text{PIOE}}$ is active (low) and $\overline{\text{DMAE}}$ is inactive (high), the primary port operates in the programmed I/O mode — refer to table 3; in this mode of operation, the register to be read-from or written-into is determined by four address lines (A0 through A3) and the Byte/$\overline{\text{Word}}$ control line — see Figure 2 and Table 4. In the DMA mode of operation, A1, A2, and A3 are not used; data is read-from or written-into preassigned registers: bytes $16_8$ ($76_8$) and $17_8$ ($yy_8$) for the byte mode of operation and bytes $14_8$ ($74_8$)/$15_8$ ($75_8$) and $16_8$ ($76_8$)/$17_8$ ($77_8$) for the word mode of operation. In both cases, switching between bytes $16_8$ and $17_8$ in the byte mode and $14_8/15_8$ and $16_8/17_8$ in the word mode is controlled by A0 (the least significant address bit). Refer to Table 5.

Table 4 defines programmed I/O operation of the primary port in terms of read/$\overline{write}$ functions and Byte/$\overline{Word}$ control. In the byte mode, data is read-from or written-into the even addresses ($p_8$, $2_8$, $4_8$, $6_8$, $10_8$, $12_8$, $14_8$, and $16_8$) via data lines $D0_A$ through $D7_A$; data is read-from or written-into odd addresses ($1_8$, $3_8$, $5_8$, $7_8$, $11_8$, $13_8$, $15_8$, and $17_8$) via data lines $D0_B$ through $D7_B$. When A0 is low (logical 0), even addresses are selected and when A0 is high (logical 1), odd addresses are selected; thus, A0 is the LSB of a 4-bit address. In the word mode, the state of A0 is irrelevant, since both the odd and even bytes are, simultaneously, read-from or written-into; thus, a register pair is selected by a 3-bit address, A1 being the LSB.

In the DMA mode of operation with $\overline{DMAE}$ set to 0 and other conditions satisfied, data is directly transferred to-or-from specified memory locations under control of Byte/$\overline{Word}$, R/$\overline{W}$, and A0. The state of the Byte/$\overline{Word}$ control line determines whether the data word is 8 bits or 16 bits. The A0 address line correlates eight of the sixteen data lines ($D0_A$ - $D7_A$ or $D0_B$ - $D7_B$) with the proper byte/word location. Thus, in the word mode, the exchange of data between the memory and the primary port occurs via $D0_A$ – $D7_A$ for bytes $14_8$ and $16_8$ and via $D0_B$ – $D7_B$ for bytes $15_8$ and $17_8$. The byte mode of operation is similar, except that the unused eight lines are 3-Stated.

**Table 5. DMA Operation Of The Primary Port**

| MODE | BYTE/WORD | A0 | $D0_A$ – $D7_A$ | $D0_B$ – $D7_B$ |
|---|---|---|---|---|
| Read | 0 (Word) | 0 | Data stored in byte $14_8$ | Data stored in byte $15_8$ |
| Read | 0 (Word) | 1 | Data stored in byte $16_8$ | Data stored in byte $17_8$ |
| Read | 1 (Byte) | 0 | Data stored in byte $16_8$ | Hi-Z |
| Read | 1 (Byte) | 1 | Hi-Z | Data stored in byte $17_8$ |
| Write | 0 (Word) | 0 | Write to byte $14_8$ | Write to byte $15_8$ |
| Write | 0 (Word) | 1 | Write to byte $16_8$ | Write to byte $17_8$ |
| Write | 1 (Byte) | 0 | Write to byte $16_8$ | Hi-Z |
| Write | 1 (Byte) | 1 | Hi-Z | Write to byte $17_8$ |

## FUNCTION AND CONTROL OF SECONDARY PORT

The secondary port provides an 8-bit interface between the sixteen memory registers and the 8X305 (or other processor). As shown in Table 6, the secondary-port interface is controlled by five input signals and a status latch. The status latch is set when SC is high (MCLK high/$\overline{ME}$ low) and a valid memory address ($60_8$ – $77_8$) is presented to the 8X320 via the secondary data port ($\overline{IV0}$/$\overline{IV7}$). The latch is cleared by internal logic when an invalid memory address is presented at the secondary port. In all read/write operations from the secondary port, the status latch acts like a master enable; data can be transferred only if the status latch is set.

**Table 6. Functional Control of Secondary Port**

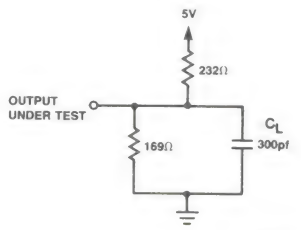
| $\overline{ME}$ | SC[1] | WC[1] | MCLK | R/$\overline{W}$ | STATUS LATCH | FUNCTION OF SECONDARY BUS |
|---|---|---|---|---|---|---|
| L | L | L | X | X | Set | Output data from 8X320 memory to 8X305. |
| L | L | H | H | H | Set | Data from 8X305 is input and written-into a previously-selected memory location of the 8X320 (Note 2). |
| L | L | H | H | L | Set | With the primary port in the write mode (R/$\overline{W}$ = 0), the secondary port is overridden and cannot write to the same register addressed by the primary port; however, the register addressed by the primary port can be read and any other register can be read-from or written-into from the secondary port (Note 2). |
| L | H | L | H | X | X | Data transmitted to the secondary port via the $\overline{IV}$ bus is interpreted as an address; if address is within range of $60_8$ - $77_8$ the memory status latch is subsequently set. |
| L | L | H | L | X | X | Inactive |
| L | H | L | L | X | X | Inactive |
| L | L | X | X | X | Not set | Inactive |
| H | X | X | X | X | X | Inactive |

**NOTES:**
1. The SC and WC lines should never both be high at the same time; the 8X305 processor never generates this condition.
2. During read or write operations, the same register can be simultaneously addressed from either port. For any write operation by both ports on the same register, the primary port has priority; other than this, the 8X320 does not indicate error conditions or resolve conflicts.
3. X = Don't Care.

## DC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V, -55°C \leq T_C \leq 125°C$

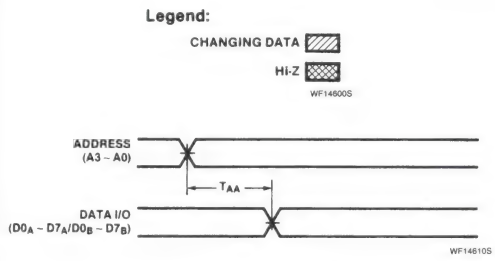
| SYMBOL | PARAMETER | TEST CONDITIONS[1, 2] | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | | 4.5 | 5 | 5.5 | V |
| $V_{IL}$ | Low level input voltage | | | | | 0.80 | V |
| $V_{IH}$ | High level input voltage | | | 2.0 | | | V |
| $V_{OL}$ | Low level output voltage | $V_{CC} = 4.5V; I_{OL} = 16mA$ | | | | 0.5 | V |
| $V_{OH}$ | High level output voltage | $V_{CC} = 4.5V; I_{OH} = -3mA$ | | 2.5 | | | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC} = 4.5V; I_I = -18mA$ | | | | -1.5 | V |
| $I_{CC}$ | Supply current | $V_{CC} = 5.5V$ | $T_A = 125°C$ | | | 210 | mA |
| | | | $T_A = 25°C$ | | | 260 | mA |
| | | | $T_A = -55°C$ | | | 300 | mA |
| $I_{OS}$ | Short circuit output current[3] | $V_{CC} = 5.5V$ | | -20 | | -100 | mA |
| $I_{IL}$ | WC, MCLK, SC, & $\overline{ME}$ | $V_{CC} = 5.5V; V_{IL} = 0.50V$ | | | | -1.0 | mA |
| $I_{IL}$ | B/$\overline{W}$ | $V_{CC} = 5.5V; V_{IL} = 0.50V$ | | | | -1.6 | mA |
| $I_{IL}$ | A0 – A3 | $V_{CC} = 5.5V; V_{IL} = 0.50V$ | | | | -1.0 | mA |
| $I_{IL}$ | $\overline{DMAE}$ | $V_{CC} = 5.5V; V_{IL} = 0.5V$ | | | | -800 | µA |
| $I_{IL}$ | WS, $\overline{PIOE}$, & R/$\overline{W}$ | $V_{CC} = 5.5V; V_{IL} = 0.5V$ | | | | -400 | µA |
| $I_{IL}$ | $\overline{IV0} - \overline{IV7}$ | $V_{CC} = 5.5V; V_{IL} - 0.5V$ | | | | -400 each line | µA |
| $I_{IL}$ | $D0_A - D7_A/D0_B - D7_B$ | $V_{CC} = 5.5V; V_{IL} = 0.5V$ | | | | -400 each line | µA |
| $I_{IH}$ | WC, SC, MCLK, & $\overline{ME}$ | $V_{CC} = 5.5V; V_{IH} = 5.5V$ | | | | 100 | µA |
| $I_{IH}$ | B/$\overline{W}$ | $V_{CC} = 5.5V; V_{IH} = 5.5V$ | | | | 240 | µA |
| $I_{IH}$ | A0 | $V_{CC} = 5.5V; V_{IH} = 5.5V$ | | | | 120 | µA |
| $I_{IH}$ | A1 – A3 | $V_{CC} = 5.5V; V_{IH} = 5.5V$ | | | | 60 | µA |
| $I_{IH}$ | $\overline{DMAE}$ | $V_{CC} = 5.5V; V_{IH} = 5.5V$ | | | | 120 | µA |
| $I_{IH}$ | WS, $\overline{PIOE}$, & R/$\overline{W}$ | $V_{CC} = 5.5V; V_{IH} = 5.5V$ | | | | 60 | µA |
| $I_{IH}$ | $\overline{IV0} - \overline{IV7}$ and $D0_A - D7_A/D0_B - D7_B$ | $V_{CC} = 5.5V; V_{IH} = 5.5V$ | | | | 100 | µA |

## AC TEST CIRCUIT

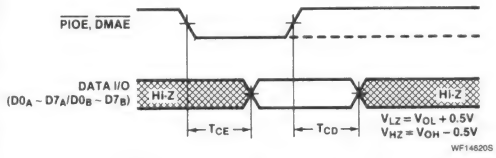



NOTE:
$C_L$ includes jig and probe capacitance.

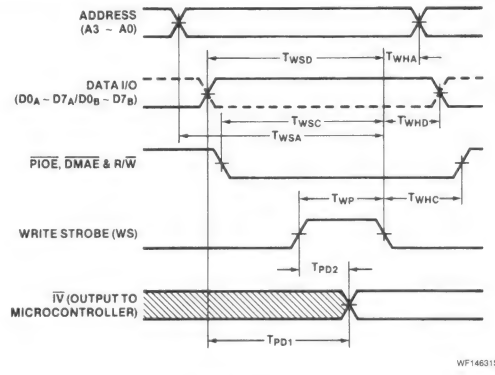
## AC CHARACTERISTICS OF PRIMARY PORT




Address Access Time




Primary Port Enable/Disable Times

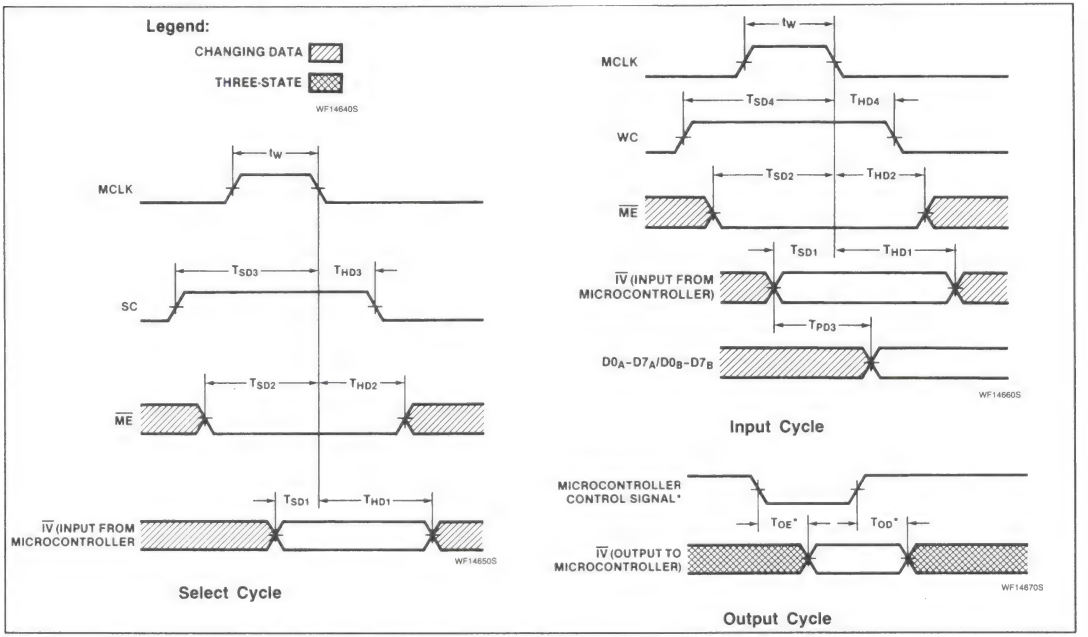



Write Cycle

## AC ELECTRICAL CHARACTERISTICS OF PRIMARY PORT $4.5V \leq V_{CC} \leq 5.5V, -55°C \leq T_C \leq 125°C$

| SYMBOL | PARAMETER | FROM | TO | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $T_{AA}$ | Address Access Time | A3 – A0 | $D0_A – D7_A/D0_B – D7_B$ | | | 65 | ns |
| $T_{CE}$ | Primary port enable time | ↓PIOE<br>↓DMAE | $D0_A – D7_A/D0_B – D7_B$ | | | 30 | ns |
| $T_{CD}$ | Primary port disable time | ↑PIOE<br>↑DMAE | $D0_A – D7_A/D0_B – D7_B$ | | | 35 | ns |
| $T_{WSA}$ | Address setup time | A3 – A0 | ↓WS | 60 | | | ns |
| $T_{WHA}$ | Address hold time | ↓WS | A3 – A0 | | | 0 | ns |
| $T_{WSD}$ | Primary port data setup time | $D0_A – D7_A/D0_B – D7_B$ | ↓WS | 30 | | | ns |
| $T_{WHD}$ | Primary port data hold time | ↓WS | $D0_A – D7_A/D0_B – D7_B$ | | | 5 | ns |
| $T_{WSC}$ | Write mode control setup time | PIOE<br>DMAE<br>R/W | ↓WS<br>↓WS<br>↓WS | 35<br>45<br>55 | | | ns<br>ns<br>ns |
| $T_{WHC}$ | Write mode control hold time | ↓WS | PIOE<br>DMAE<br>R/W | | | 15<br>10<br>10 | ns<br>nsns |
| $T_{WP}$ | Write strobe pulse width | | | 25 | | | ns |
| $T_{PD1}$[4] | Primary port data delay | $D0_A – D7_A/D0_B – D7_B$ | IV0 – IV7 | | | 90 | ns |
| $T_{PD2}$[5] | Primary port data delay from WS | ↑WS | IV0 – IV7 | | | 90 | ns |

## AC CHARACTERISTICS OF SECONDARY PORT




## AC ELECTRICAL CHARACTERISTICS $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_C \le 125°C$

| SYMBOL | PARAMETER[1] | FROM | TO | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $T_W$ | MCLK pulse width | | | 30 | | | ns |
| $T_{SD1}$ | Data setup time | $\overline{IV0} - \overline{IV7}$ | ↓MCLK | 35 | | | ns |
| $T_{SD2}$ | $\overline{ME}$ setup time | $\overline{ME}$ | ↓MCLK | 40 | | | ns |
| $T_{SD3}$ | SC setup time | SC | ↓MCLK | 40 | | | ns |
| $T_{SD4}$ | WC setup time | WC | ↓MCLK | 40 | | | ns |
| $T_{HD1}$ | Data hold time | ↓MCLK | $\overline{IV0} - \overline{IV7}$ | | | 5 | ns |
| $T_{HD2}$ | $\overline{ME}$ hold time | ↓MCLK | $\overline{ME}$ | | | 0 | ns |
| $T_{HD3}$ | SC hold time | ↓MCLK | SC | | | 0 | ns |
| $T_{HD4}$ | WC hold time | ↓MCLK | WC | | | 0 | ns |
| $T_{PD3}$[6] | $\overline{IV}$ propagation time | $\overline{IV}$ | $D0_A - D7_A/D0_B - D7_B$ | | | 65 | ns |
| $T_{OE}$ | Output enable | $\overline{ME}$, SC, or WC | $\overline{IV0} - \overline{IV7}$ | | | 30 | ns |
| $T_{OD}$ | Output disable | RME, SC, or WC | $\overline{IV0} - \overline{IV7}$ | | | 35 | ns |

**NOTE:**
1. Operating temperature ranges are guaranteed after terminal equilibrium has been reached.
2. All voltages are measured with respect to ground terminal.
3. Short only one output at a time.
4. Measurement with Write Strobe set High and the control signals of the secondary port set for output data from the same register.
5. Measurement with primary port data stable and control signals of secondary port set for output data from the same register.
6. Measured with MCLK = High and control signals of the primary port set for output data from the same register.

Signetics

# 8X371

## 8-Bit Latched Bidirectional I/O Port

***Product Specification***

**Military**
**Customer Specific Products**

### FEATURES

- **Two bidirectional 8-bit busses**
- **Independent bus operation (user-bus priority for data entry)**
- **User data input synchronous with respect to MCLK**
- **3-State TTL outputs with high-drive capabilities**
- **Power-up to predetermined logic state**
- **Directly compatible with 8X305**
- **Single +5V supply**
- **0.4", 24-pin DIP**

### FUNCTIONAL OPERATION

#### UD Bus Control

As shown in Table 1, the User Data (UD) bus interface is controlled by the $\overline{UIC}$ and $\overline{UOC}$ inputs. Data input to the UD bus is synchronous with MCLK, that is, with $\overline{UIC}$ Low, information is written into the data latches only when MCLK is High. Output drivers on the UD bus are enabled when $\overline{UOC}$ is Low and $\overline{UIC}$ is High.

### PRODUCT DESCRIPTION

The 8X371 I/O Port is a bidirectional device designed for use as an interface element in systems that use TTL-compatible busses. Typically, the 8X371 is used with the 8X305 Microcontroller and its associated Interface Vector ($\overline{IV}$) bus; however, it can also be used with an equivalent microprocessor. As shown in the logic diagram of Figure 1, the 8X371 consists of eight identical data latches — bits 0 through 7. The latches are accessed from either of two 8-bit busses — the Microcontroller ($\overline{IV}$ bus) and the user data (UD bus). Separate controls are provided for each bus and both busses operate independently, except when both attempt to input data at the same time; in such situations, the user bus always has priority. A Master Enable ($\overline{ME}$) input is available for additional control over the $\overline{IV}$ bus. The data latches are transparent, in that, while either bus is enabled for input, all input-data transitions are propagated to the other bus, if enabled for output.

**Table 1. Input/Output Control Of UD Bus**

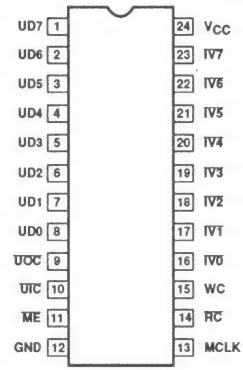
| $\overline{UIC}$ | $\overline{UOC}$ | MCLK | FUNCTION OF UD BUS |
|---|---|---|---|
| H | L | X | Output data |
| L | X | H | Input data |
| L | X | L | Inactive |
| H | H | X | Inactive |

**NOTE:**
X = don't care

### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 24–Pin DIP | 8X371/BXA |

### PIN CONFIGURATION




| PIN NO. | IDENTIFIER | FUNCTION |
|---|---|---|
| 1–8 | UD7–UD0 | 3–State, bidirectional User Data (UD) bus; UD0 and corresponds to $\overline{IV0}$. |
| 9 | $\overline{UOC}$ | User Output Control – active low input to enable data output to UD0 – UD7. |
| 10 | $\overline{UIC}$ | User Input Control – active low input to enable data input from UD0 – UD7. |
| 11 | $\overline{ME}$ | Master Enable – active low input to enable the $\overline{IV}$ bus for data input, or data output; UD–bus operations are unaffected. |
| 12 | GND | Ground. |
| 13 | MCLK | Master Clock – active high input (from Microcontroller used to strobe data into data latches from the $\overline{IV}$ and UD buses. |
| 14 | $\overline{RC}$ | Read Control – active low input to enable data output to $\overline{IV0}$ – $\overline{IV7}$. |
| 15 | WC | Write Command – active high input (from Micontroller) to enable the writing of data into the data latches from the $\overline{IV}$ bus (provided $\overline{UIC}$ is not low). |
| 16–23 | $\overline{IV0}$–$\overline{IV7}$ | Interface Vector (Input/Output Bus) – 3–State, bidirectional, Microcontroller data bus; $\overline{IV0}$ corresponds to UD0. |
| 24 | $V_{CC}$ | +5V power supply. |

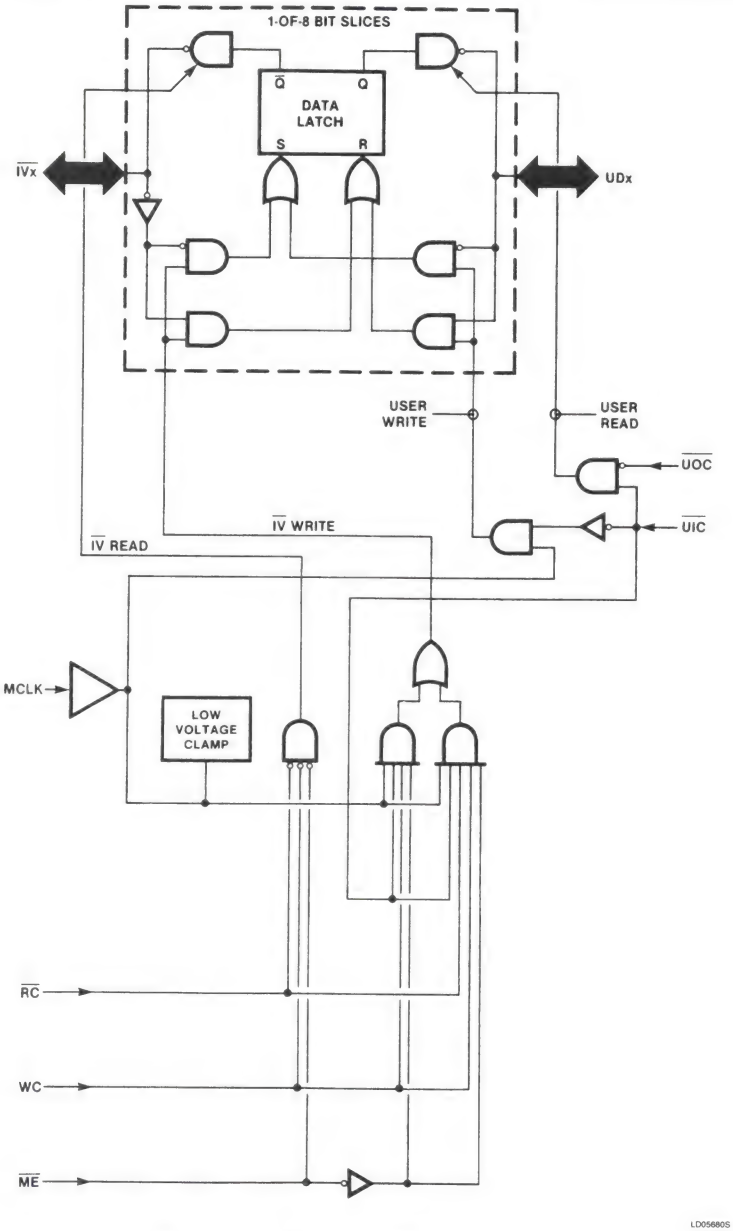



Figure 1. Logic Diagram for 8X371 I/O Port

# 8-Bit Latched Bidirectional I/O Port — 8X371

## $\overline{IV}$ Bus Control

Input/output control of the $\overline{IV}$ bus is shown in Table 2; this bus is controlled by $\overline{RC}$, WC, $\overline{ME}$, and MCLK. The $\overline{IV}$ bus is enabled for output (Microcontroller read operation) when $\overline{ME}$, $\overline{RC}$, and WC are all low. Data is written into the data latches from the $\overline{IV}$ bus when $\overline{ME}$ is low and both WC and MCLK are high. To avoid data-input conflicts, inputs from the $\overline{IV}$ bus are inhibited when $\overline{UIC}$ is low; under all other conditions, the $\overline{IV}$ and UD busses operate independently. The Microcontroller Left Bank ($\overline{LB}$) and Right Bank ($\overline{RB}$) outputs can control the $\overline{ME}$ inputs for two banks of I/O devices, thus acting as a ninth address bit. If more than one I/O Port (including the addressable parts — 8X372, 8X376, 8X382, etc.) are to be connected to the same bank ($\overline{LB}$ or $\overline{RB}$) of the Microcontroller, selection of each 8X371 must be accomplished with external logic to avoid bus conflicts.

**Table 2. Input/Output Control Of $\overline{IV}$ Bus**

| $\overline{ME}$ | $\overline{RC}$ | WC | MCLK | $\overline{UIC}$ | FUNCTION OF $\overline{IV}$ BUS |
|---|---|---|---|---|---|
| L | L | L | X | X | Output Data |
| L | X | H | H | H | Input Data |
| L | H | L | X | X | Inactive |
| L | X | H | X | L | Inactive |
| L | X | H | L | H | Inactive |
| H | X | X | X | X | Inactive |

## Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note: *A logic "1" in Microcontroller software corresponds to a high level on the UD bus even though the $\overline{IV}$ bus is inverted.*) The 8X382 wakes up in the unselected state with all data bits latched at the "logic 1" level (UD bus outputs high if enabled).

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Power supply voltage | +7 | $V_{DC}$ |
| $V_I$ | Input voltage | +5.5 | $V_{DC}$ |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

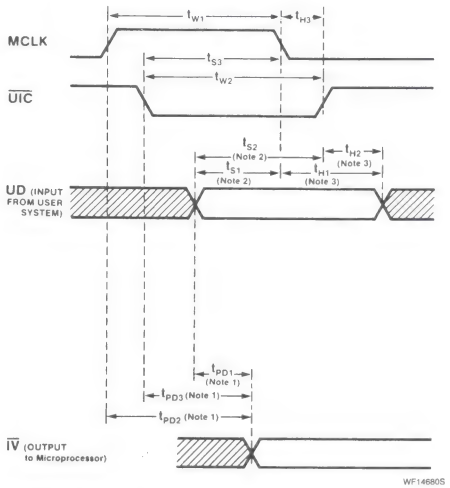
## DC ELECTRICAL CHARACTERISTICS $4.75V \leq V_{CC} \leq 5.25V$, $-55°C \leq T_C \leq +125°C$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High level input voltage | | 2.0 | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN; $I_I$ = –10mA | | | –1.5 | V |
| $I_{IH}$ | High level input current[1] | $V_{CC}$ = MAX; $V_{IH}$ = 2.7V | | | 100 | µA |
| $I_{IL}$ | Low level input current[1] | $V_{CC}$ = MAX; $V_{IL}$ = 0.5V | | | –550 | µA |
| $V_{OL}$ | Low level output voltage | $V_{CC}$ = MIN; $I_{OL}$ = 16mA | | | 0.55 | V |
| | $\overline{IV}$ bus ($\overline{IV0}$ = $\overline{IV7}$), User bus (UD4 – UD7) | $V_{CC}$ = MIN; $I_{OL}$ = 24mA | | | 0.55 | V |
| $V_{OH}$ | High level output voltage | $V_{CC}$ = MIN; $I_{OH}$ = –3.2mA | 2.4 | | | V |
| $I_{OS}$ | Short circuit output current[2] | $V_{CC}$ = MAX | –20 | | | mA |
| | $\overline{IV}$ bus ($\overline{IV0}$ – $\overline{IV7}$), UD bus (UD4 – UD7) | $V_{CC}$ = MAX | –10 | | | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX; $\overline{ME}$ = $\overline{UOC}$ = $V_{CC}$ | | | 150 | mA |

## AC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V, -55°C \leq T_C \leq +125°C$

| SYMBOL | PARAMETER | REFERENCES | | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|
| | | From | To | | Min | Max | |
| **Pulse Widths:** | | | | | | | |
| $T_{W1}$ | Clock high | ↑MCLK | ↓MCLK | | 30 | | ns |
| $t_{W2}$ | User input control | ↓$\overline{UIC}$ | ↑$\overline{UIC}$ | MCLK = High | 35 | | ns |
| **Propagation Delays:** | | | | | | | |
| $t_{PD1}$ | UD propagation delay | UD | $\overline{IV}$ | MCLK = High<br>$\overline{RC}$ = WC = $\overline{ME}$ = $\overline{UCI}$ = Low | | 45 | ns |
| $t_{PD2}$ | UD clock delay | ↑MCLK | $\overline{IV}$ | UD = stable;<br>$\overline{RC}$ = WC = $\overline{ME}$ = $\overline{UIC}$ = Low | | 55 | ns |
| $t_{PD3}$ | UD input delay | ↓$\overline{UIC}$ | $\overline{IV}$ | UD = Stable; MCLK = High<br>$\overline{RC}$ = WC = $\overline{ME}$ = Low | | 55 | ns |
| $t_{PD4}$ | $\overline{IV}$ data propagation delay | $\overline{IV}$ | UD | MCLK = WC = $\overline{UIC}$ = High;<br>$\overline{ME}$ = $\overline{UOC}$ = $\overline{RC}$ = Low | | 45 | ns |
| $t_{PD5}$ | $\overline{IV}$ data clock delay | ↑MCLK | UD | WC = $\overline{UIC}$ = High; $\overline{IV}$ = Stable<br>$\overline{ME}$ = $\overline{UOC}$ = $\overline{RC}$ = Low | | 55 | ns |
| **Output Enable Timing:** | | | | | | | |
| $t_{OE1}$ | UD output enable | ↓UOC | UD | $\overline{UIC}$ = High | | 45 | ns |
| $t_{OE2}$ | UD input recovery | ↑$\overline{UIC}$ | UD | $\overline{UOC}$ = Low | | 45 | ns |
| $t_{OE3}$ | $\overline{IV}$ data master enable | ↓$\overline{ME}$ | $\overline{IV}$ | WC = $\overline{RC}$ = Low | | 45 | ns |
| $t_{OE4}$ | $\overline{IV}$ data read enable | ↓$\overline{RC}$ | $\overline{IV}$ | WC = $\overline{ME}$ = Low | | 45 | ns |
| $t_{OE5}$ | $\overline{IV}$ data write recovery | ↓WC | $\overline{IV}$ | $\overline{RC}$ = $\overline{ME}$ = Low | | 45 | ns |
| **Output Disable Timing:** | | | | | | | |
| $t_{OD1}$ | UD output disable | ↑$\overline{UOC}$ | UD | $\overline{UIC}$ = High | | 40 | ns |
| $t_{OD2}$ | UD input override | ↓$\overline{UIC}$ | UD | $\overline{UOC}$ = Low | | 45 | ns |
| $t_{OD3}$[3] | $\overline{IV}$ data master disable | ↑$\overline{ME}$ | $\overline{IV}$ | WC = $\overline{RC}$ = Low | | 40 | ns |
| $t_{OD4}$[3] | $\overline{IV}$ data read disable | ↑$\overline{RC}$ | $\overline{IV}$ | WC = $\overline{ME}$ = Low | | 40 | ns |
| $t_{OD5}$[3] | $\overline{IV}$ data write override | ↑WC | $\overline{IV}$ | $\overline{RC}$ = $\overline{ME}$ = Low | | 40 | ns |
| **Setup Time:** | | | | | | | |
| $t_{S1}$ | UD clock setup time | UD | ↓MCLK | $\overline{UIC}$ = Low | 15 | | ns |
| $t_{S2}$ | UD setup time | UD | ↑UIC | MCLK = High | 25 | | ns |
| $t_{S3}$ | User input control setup time | ↓$\overline{UIC}$ | ↓MCLK | | 25 | | ns |
| $t_{S4}$ | $\overline{IV}$ data setup time | $\overline{IV}$ | ↓MCLK | WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low | 15 | | ns |
| $t_{S5}$[4] | $\overline{IV}$ master enable setup time | ↓$\overline{ME}$ | ↓MLCK | WC = $\overline{UIC}$ = High | 20 | | ns |
| $t_{S6}$ | $\overline{IV}$ write control setup time | ↑WC | ↓MCLK | $\overline{ME}$ = Low; $\overline{UIC}$ = High | 40 | | ns |
| **Hold Times:** | | | | | | | |
| $t_{H1}$ | UD clock hold time | ↓MCLK | UD | $\overline{UIC}$ = Low | 20 | | ns |
| $t_{H2}$ | UD control hold time | ↑$\overline{UIC}$ | UD | MCLK = High | 10 | | ns |
| $t_{H3}$ | User input control hold time | ↓MCLK | ↑UIC | | 0 | | ns |
| $t_{H4}$ | $\overline{IV}$ data hold time | ↓MCLK | $\overline{IV}$ | WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low, 25°C | 5 | | ns |
| | | | | Temp. | 20 | | ns |
| $t_{H5}$[4] | $\overline{IV}$ master enable hold time | ↓MCLK | ↓$\overline{ME}$ | WE = $\overline{UIC}$ = High | 0 | | ns |
| $t_{H6}$ | $\overline{IV}$ write control hold time | ↓MCLK | ↓WC | $\overline{ME}$ = Low; $\overline{UIC}$ = High | 0 | | ns |

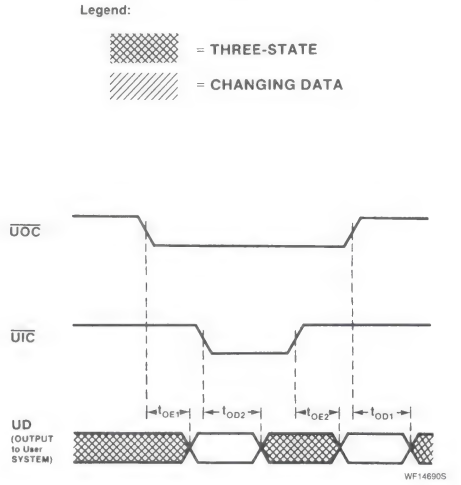
**NOTES:**
1. The input current includes the 3-State leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.
3. These parameters are measured with a capacitive loading of 50pF and represent the output driver turn-off time.
4. If $\overline{ME}$ is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.



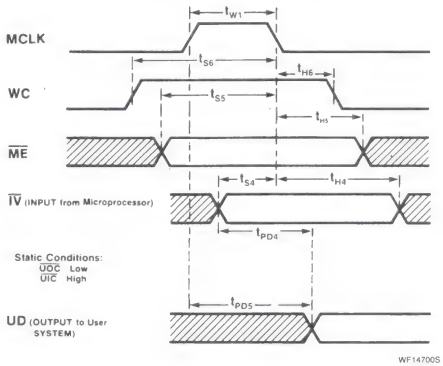

**STATIC CONDITIONS:**
SC = WC = $\overline{ME}$ = Low; $\overline{UOC}$ = High

**NOTES:**
1. The actual time for stable data on the $\overline{IV}$ bus is the latest propagation from $t_{PD1}$, $t_{PD2}$, and $t_{PD3}$.
2. The UD input must satisfy the setup-time requirements for both $t_{S1}$ and $t_{S2}$.
3. Minimum hold-time required for the UD input is the earlier of the times specified by $t_{H1}$ and $t_{H2}$.

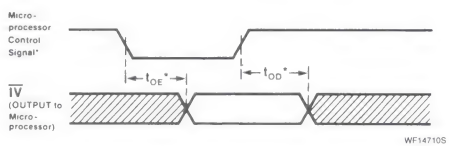
**a. User Data Input Timing**




**b. User Data Output Timing**




**c. Microcontroller Write Cycle Timing**



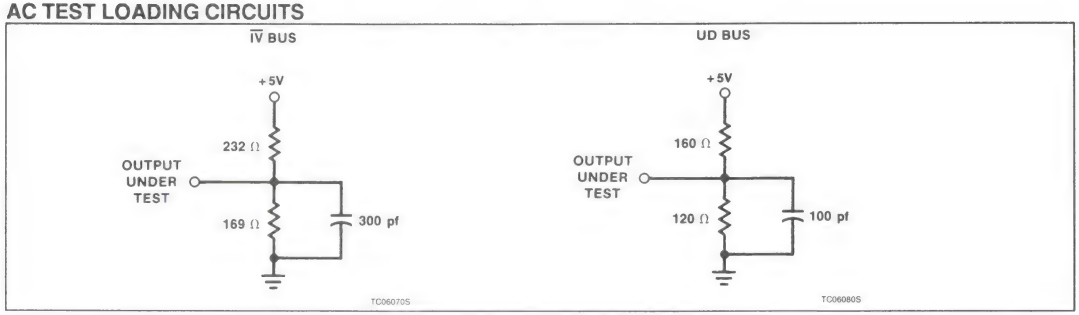

**d. Microcontroller Select Cycle Timing**

***PARAMETER KEY**

| MICROPROCESSOR CONTROL SIGNAL | AC TIMING PARAMETERS | STATIC CONDITIONS |
|---|---|---|
| $\overline{ME}$ | $t_{OE3}$ $t_{OD3}$ | SC = WC = LOW |
| $\overline{RC}$ | $t_{OE4}$ $t_{OD4}$ | SC = $\overline{ME}$ = LOW |
| SC | $t_{OE5}$ $t_{OD5}$ | $\overline{RC}$ = $\overline{ME}$ = LOW |

**Figure 2. Timing Diagrams**

## AC TEST LOADING CIRCUITS



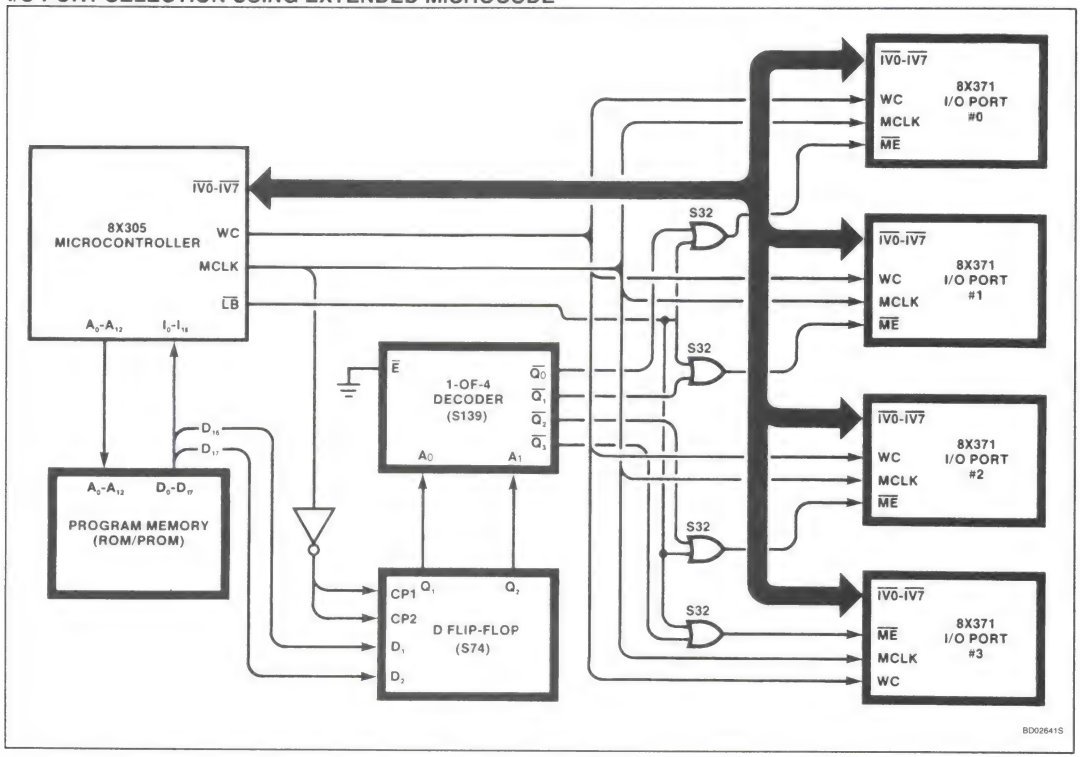

## APPLICATIONS

In some applications, performance of a Microcontroller system can be enhanced by using the 8X371 I/O Port instead of an addressable 8X372 port. Using a technique referred to as Extended Microcode or Fast $\overline{IV}$ Select, the address select cycles which normally precede a read or write operation when using an 8X372 can be eliminated by use of the 8X371.

This technique is often used in bit slice microprocessor designs and involves widening the program memory beyond the normal 16-bit requirement of the Microcontroller. the extra bits are used as enable signals for the 8X371 ports. Thus, the 8X371 is enabled during the instruction cycle in which it is required for input/output operations. Since the software overhead of separate address select cycles is eliminated, the overall system performance is improved.

As shown in the accompanying diagram, the program memory is extended by two bit positions ($D_{16}$ and $D_{17}$), permitting any one of four 8X371 ports to be enabled during those instructions. Because of timing considerations, latches must be used to hold the Extended Microcode through the end of the instruction cycle. A decoder is used to obtain four enable signals from the two extra bits. The decoder outputs are ORed with the $\overline{LB}$ output of the 8X305; thus, all four I/O ports are placed on the Left Bank of the $\overline{IV}$ bus.

## I/O PORT SELECTION USING EXTENDED MICROCODE



Signetics

# 8X372/8X376

## Addressable/Bidirectional I/O Ports

***Product Specification***

**Military**
**Customer Specific Products**

### FEATURES

- **Two bidirectional 8-bit busses**
- **Independent bus operation (user-bus priority for data entry)**
- **User data input synchronous (8X372) or asynchronous (8X376) with respect to MCLK**
- **Programmed Microcontroller port address**
- **3-State TTL outputs with high-drive capabilities**
- **Power-up to predetermined logic state**
- **Directly compatible with 8X305**
- **Single +5V supply**
- **0.4", 24-pin Dip**

### PRODUCT IDENTITY

8X372 Synchronous 3–State bidirectional I/O port with programmed address

8X376 Asynchronous, 3–State, bidirectional I/O port with programmed address.

### PRODUCT DESCRIPTION

Each of these I/O ports is an addressable device designed for use as a bidirectional interface element in systems that use TTL–compatible busses. Typically, these I/O ports are used with the 8X305 Microcontroller and its associated Interface Vector ($\overline{IV}$) bus; however, either port can also be used with the 8X300 Microcontroller or an equivalent microprocessor.

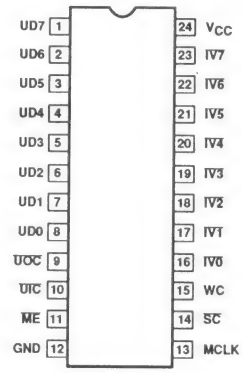
As shown in the logic diagram of Figure 1, each I/O port consists of eight identical data latches — bits 0 through 7. These latches are accessed through either of two 8-bit busses — one connected to the Microcontroller ($\overline{IV}$ bus) and the other to the user system (UD bus). Separate controls are provided for each bus and both busses operate independently, except when both attempt to input data at the same time. In such situations, the user bus always has priority. The data latches are transparent, in that, while either bus is enabled for input, all transitions in input data are propagated to the other bus, if enabled for output.

Both the 8X372 and 8X376 are available with preprogrammed addresses ($0_{10}$ through $255_{10}$); either device can be field-programmed over the same address range. Input/output operations can begin once the I/O port is selected and appropriate control signals are generated. Port selection is implemented by putting the I/O port address ($0_{10} - 255_{10}$) on the $\overline{IV}$ bus; once selected, the I/O port remains selected until a different "port address" is put on the bus. Thus, software overhead is minimized. Data is accessible on the UD bus at all times. A Master Enable ($\overline{ME}$) input, which is typically connected to the Left Bank ($\overline{LB}$) or Right Bank ($\overline{RB}$) output of the Microcontroller, provides the capability of organizing the $\overline{IV}$ bus into two separate and independent banks of I/O devices.

### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 24–Pin DIP | 8X372/BXA<br>8X376/BXA |

### PIN CONFIGURATION




| PIN NO. | IDENTIFIER | FUNCTION |
|---|---|---|
| 1–8 | UD7–UD0 | 3–State, bidirectional User Data (UD) bus; UD0 and corresponds to $\overline{IV0}$. |
| 9 | $\overline{UOC}$ | User Output Control – active low input to enable data output to UD0 – UD7. |
| 10 | $\overline{UIC}$ | User Input Control – active low input to enable data input from UD0 – UD7. |
| 11 | $\overline{ME}$ | Master Enable – active low input to enable the $\overline{IV}$ bus for data input, data output; or $\overline{IV}$ address selection/deselection; UD–bus operations are unaffected. |
| 12 | GND | Ground. |
| 13 | MCLK | Master Clock – active high input (from Microcontroller used to strobe data into data latches from the $\overline{IV}$ bus and, for the synchronous 8X372, from the UD bus; MCLK also synchronizes $\overline{IV}$ address selection. |
| 14 | $\overline{SC}$ | Select Command – active high input from Microcontroller to enable $\overline{IV}$ address input from the $\overline{IV}$ bus for device selection. |
| 15 | WC | Write Command – active high input from Micontroller to enable the writing of data into the data latches from the $\overline{IV}$ bus, provided $\overline{UIC}$ is not low. |
| 16–23 | $\overline{IV0}$–$\overline{IV7}$ | Interface Vector (Input/Output Bus) – 3–State, bidirectional, Microcontroller data bus; $\overline{IV0}$ corresponds to UD0. |
| 24 | $V_{CC}$ | +5V power supply. |

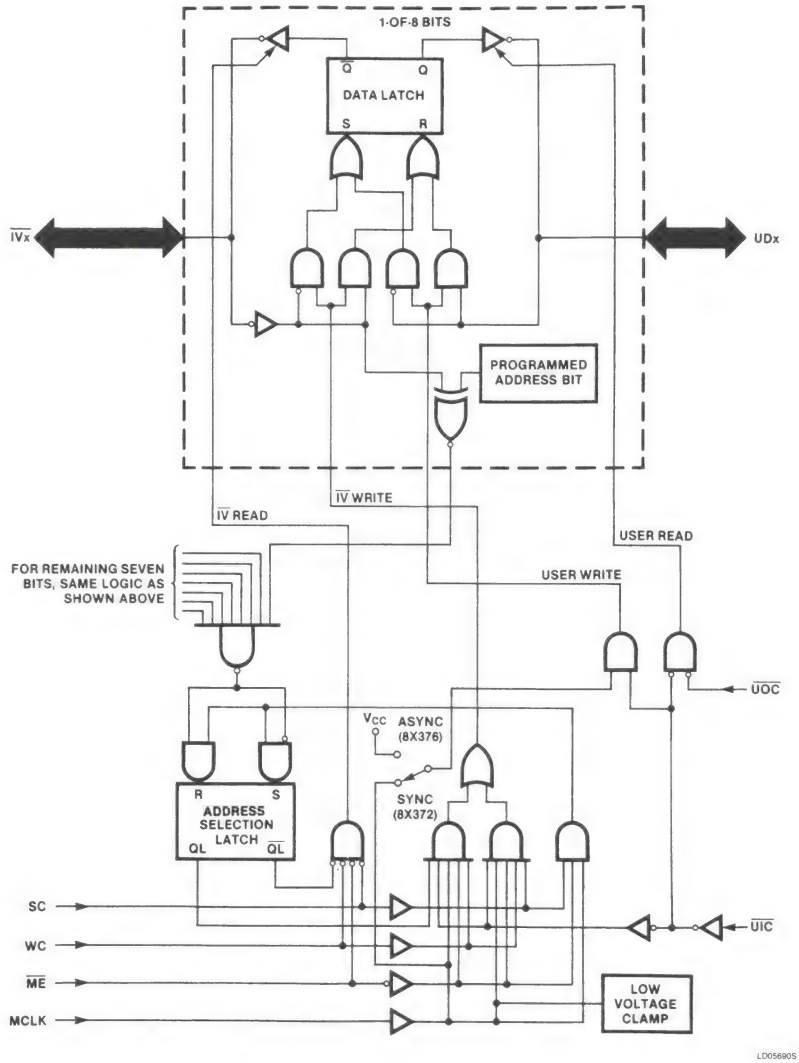



**Figure 1. Logic Diagram for 8X372/8X376 I/O Ports**

## FUNCTIONAL OPERATION

### UD Bus Control

As shown in Table 1, the User Data (UD) bus interface is controlled by the $\overline{UIC}$ and $\overline{UOC}$ inputs. For the 8X372, data input from the UD bus is written synchronously with MCLK, that is, with $\overline{UIC}$ low, information is written into the data latches only when MCLK is high. In the case of the 8X376, data input is asynchronous, in that, with $\overline{UIC}$ low, data is latched in without regard to the level of MCLK. (Note: *To avoid the possibility of processor error when using the asynchronous 8X376, the $\overline{IV}$ bus should not be read during the time the data latches are changing due to user input.*.) Output drivers on the UD bus are enabled when UOC is low and $\overline{UIC}$ is high.

### $\overline{IV}$ Bus Control

Input/output control of the $\overline{IV}$ bus is shown in Table 2; this bus is controlled by SC, WC, $\overline{ME}$, MCLK and the current state of the internal address selection latch. As shown in Table 2, $\overline{UIC}$ is required to indicate priority of the UD bus for data input operations. The selection latch in the I/O port stores the result of the most recent $\overline{IV}$ address selection. The latch is set when the internally preprogrammed address of the port matches the address on the $\overline{IV}$ bus during an address–selection operation (SC = MCLK = High/WC = Low). The latch is cleared when the two 8–bit address patterns are in disagreement. The $\overline{IV}$ bus can transfer data only when the selection latch is set. As shown in the APPLICATION DIAGRAM, the Microcontroller Left Bank ($\overline{LB}$) and Right Bank ($\overline{RB}$) outputs can control the $\overline{ME}$ inputs for two banks of I/O devices, thus, acting as a ninth address bit.

Data is written into the data latches of a selected device from the $\overline{IV}$ bus when WC, MCLK, and $\overline{UIC}$ are all high and $\overline{ME}$ is low. To prevent data–input conflicts, inputs from the $\overline{IV}$ bus are inhibited when $\overline{UIC}$ is low; under all other conditions, the $\overline{IV}$ and UD busses operate independently. Output drivers on the $\overline{IV}$ bus of a selected device are enabled when $\overline{ME}$, WC, and SC are all low and the address selection latch is set. With SC and WC both high (Shaded entry of Table 2), the bit pattern present on $\overline{IV0}$ – $\overline{IV7}$ is interpreted as both input data and $\overline{IV}$ address. Provided $\overline{UIC}$ is high, the data is latched into the data latches whether or not the I/O port has been previously selected. If the preprogrammed address of the I/O port matches the bit pattern on $\overline{IV0}$ = $\overline{IV7}$ when SC and WC are both high, the selection latch is set; otherwise, it is reset. (Note: *The Microcontroller never drives both SC and WC high at the same time.*)

**Table 1. Input/Output Control of UD Bus**

| $\overline{UIC}$ | $\overline{UOC}$ | MCLK | FUNCTION OF UD BUS | |
|---|---|---|---|---|
| | | | 8X372 | 8X376 |
| H | L | X | Output data | Output data |
| L | X | H | Input data | Input data |
| L | X | L | Inactive | Input data |
| H | H | X | Inactive | Inactive |

NOTE:
X = Don't care

**Table 2. Input/Output Control Of IV Bus**

| $\overline{ME}$ | SC | WC | MCLK | $\overline{UIC}$ | SELECTION | FUNCTION |
|---|---|---|---|---|---|---|
| | | | | | LATCH | $\overline{IV}$ BUS |
| L | L | L | X | X | Set | Output Data |
| L | L | H | H | H | Set | Input Data |
| L | H | L | H | X | X | Input Address* |
| L | H | H | H | H | X | Input data and Address* |
| L | H | H | H | L | X | Input Address* |
| L | X | H | L | X | X | Inactive |
| L | H | X | L | X | X | Inactive |
| L | L | H | H | L | X | Inactive |
| L | L | X | X | X | Not Set | Inactive |
| H | X | X | X | X | X | Inactive |

NOTE:
X = Don't care
* Selection latch is updated

### Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note: *A logic "1" in Microcontroller software corresponds to a high level on the UD bus even though the $\overline{IV}$ bus is inverted.*) Both the 8X372 and 8X376 wickiup with the address selection latch in the unselected state and all data bits latched at the "logic 1" level (UD bus outputs high if enabled).

## ADDRESS PROGRAMMING AND ADDRESS PROTECT

### Programming Procedures

Both 8X372 and 8X376 can be programmed to respond to any address within a range of $0_{10}$ through $255_{10}$. In an unprogrammed state, low level ($\leq$0.8V) inputs on all $\overline{IV}$ bus lines (address $255_{10}$) will select the device. To program a given address bit to match a high level ($\geq$ 2.0V) input on the corresponding $\overline{IV}$ pin (a logical "0" to the Microcontroller), the counterpart UD–bus pin must be pulsed according to Table 3 and the following procedures:

Step 1: Set all control inputs to the inactive state— $\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = $V_{CC}$ and SC = WC = MCLK = GND; leave the UD and $\overline{IV}$ bus pins open.

Step 2: Increase $V_{CC}$ to $V_{CCP}$.

Step 3: After $V_{CC}$ has stabilized, apply a single programming pulse (Figure 2) to the user–bus bit that corresponds to the desired high–level $\overline{IV}$ address bit. The I/O port is programmed from the user bus (UD0 – UD7) for addressing from the Microcontroller bus ($\overline{IV0}$ – $\overline{IV7}$).

Step 4: Return $V_{CC}$ to 0–V. (Note: *If the programming of all address bits is completed in less than 1–second $V_{CC}$ can remain at 90–V for the required interval of time.*)

Step 5: Steps 1 through 3 are applicable to the programming of each address bit that requires a high–level $\overline{IV}$ match.

Step 6: To verify that the address is properly programmed, return $V_{CC}$ to +5V, set $\overline{IV0}$ – $\overline{IV7}$ to the desired (inverted) binary address pattern, set $\overline{ME}$ = WC = Low and SC = MCLK = High. If there are no programming errors, subsequent data written from $\overline{IV0}$ – $\overline{IV7}$ (WC = High) will appear inverted on UD0 – UD7.

### Address Protect

After programming the I/O Port, steps should be taken to isolate the address circuits and make these circuits permanently immune to further change.

Step 1: Set $V_{CC}$ and all control inputs to 0V $V_{CC}$ = $\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = SC = WC = MCLK = 0V; $\overline{IV0}$ – $\overline{IV7}$ = open circuit.

Step 2: Taking one pin at a time, apply a protect programming pulse (Figure 3) to each user–bus bit (UD0 – UD7) — refer to Table 3 for Min/Max specifications pertaining to voltage and current.

Step 3: Verify that the address circuits for each bit is isolated by applying 9V, in turn, to each user–bus pin (UD0 – UD7) and measuring less than 200 microamperes of input current. (Note: *Setup conditions are the same as those in Step 1.*)

**Table 3. Programming Specification**

| PARAMETERS | LIMITS | | | UNITS |
|---|---|---|---|---|
| | Min | Typ | Max | |
| $V_{CCP}$ — Programming supply voltage: | | | | |
| Address | 8.75 | 9.0 | 9.25 | V |
| Protect | | 0 | | V |
| Maximum time $V_{CCP}$ > 5.25V | | | 1.0 | Sec |
| Programming voltage: | | | | |
| Address | 8.75 | 9.0 | 9.25 | V |
| Protect | 8.75 | | 9.25 | V |
| Programming current: | | | | |
| Address | | | 5 | mA |
| Protect | | | 50 | mA |
| $t_r$ — Programming pulse rise time: | | | | |
| Address | 10 | | 100 | µS |
| Protect | 10 | | 100 | µS |
| tω — Programming pulse width | 0.5 | | 1.0 | mS |

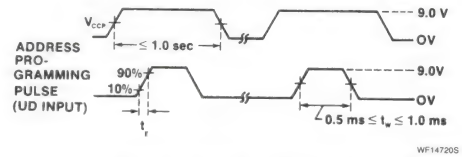



**Figure 2. Address Programming Pulse**

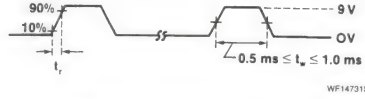



**Figure 3. Protect Programming Pulse**

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Power supply voltage[3] | +7 | $V_{DC}$ |
| $V_I$ | Input voltage[3] | +5.5 | $V_{DC}$ |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V, -55°C \leq T_C \leq +125°C$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High level input voltage | | 2.0 | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = Min; $I_I$ = –10mA | | | –1.5 | V |
| $I_{IH}$ | High level input current[1] | $V_{CC}$ = Max; $V_{IH}$ = 2.7V | | | 100 | µA |
| $I_{IL}$ | Low level input current[1] | $V_{CC}$ = Max; $V_{II}$ = 0.5V | | | –550 | µA |
| $V_{OL}$ | Low level output voltage<br>$\overline{IV}$ Bus ($\overline{IV0}$ – $\overline{IV7}$) | $V_{CC}$ = Min; $I_{OL}$ = 16mA | | | 0.55 | V |
| | User Bus (UD0 – UD7) | $V_{CC}$ = Min; $I_{OL}$ = 24mA | | | 0.55 | V |
| $V_{OH}$ | High level output voltage | $V_{CC}$ = Min; $I_{OH}$ = –3.2mA | 2.4 | | | V |
| $I_{OS}$ | Short circuit output current[2]<br>$\overline{IV}$ bus ($\overline{IV0}$ – $\overline{IV7}$) | $V_{CC}$ = Max | –20 | | | mA |
| | UD bus (UD0 – UD7) | $V_{CC}$ = Max | –10 | | | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = Max; $\overline{ME}$, $\overline{UOC} \geq 4.0V$ | | | 150 | mA |

**NOTES:**
1. The input current includes the 3–State leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.
3. These limits do not apply during address programming.

## AC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq +125°C$

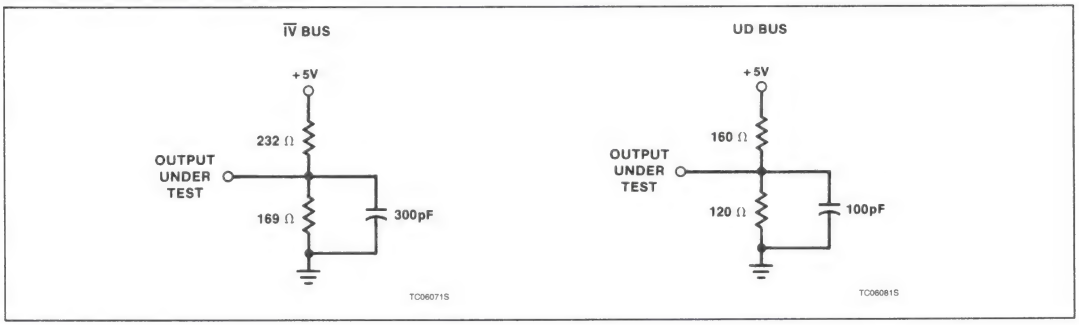
| SYMBOL | PARAMETER | REFERENCES | | TEST CONDITIONS | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | From | To | | | Min | Typ | Max | |
| **Pulse Widths:** | | | | | | | | | |
| $t_{W1}$ | Clock high | ↑MCLK | ↓MCLK | | | 30 | | | ns |
| $t_{W2}$ | User input control | ↓$\overline{UIC}$ | ↑$\overline{UIC}$ | MCLK = High | | 35 | | | ns |
| **Propagation Delays:** | | | | | | | | | |
| $t_{PD1}$ | UD propagation delay | UD | $\overline{IV}$ | MCLK = High<br>SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low | | | | 45 | ns |
| $t_{PD2}$ | UD clock delay (8X732 only) | ↑MCLK | $\overline{IV}$ | UD = Stable;<br>SC = WC = $\overline{ME}$ = $\overline{UIC}$ = Low | | | | 55 | ns |
| $t_{PD3}$ | UD input delay | ↓$\overline{UIC}$ | $\overline{IV}$ | UD = Stable; MCLK = High;<br>SC = WC = $\overline{ME}$ = Low | | | | 55 | ns |
| $t_{PD4}$ | $\overline{IV}$ data propagation delay | $\overline{IV}$ | UD | MCLK = WC = $\overline{UIC}$ = High<br>$\overline{ME}$ = $\overline{UOC}$ = SC = Low | | | | 45 | ns |
| $t_{PD5}$ | $\overline{IV}$ data clock delay | ↑MCLK | UD | WC = $\overline{UIC}$ = High; $\overline{IV}$ = Stable;<br>$\overline{ME}$ = $\overline{UOC}$ = SC = Low | | | | 55 | ns |
| **Output Enable Timing:** | | | | | | | | | |
| $t_{OE1}$ | UD output enable | ↓UOC | UD | $\overline{UIC}$ = High | | | | 45 | ns |
| $t_{OE2}$ | UD input recovery | ↑$\overline{UIC}$ | UD | $\overline{UOC}$ = Low | | | | 45 | ns |
| $t_{OE3}$ | $\overline{IV}$ data master enable | ↓$\overline{ME}$ | $\overline{IV}$ | WC = SC = Low | | | | 45 | ns |
| $t_{OE4}$ | $\overline{IV}$ data write recovery | ↓WC | $\overline{IV}$ | SC = $\overline{ME}$ = Low | | | | 45 | ns |
| $t_{OE5}$ | $\overline{IV}$ data select recovery | ↓SC | $\overline{IV}$ | SC = $\overline{ME}$ = Low | | | | 45 | ns |
| **Output Disable Timing:** | | | | | | | | | |
| $t_{OD1}$ | UD output disable | ↑$\overline{UOC}$ | UD | $\overline{UIC}$ = High | | | | 40 | ns |
| $t_{OD2}$ | UD input override | ↓WC | UD | $\overline{UOC}$ = Low | 8X372 | | | 45 | ns |
| | | | | | 8X376 | | | 55 | |
| $t_{OD3}$[2] | $\overline{IV}$ data master disable | ↑$\overline{ME}$ | $\overline{IV}$ | WC = SC = Low | | | | 40 | ns |
| $t_{OD4}$[2] | $\overline{IV}$ data write override | ↑WC | $\overline{IV}$ | SC = $\overline{ME}$ = Low | | | | 40 | ns |
| $t_{OD5}$[2] | $\overline{IV}$ data select override | ↑SC | $\overline{IV}$ | WC = $\overline{ME}$ = Low | | | | 40 | ns |
| **Setup Times:** | | | | | | | | | |
| $t_{S1}$ | UD clock setup time (8X372 only) | UD | ↓MCLK | $\overline{UIC}$ = Low | | 15 | | | ns |
| $t_{S2}$ | UD control setup time | UD | ↑$\overline{UIC}$ | MCLK = High | | 25 | | | ns |
| $t_{S3}$ | User input control setup time (8X372 only) | ↓$\overline{UIC}$ | ↓MCLK | | | 25 | | | ns |
| $t_{S4}$ | $\overline{IV}$ data setup time | $\overline{IV}$ | ↓MCLK | WC = High or SC = High;<br>$\overline{ME}$ = Low; $\overline{UIC}$ = High | | 15 | | | ns |
| $t_{S5}$[3] | $\overline{IV}$ master enable setup time | ↓ME | ↓MCLK | WC = High or SC = High;<br>$\overline{UIC}$ = High | | 21 | | | ns |
| $t_{S6}$ | $\overline{IV}$ write control setup time | ↑WC | ↓MCLK | SC = $\overline{ME}$ = Low; $\overline{UIC}$ = High | | 40 | | | ns |
| $t_{S7}$ | $\overline{IV}$ select control setup time | ↑SC | ↓MCLK | WC = $\overline{ME}$ = Low | | 30 | | | ns |

## AC ELECTRICAL CHARACTERISTICS (Continued)

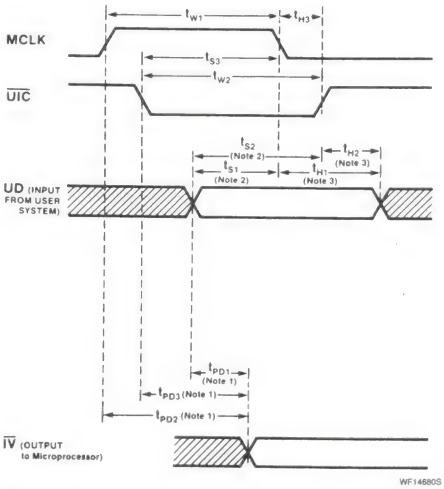
| SYMBOL | PARAMETER | REFERENCES | | TEST CONDITIONS | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | From | To | | | Min | Typ | Max | |
| **Hold Times:** | | | | | | | | | |
| $t_{H1}$ | UD clock hold time (8X372 only) | ↓MCLK | UD | $\overline{UIC}$ = Low | | 20 | | | ns |
| $t_{H2}$ | UD control hold time | ↑$\overline{UIC}$ | UD | MCLK = High | | 10 | | | ns |
| $t_{H3}$ | User input control hold time (8X372 only) | ↓MCLK | ↑$\overline{UIC}$ | | | 0 | | | ns |
| $t_{H4}$ | $\overline{IV}$ data hold time | ↓MCLK | $\overline{IV}$ | WC = High or SC = High; | 25°C | 5 | | | ns |
| | | | | $\overline{ME}$ = Low, $\overline{UIC}$ = High | Temp | 20 | | | |
| $t_{H5}$[3] | $\overline{IV}$ master enable hold time | ↓MCLK | ↑$\overline{ME}$ | WC = High or SC = High; $\overline{UIC}$ = High | | 0 | | | ns |
| $t_{H6}$ | $\overline{IV}$ write control hold time | ↓MCLK | ↓WC | SC = $\overline{ME}$ = Low; $\overline{UIC}$ = High | | 0 | | | ns |
| $t_{H7}$ | $\overline{IV}$ select control | ↓MCLK | ↓SC | WC = $\overline{ME}$ = Low | | 0 | | | ns |

**NOTES:**
1. All measurements to the $\overline{IV}$ bus assumes the address selection latch is set.
2. These parameters are measured with a capacitive loading of 50pf and represent the output drive turn–off time.
3. If $\overline{ME}$ is to be high (inactive) it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.

## AC TEST LOADING CIRCUITS



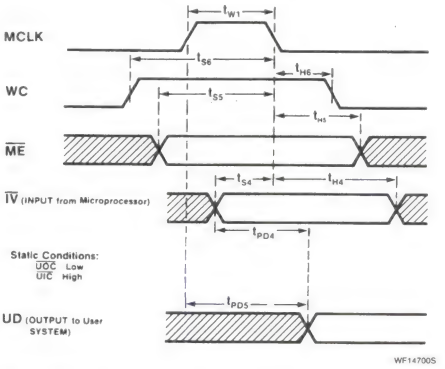
## TIMING DIAGRAMS




**STATIC CONDITIONS:**
SC WC $\overline{ME}$ Low
$\overline{UOC}$ High

**NOTES:**
1. The actual time for stable data on the $\overline{IV}$ bus is the latest propagation from $t_{PD1}$, $t_{PD2}$ and $t_{PD3}$.
2. The UD input must satisfy the setup-time requirements for both $t_{S1}$ and $t_{S2}$.
3. Minimum hold-time required for the UD input is the earlier of the times specified by $t_{H1}$ and $t_{H2}$.

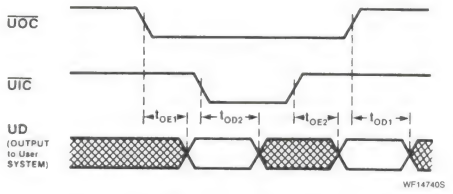
**a. User Data Input Timing**



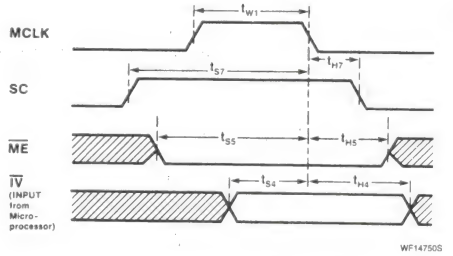

**STATIC CONDITIONS:**
$\overline{UOC}$ Low
$\overline{UIC}$ High

**c. Microcontroller Write Cycle Timing**

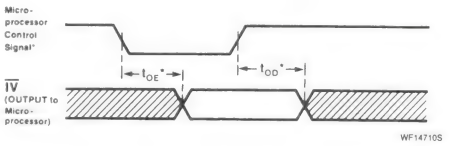
Legend:
= THREE-STATE
= CHANGING DATA




**b. User Data Output Enable**




**d. Microcontroller Select Cycle Timing**



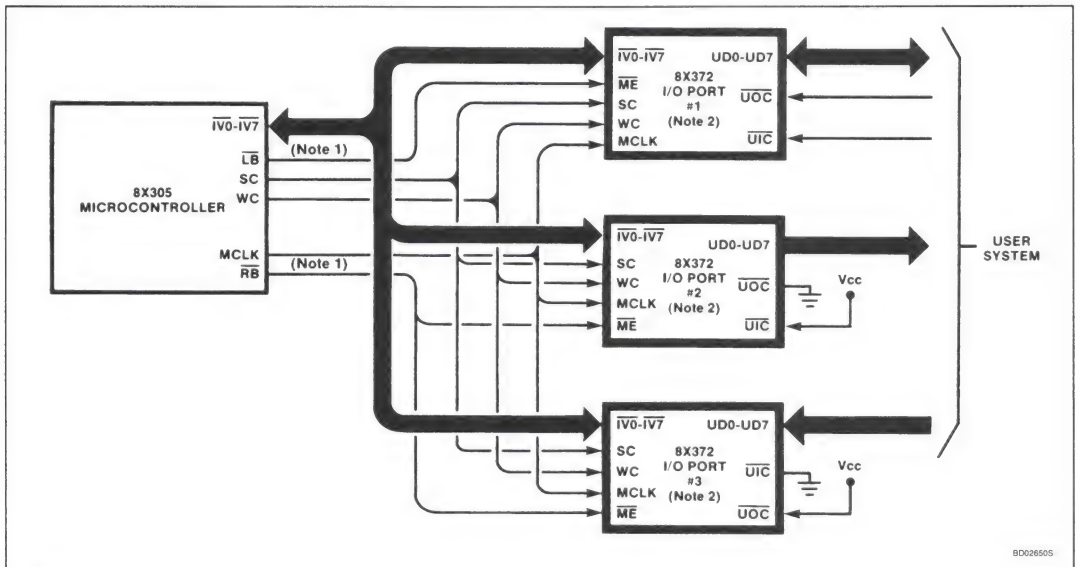

**e. Microcontroller Output Enable Timing**

### *PARAMETER KEY

| MICROPROCESSOR CONTROL SIGNAL | AC TIMING PARAMETERS | STATIC CONDITIONS |
|---|---|---|
| $\overline{ME}$ | $t_{OE3}$ $t_{OD3}$ | SC = WC = LOW |
| WC | $t_{OE4}$ $t_{OD4}$ | SC = $\overline{ME}$ = LOW |
| SC | $t_{OE5}$ $t_{OD5}$ | WC = $\overline{ME}$ = LOW |

## APPLICATIONS

One way of using I/O Ports in a microprocessor–based system is shown in the following application diagram; there are many other ways of implementing I/O functions with these parts, both singularly and in combination. By proper control the $\overline{UIC}$ and $\overline{UOC}$ lines, the user can implement bidirectional data transfers, exercise system control, and/or read system status. In the concept shown here, I/O Port #1 is setup for bidirectional data transfers and I/O Ports #2 and #3, respectively, serve as dedicated output and input devices.




**NOTES:**
1. Up to 256 discrete addresses can be assigned to each bank ($\overline{LB}$ or $\overline{RB}$).
2. The 8X376 can be implemented in an identical manner.

Signetics

# Section 5
# EPROM

**Military Products**

## INDEX


| | | |
|---|---|---|
| **27C64A** | 64K CMOS UV Erasable PROM (8K×8) | 613 |
| **27C256** | 256K CMOS UV Erasable PROM (32K×8) | 621 |
| **27C512** | 512K CMOS UV Erasable PROM (64K×8) | 630 |
| **27HC641** | 64K-Bit CMOS PROM (8K×8) | 634 |

Signetics

# 27C64A

## 64K CMOS UV Erasable PROM (8K×8)

*Product Specification*

**Military Application Specific Products**

### DESCRIPTION

The Signetics 27C64A CMOS EPROM is 64K-Bit 5V only memory organized as 8192 words of 8 bits, employing advanced CMOS circuitry for systems requiring high-power, high performance speeds and immunity to noise

The 27C64A has a non-multiplexed addressing interface and is pin compatible with the standard 2764.

The 27C64A achieves both high performance (200ns access time) and low power consumption (10mA active current maximum, CMOS inputs) making it ideal for high performance portable equipment.

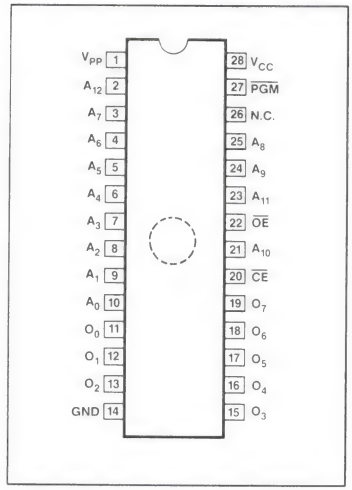
The highest degree of protection against latch-up is achieved through EPI (Epitaxial) processing. Prevention of latch-up is provided for stresses up to 100mA on address and data pins for -1V to $V_{CC}$ + 1V.

The 27C64A is programmed with standard EPROM programmers and the intelligent programming algorithm may be utilized.

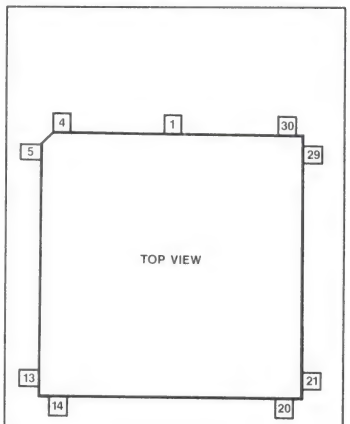
### FEATURES

- **CMOS microcontroller and microprocessor compatible**
  - **Universal 28- and 32-Pin memory site, 2-line control**
- **Low power consumption**
  - **10mA maximum active current**
  - **100μA maximum standby current**
- **High-performance speeds**
  - **200ns access time**
- **Noise Immunity features**
  - **±10% supply voltage**
  - **Maximum latch-up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **Programs in under one minute**
  - **12.5$V_{PP}$**

### CERDIP PIN CONFIGURATION




### LLCC PIN CONFIGURATION




**PIN / FUNCTION**

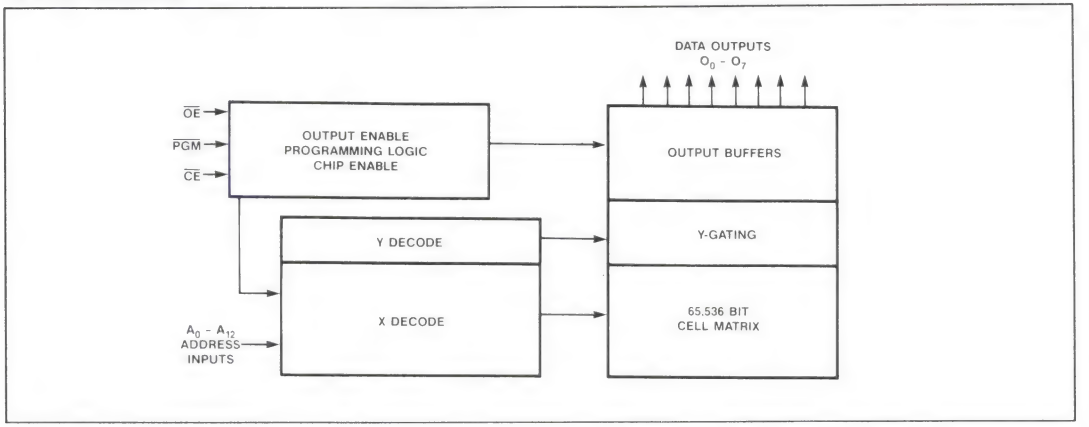
| | | | | | |
|---|---|---|---|---|---|
| 1 | NC | 12 | NC | 23 | $\overline{CE}$ |
| 2 | $V_{PP}$ | 13 | $O_0$ | 24 | $A_{10}$ |
| 3 | $A_{12}$ | 14 | $O_1$ | 25 | $\overline{OE}$ |
| 4 | $A_7$ | 15 | $O_2$ | 26 | NC |
| 5 | $A_6$ | 16 | $V_{SS}$ | 27 | $A_{11}$ |
| 6 | $A_5$ | 17 | NC | 28 | $A_9$ |
| 7 | $A_4$ | 18 | $O_3$ | 29 | $A_8$ |
| 8 | $A_3$ | 19 | $O_4$ | 30 | NC |
| 9 | $A_2$ | 20 | $O_5$ | 31 | $\overline{PGM}$ |
| 10 | $A_1$ | 21 | $O_6$ | 32 | $V_{CC}$ |
| 11 | $A_0$ | 22 | $O_7$ | | |

### PIN NAMES

| | |
|---|---|
| $A_0 - A_{12}$ | Addresses |
| $O_0 - O_7$ | Outputs |
| $\overline{OE}$ | Output Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{PGM}$ | Program Strobe |
| NC | No connect |
| GND | Ground |
| $V_{PP}$ | Program Voltage |
| $V_{CC}$ | Power Supply |

# 64K CMOS UV Erasable PROM (8K×8) — 27C64A

## BLOCK DIAGRAM




## ORDERING INFORMATION

| PACKAGES | ORDER CODE | | |
|---|---|---|---|
| | 200ns | 250ns | 350ns |
| 28–Pin Ceramic DIP w/Quartz Window | 27C64A/BXA–20 | 27C64A/BXA–25 | 27C64A/BXA–35 |
| 28–Pin Ceramic DIP w/o Quartz Window[1] | 27C64A/BXA–20 OT | 27C64A/BXA–25 OT | 27C64A/BXA–35 OT |
| 32–Pin Rectangular LLCC w/Quartz Window | 27C64A/BUA–20 | 27C64A/BUA–25 | 27C64A/BUA–35 |

## ABSOLUTE MAXIMUM RATINGS[2]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +125 | °C |
| $V_I$, $V_O$ | Voltage on any pin with respect to ground | –2.0 to $V_{CC}$ +7V | V |
| $V_I$ | Voltage on $\overline{CE}$ pin with respect to ground | –2.0 to +13.5 | V |
| $V_{PP}$ | Supply voltage with respect to ground during programming | –2.0 to 14.0 | V |
| $T_C$ | Operating temperature during read | –55 to +125 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$[3] | High–level input voltage | | 2.0 | | $V_{CC}$ + 0.5[9] | V |
| $V_{IH}$[3] | High–level input voltage CMOS | $V_{PP} = V_{CC}$ | $V_{CC}$ – 0.2 | | $V_{CC}$ + 0.2[9] | V |
| $V_{IL}$[3] | Low–level input voltage | $V_{PP} = V_{CC}$ | –0.5[9] | | 0.8 | V |
| $V_{IL}$[3] | Low–level input voltage CMOS | $V_{PP} = V_{CC}$ | –0.2[9] | | 0.2 | V |
| $I_{OH}$ | High–level output current | | | | –400 | µA |
| $I_{OL}$ | Low–level output current | | | | 2.1 | mA |
| $V_{PP}$ | $V_{PP}$ read voltage[8] | | $V_{CC}$ – 0.7 | | $V_{CC}$ | V |
| $T_A$ | Operating temperature range | | –55 | | +125 | °C |

# 64K CMOS UV Erasable PROM (8K×8) — 27C64A

## DC ELECTRICAL CHARACTERISTICS $-55\,°C \le T_C \le +125°C$, $V_{CC} = 5V \pm 10\%$

| SYMBOL | PARAMETER | TEST CONDITIONS | 27C64A–20, –25 | | | 27C64A–35 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[4] | Max | Min | Typ[4] | Max | |
| $I_{LIH}$ | Input leakage current | $V_I = V_{CC}$ = MAX | | 0.01 | +1.0 | | 0.01 | +1.0 | µA |
| $I_{LIL}$ | | $V_I$ = 0.0V | | | –1.0 | | | –1.0 | |
| $I_{OIH}$ | Output leakage current | $V_I = V_{CC}$ = MAX | | 0.01 | +1.0 | | 0.01 | +1.0 | µA |
| $I_{OIL}$ | | $V_I$ = 0.0V | | | –1.0 | | | –1.0 | |
| $I_{CC}$[5,7] TTL | Operating supply current TTL inputs | $\overline{CE} = \overline{OE} - V_{IL}$, $V_{PP} = V_{CC}$, $O_{0-7}$ = 0mA | | | 30.0 | | | 25.0 | mA |
| $I_{CC}$[5,7] CMOS | Operating supply current | $\overline{CE} = \overline{OE} - V_{IL}$, $V_{PP} = V_{CC}$ = MAX, $O_{0-7}$ = 0mA | | | 10.0 | | | 10.0 | mA |
| $I_{SB}$[5] TTL | Standby supply current TTL inputs | $\overline{CE} = V_{IH}$, $V_{CC}$ = MAX | | | 1.0 | | | 1.0 | mA |
| $I_{SB}$[5,6] CMOS | Standby supply current CMOS inputs | $\overline{CE} = V_{CC}$ = MAX | | | 100.0 | | | 140.0 | µA |
| $I_{PP}$[7] | $V_{PP}$ read current | $V_{PP} = V_{CC}$ = MAX | | | 100.0 | | | 100.0 | µA |
| $V_{IL}$<br>$V_{IL}$ | Input Low voltage (TTL)<br>Input Low voltage (CMOS) | $V_{PP} = V_{CC}$ = MAX<br>$V_{PP} = V_{CC}$ = MAX | –0.5[10]<br>–0.2[10] | | +0.8<br>+0.2 | –0.5[10]<br>–0.2[10] | | +0.8<br>+0.2 | V<br>V |
| $V_{IH}$ | Input High voltage | $V_{PP} = V_{CC}$ = MIN | 2.0 | | $V_{CC}$ + 0.5[10] | 2.0 | | $V_{CC}$ + 0.5[10] | V |
| $V_{IH}$ | Input High voltage (CMOS) | $V_{PP} = V_{CC}$ = MIN | $V_{CC}$ – 0.2 | | $V_{CC}$ + 0.2[10] | $V_{CC}$ – 0.2 | | $V_{CC}$ + 0.2[10] | V |
| $V_{OL}$ | Output Low voltage | $I_{OL}$ = MAX, $V_{CC}$ = MIN | | | 0.45 | | | 0.45 | V |
| $V_{OH}$ | Output High voltage | $I_{OH}$ = MAX, $V_{CC}$ = MIN | 2.4 | | | 2.4 | | | V |
| $I_{OS}$[8] | Output short–circuit current | $V_{CC}$ = MAX | | | –100.0 | | | –100.0 | mA |

## CAPACITANCE $T_A = 25°C$, f = 1.0MHz[10]

| SYMBOL | PARAMETER | TEST CONDITIONS | MAX | UNIT |
|---|---|---|---|---|
| $C_I$ | Address/control capacitance | $V_I$ = 0V | 6 | pF |
| $C_O$ | Output capacitance | $V_O$ = 0V | 12 | pF |

## READ MODES

| MODE | PINS | | | | |
|---|---|---|---|---|---|
| | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $\overline{PGM}$ (27) | $V_{PP}$ (1) | OUTPUTS (11–13, 15–19) |
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | $D_O$ |
| Output disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{CC}$ | Hi–Z |
| Standby | $V_{IH}$ | X[12] | X[12] | $V_{CC}$ | Hi–Z |

## READ MODE

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Assuming that addresses are stable, the address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs after a delay of $t_{CE}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

## STANDBY MODE

The 27C64A has a Standby mode which reduces the maximum $V_{CC}$ current to 100µA. The device is placed in the Standby mode when $\overline{CE}$ pin is in the High state. When in the Standby mode, the outputs are in a high–impedance state, independent of the $\overline{OE}$ input.

# 64K CMOS UV Erasable PROM (8K×8) — 27C64A

## READ OPERATION – AC CHARACTERISTICS $-55\ °C \leq T_C \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| VERSIONS | | 27C64A–20 | | 27C64A–25 | | 27C64A–35 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic[11] | Min | Max | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to output delay | | 200 | | 250 | | 350 | ns |
| $t_{CE}$ | $\overline{CE}$ to output delay | | 200 | | 250 | | 350 | ns |
| $t_{OE}$ | $\overline{OE}$ to output delay | | 75 | | 100 | | 120 | ns |
| $t_{OP}$[10] | $\overline{OE}$ or $\overline{CE}$ High to output Hi–Z | | 55 | | 55 | | 75 | ns |
| $t_{OH}$[10] | Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change – whichever is first | 0 | | 0 | | 0 | | ns |

## ERASURE CHARACTERISTICS

The recommended erasure procedure for the 27C64A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms ( Å ). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15Wsec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm$^2$ power rating. The 27C64A should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C64A can be exposed to without damage is 7258µW/cm$^2$ (1 week @ 12,000Wsec/cm$^2$). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

The erasure characteristics of the 27C64A are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms ( Å ). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C64A in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C64A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

## AC TESTING LOAD CIRCUIT

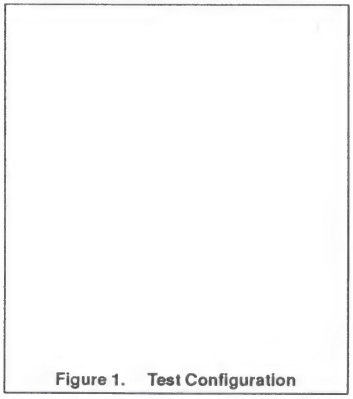
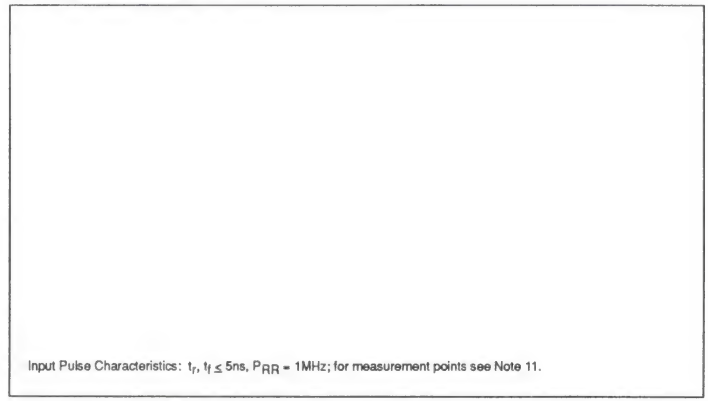


**Figure 1. Test Configuration**

## AC WAVEFORMS



Input Pulse Characteristics: $t_r$, $t_f \leq 5ns$, $P_{RR}$ = 1MHz; for measurement points see Note 11.

## PROGRAMMING MODES

| MODES | PINS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $\overline{PGM}$ (27) | $A_9$ (24) | $A_0$ (10) | $V_{PP}$ (1) | $V_{CC}$ (28) | OUTPUTS (11–13, 15–19) |
| Intelligent programming | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X[12] | X[12] | $V_{PP}$ | 6.0V[15] | $D_1$ |
| Program verify | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | X[12] | X[12] | $V_{PP}$ | 6.0V[15] | $D_0$ |
| Program inhibit | $V_{IH}$ | $V_{IH}$ | X | X[12] | X[12] | $V_{PP}$ | 6.0V[15] | Hi–Z |
| Intelligent identifier–manufacturer[14] | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_H$[13] | $V_{IL}$ | $V_{CC}$ | $V_{CC}$ | 15H |
| Intelligent identifier[14] | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_H$[13] | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | OBH |

# 64K CMOS UV Erasable PROM (8K×8) — 27C64A

## CMOS NOISE CHARACTERISTICS

Special epitaxial processing techniques have enabled Signetics to build CMOS with features adding to system reliability. These include Input/Output protection to latch–up. Each of the data and address pins will not latch–up with currents up to 100mA and voltages from –1V to $V_{CC}$ + 1V.

Additionally, the $V_{PP}$ (Programming) pin is designed to resist latch–up to the 14V maximum device limit.

## PROGRAMMING

***Caution:*** Exceeding 14.0V on $V_{PP}$ pin may permanently damage the 27C64A.

Initially, and after each erasure, all bits of the 27C64A are in the "1" state. Data is introduced by selectively programming "0" into the desired bit locations. Although only "0" will be programmed, both "1" and "0" can be present in the data word. The only way to change an "0" to a "1" is by ultraviolet light erasure.

The 27C64A is in the programming mode when the $V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL–low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

## INTELLIGENT PROGRAMMING ALGORITHM

The 27C64A intelligent programming algorithms rapidly program Signetics CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of five minutes. Actual programming times may vary due to differences in programming equipment.

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flow–chart of the 27C64A intelligent program algorithm is shown in Figure 2.

The intelligent programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3Xms. X is a duration counter and is equal to the number of the initial 1ms pulses applied to a particular 27C64A location, before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram is applied.

The entire sequence of program pulses and byte verifications is performed at $V_{CC}$ = 6.0V and $V_{PP}$ = 12.5V.

When the intelligent programming cycle has been completed, all bytes should be compared to the original data with $V_{CC}$ = 5.0V.

## PROGRAM INHIBIT

Programming of multiple 27C64A EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high–level $\overline{CE}$ input inhibits other 27C64A EPROMs from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27C64A's may be common. A TTL low–level pulse applied to the $\overline{PGM}$ and $\overline{CE}$ input with $V_{PP}$ at 12.5V will program the selected 27C64A.

## VERIFY

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ at $V_{IL}$ and $\overline{PGM}$ at $V_{IH}$. Data should be verified a minimum of $T_{OEV}$ after the falling edge of $\overline{OE}$.

## INTELLIGENT IDENTIFIER MODE

The intelligent identifier mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C64A.

To activate this mode the programming equipment must force 11.5V to 12.5V on address line $A_9$ of the 27C64A. Two bytes may then be sequenced from the device outputs by toggling address line $A_0$ from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during intelligent identifier mode.

## INTELLIGENT PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

$T_A$ = 25°C ± 5°C, $V_{CC}$ = 6.0V ± 0.25V, $V_{PP}$ = 12.5V ± 0.5V

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_I$ | Input current (all inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | 1.0 | µA |
| $V_{IL}$ | Input Low level (all inputs) | | –0.1 | 0.8 | V |
| $V_{IH}$ | Input High level | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low voltage during verify | $I_{OL}$ = 2.1mA | | 0.45 | V |
| $V_{OH}$ | Output High voltage during verify | $I_{OH}$ = –2.5mA | 3.5 | | V |
| $I_{CC2}$ | $V_{CC}$ supply current | $O_0 - O_7$ = 0mA | | 30 | mA |
| $I_{PP2}$ | $V_{PP}$ supply current (program) | $\overline{CE} = V_{IL}$ | | 30 | mA |

# 64K CMOS UV Erasable PROM (8K×8) — 27C64A

## AC PROGRAMMING CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS[16] | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{CES}$ | $\overline{CE}$ setup time | | 2 | | | µs |
| $t_{AS}$ | Address setup time | | 2 | | | µs |
| $t_{OES}$ | $\overline{OE}$ setup time | | 2 | | | µs |
| $t_{DS}$ | Data setup time | | 2 | | | µs |
| $t_{AH}$ | Address hold time | | 0 | | | µs |
| $t_{DH}$ | Data hold time | | 2 | | | µs |
| $t_{DFP}$[19] | $\overline{OE}$ High to output float delay | | 0 | | 130 | µs |
| $t_{VPS}$ | $V_{PP}$ setup time | | 2 | | | µs |
| $t_{VCS}$ | $V_{CC}$ setup time | | 2 | | | µs |
| $t_{PW}$ | $\overline{PGM}$ initial program pulse width | (See note 17) | 0.95 | 1.0 | 1.05 | ms |
| $t_{OPW}$ | $\overline{PGM}$ overprogram pulse width | (See note 18) | 2.85 | | 78.75 | ms |
| $t_{OE}$ | Data valid from $\overline{OE}$ | | | | 150 | ns |

**NOTES:**

1. Erase characteristics do not apply for one time programming (OT).
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Minimum DC input voltage is –0.5V. During transitions, the inputs may undershoot to –2.0V for periods less than 20ns.
4. Typical limits are at $V_{CC}$ = 5V, $T_A$ = + 25°C.
5. TTL inputs: spec $V_{IL}$, $V_{IH}$ levels;
   CMOS inputs: GND ± 0.2V to $V_{CC}$ ± 0.2V.
6. $\overline{CE}$ is $V_{CC}$ ± 0.2V. All other inputs can have any value within spec.
7. Maximum active power usage is the sum $I_{PP} + I_{CC}$.
8. Output shorted for no more than one second. No more than one output shorted at a time.
9. $V_{PP}$ may be one diode voltage drop below $V_{CC}$. It may be connected directly to $V_{CC}$.
10. Guaranteed, but not tested.
11. AC characteristics tested at $V_{IH}$ = 2.4V and $V_{IL}$ = 0.45V. Timing measurements made at $V_{OL}$ = 0.8V and $V_{OH}$ = 2.0V.
12. X can be $V_{IL}$ or $V_{IH}$.
13. $V_H$ = 12.0V ± 0.5V.
14. $A_1 - A_8$, $A_{10} - A_{12} = V_{IL}$.
15. $V_{CC}$ = 6.0V ± 0.25V.
16. AC Conditions of Test:
    Input Rise and Fall Times (100% to 90%): 20ns
    Input Pulse Levels: 0.45V to 2.4V
    Input Timing Reference Level: 0.8V to 2.0V
    Output Timing Reference Level: 0.8V to 2.0V
17. Initial Program Pulse width tolerance is 1msec ± 5%.
18. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
19. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven (see Timing Diagram).

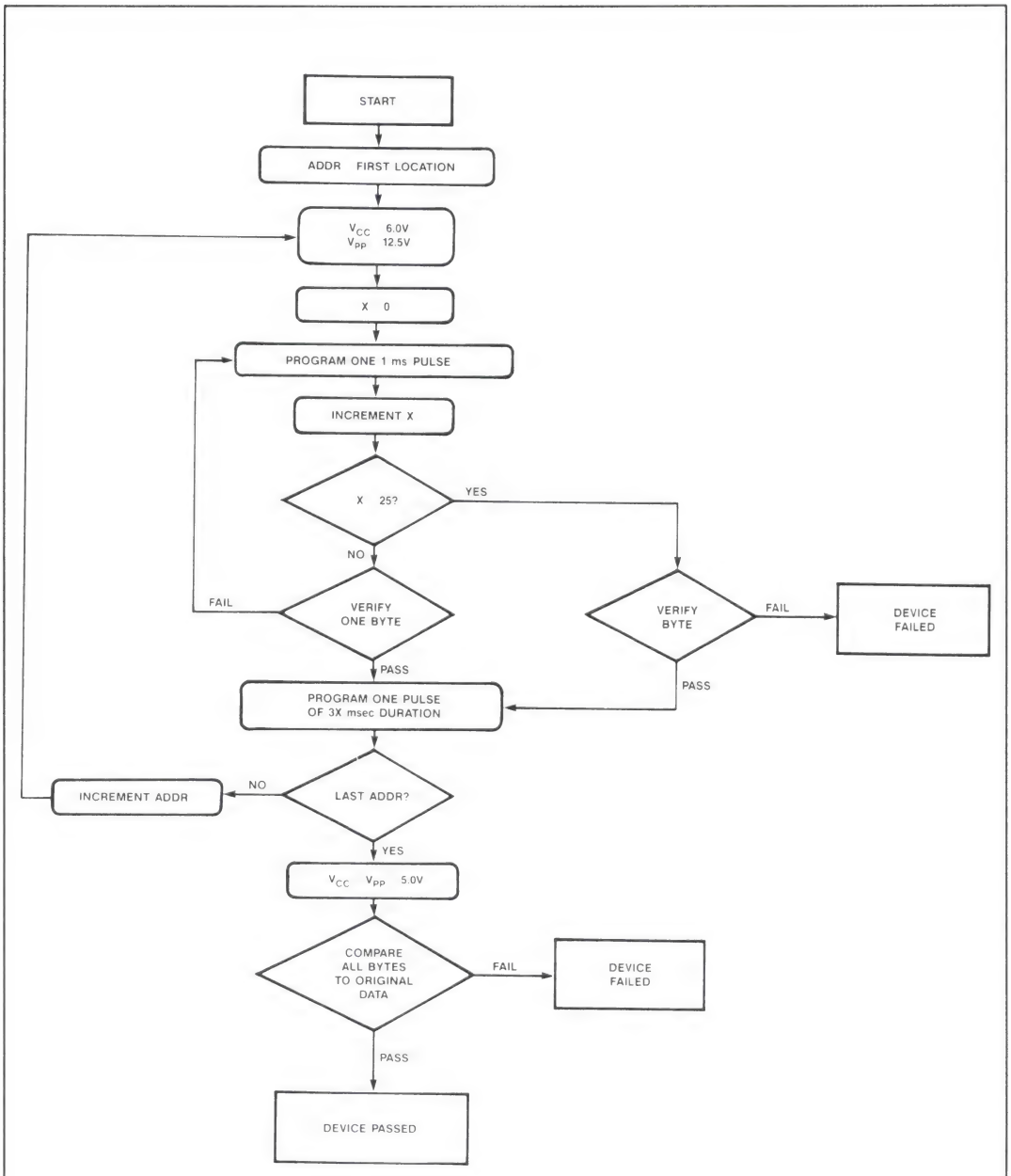
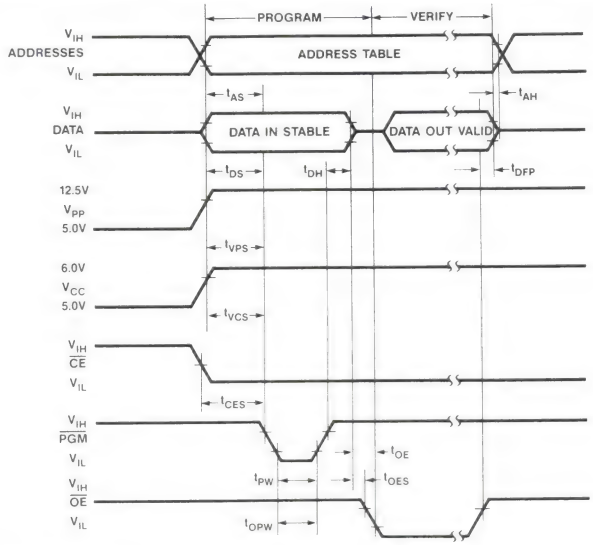



**Figure 2. Intelligent Programming Flowchart**




**NOTES:**

1. The Input Timing Regerence Level is 0.8V for $V_{IL}$ and 2V for a $V_{IH}$.
2. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer.
3. When programming 27C64A, a 0.1uF capacitor is required across Vpp and ground to suppress spurious voltage transients which can damage the device.

**Figure 3. Intelligent Programming Waveform**

Signetics

# 27C256

## 256K CMOS UV Erasable PROM (32K×8)

***Product Specification***

**Military Application Specific Products**

### DESCRIPTION

The Signetics 27C256 CMOS EPROMs are 256K-Bit 5V only memories organized as 32,768 words of 8 bits. They employ advanced CMOS circuitry for systems requiring low-power, high-performance speeds and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug compatible with the industry standard 27256.

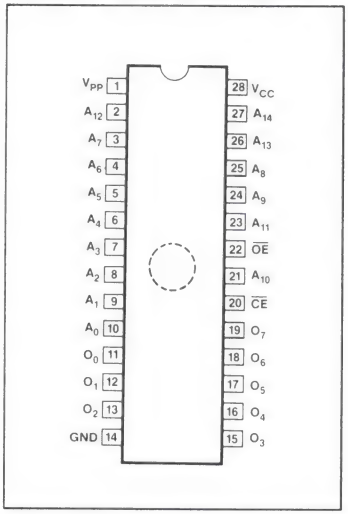
The 27C256 achieves both high-performance and low power consumption (10mA active current maximum, CMOS inputs), making them ideal for high-performance, portable equipment.

It is programmed with standard EPROM programmers and the intelligent programming algorithm may be utilized.

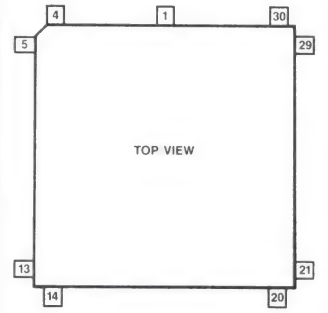
### FEATURES

- **CMOS/NMOS microcontroller and microprocessor compatible**
  - **Universal 28- or 32-Pin memory site, 2-line control**
- **Low power consumption**
- **Noise Immunity features**
  - **±10% $V_{CC}$ tolerance**
  - **Maximum latch-up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **12.5V $V_{PP}$, HCMOS 11-E compatible**

### CERDIP PIN CONFIGURATION




### LLCC PIN CONFIGURATION




**PIN/FUNCTION**

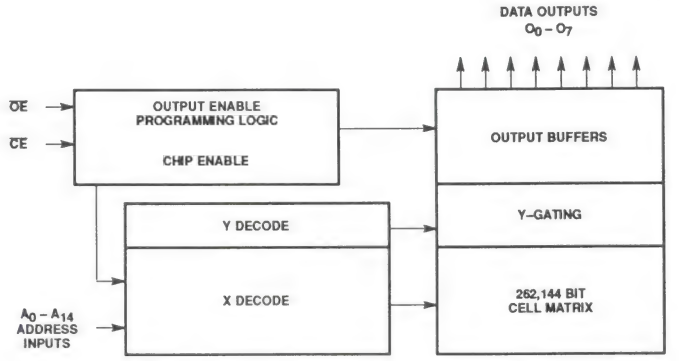
| | | | | | |
|---|---|---|---|---|---|
| 1 | NC | 12 | NC | 23 | $\overline{CE}$ |
| 2 | $V_{PP}$ | 13 | $O_0$ | 24 | $A_{10}$ |
| 3 | $A_{12}$ | 14 | $O_1$ | 25 | $\overline{OE}$ |
| 4 | $A_7$ | 15 | $O_2$ | 26 | NC |
| 5 | $A_6$ | 16 | $V_{SS}$ | 27 | $A_{11}$ |
| 6 | $A_5$ | 17 | NC | 28 | $A_9$ |
| 7 | $A_4$ | 18 | $O_3$ | 29 | $A_8$ |
| 8 | $A_3$ | 19 | $O_4$ | 30 | $A_{13}$ |
| 9 | $A_2$ | 20 | $O_5$ | 31 | $A_{14}$ |
| 10 | $A_1$ | 21 | $O_6$ | 32 | $V_{CC}$ |
| 11 | $A_0$ | 22 | $O_7$ | | |

### PIN NAMES

| | |
|---|---|
| $A_0 - A_{14}$ | Addresses |
| $O_0 - O_7$ | Outputs |
| $\overline{OE}$ | Output Enable |
| $\overline{CE}$ | Chip Enable |
| GND | Ground |
| $V_{PP}$ | Program Voltage |
| $V_{CC}$ | Power Supply |

# 256K CMOS UV Erasable PROM (32Kx8) — 27C256

## BLOCK DIAGRAM




## ORDERING INFORMATION

| PACKAGES | ORDER CODE | |
|---|---|---|
| | 200ns | 250ns |
| 28–Pin Ceramic DIP w/Quartz Window | 27C256/BXA–20 | 27C256/BXA–25 |
| 28–Pin Ceramic DIP w/o Quartz Window[1] | 27C256/BXA–20 OT | 27C256/BXA–25 OT |
| 32–Pin Rectangular LLCC w/Quartz Window | 27C256/BUA–20 | 27C256/BUA–25 |

## ABSOLUTE MAXIMUM RATINGS[2]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_I$, $V_O$ | Voltage on any pin with respect to ground | –2.0 to $V_{CC}$ +7V | V |
| $V_I$ | Voltage on $\overline{CE}$ Pin with respect to ground | –2.0 to +13.5 | V |
| $V_{PP}$ | Supply voltage with respect to ground during programming | –2.0 to 14.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$[3] | High–level input voltage | 2.0 | | $V_{CC}$ + 0.5[12] | V |
| $V_{IH}$[3] | High–level input voltage CMOS $V_{PP} = V_{CC}$ | $V_{CC}$ – 0.2 | | $V_{CC}$ + 0.2[12] | V |
| $V_{IL}$[3] | Low–level input voltage $V_{PP} = V_{CC}$ | –0.5[12] | | 0.8 | V |
| $V_{IL}$[3] | Low–level input voltage CMOS $V_{PP} = V_{CC}$ | –0.2[12] | | 0.2 | V |
| $I_{OH}$ | High–level output current | | | –400 | µA |
| $I_{OL}$ | Low–level output current | | | 2.1 | mA |
| $V_{PP}$ | $V_{PP}$ read voltage [8] | $V_{CC}$ – 0.7 | | $V_{CC}$ | V |
| $T_A$ | Operating temperature range | –55 | | +125 | °C |

# 256K CMOS UV Erasable PROM (32Kx8) 27C256

## READ OPERATION DC CHARACTERISTICS $-55\ °C \leq T_A \leq +125°C$, $V_{CC} = 5V \pm 10\%$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[4] | Max | |
| $I_{LIH}$ | Input leakage current | $V_I = V_{CC} = MAX$ | | 0.01 | +1.0 | µA |
| $I_{LIL}$ | | $V_I = 0.0V$ | | | –1.0 | µA |
| $I_{OIH}$ | Output leakage current | $V_I = V_{CC} = MAX$ | | 0.01 | +1.0 | µA |
| $I_{OIL}$ | | $V_I = 0.0V$ | | | –1.0 | µA |
| $I_{CC}TTL$[6,8] | Operating current TTL inputs | $\overline{CE} = \overline{OE} - V_{IL}$, $V_{PP} = V_{CC}$ - MAX $O_0 - O_7 = 0mA$ | | | 30 | mA |
| $I_{CC}CMOS$[6,8] | Operating current CMOS inputs | $\overline{CE} = \overline{OE} - V_{IL}$, $V_{PP} = V_{CC}$ - MAX $O_0 - O_7 = 0mA$ | | | 10 | mA |
| $I_{SB}TTL$[8] | Standby current TTL inputs | $\overline{CE} = V_{IH}$ | | | 2 | mA |
| $I_{SB}CMOS$[5] | Standby current CMOS inputs | $\overline{CE} = V_{IH}$ | | | 100 | µA |
| $I_{PP}$[8] | $V_{PP}$ read current | $V_{PP} = V_{CC} = MAX$ | | | 200 | µA |
| $V_{IL}$[9] | Input Low voltage (TTL)<br>Input Low voltage (CMOS) | $V_{PP} = V_{CC}$ | –0.5[10]<br>–0.2[10] | | 0.8<br>0.2 | V<br>V |
| $V_{IH}$[9] | Input High voltage (TTL)<br>Input High voltage (CMOS) | $V_{PP} = V_{CC}$ | 2.0<br>$V_{CC}$ –0.2 | | $V_{CC}$ + 0.5[10]<br>$V_{CC}$ + 0.2[10] | V<br>V |
| $V_{OL}$ | Output Low voltage | $I_{OL} = MAX$ | | | 0.45 | V |
| $V_{OH}$ | Output High voltage | $I_{OH} = MAX$ | 2.4 | | | V |
| $I_{OS}$[7] | Output short–circuit current | | | | –100 | mA |

## CAPACITANCE $T_A = 25°C$, $f = 1.0MHz$

| SYMBOL | PARAMETER | TEST CONDITIONS | MAX | UNIT |
|---|---|---|---|---|
| $C_I$[10] | Address/control capacitance | $V_I = 0V$ | 6 | pF |
| $C_O$[10] | Output capacitance | $V_O = 0V$ | 12 | pF |

## READ MODES

| MODE | PINS | | | |
|---|---|---|---|---|
| | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $V_{PP}$ (1) | OUTPUTS (11–13, 15–19) |
| Read | $V_{IL}$ | $V_{IL}$ | $V_{CC}$ | $D_O$ |
| Output disable | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | Hi–Z |
| Standby | $V_{IH}$ | X | $V_{CC}$ | Hi–Z |

## READ MODE

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs after a delay of $t_{\overline{OE}}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}$–$t_{OE}$.

## STANDBY MODE

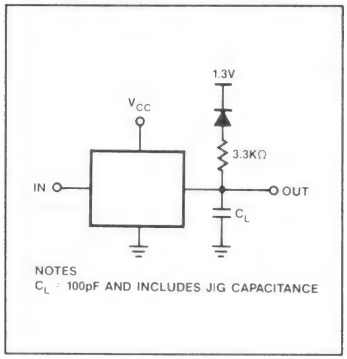
The 27C256 has a Standby mode which reduces the maximum CMOS V current to 100µA. The device is placed in the Standby mode when Pin 20 is in the High state. When in the Standby mode, the outputs are in a high–impedance state, independent of the $\overline{OE}$ input.

# 256K CMOS UV Erasable PROM (32Kx8) 27C256

## READ OPERATION – AC CHARACTERISTICS $-55\,°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$[12]

| SYMBOL | PARAMETER | 27C256–20 | | 27C256–25 | | UNIT |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to output delay | | 200 | | 250 | ns |
| $t_{CE}$ | $\overline{CE}$ to output delay | | 200 | | 250 | ns |
| $t_{OE}$ | $\overline{OE}$ to output delay | | 75 | | 100 | ns |
| $t_{OP}$[10] | $\overline{OE}$ or $\overline{CE}$ High to output Hi–Z | | 55 | | 60 | ns |
| $t_{OH}$[10] | Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change – whichever is first | 0 | | 0 | | ns |

## AC TESTING LOAD CIRCUIT




## SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS EPROMs require careful decoupling of the devices. The supply current, $I_{CC}$, has three segments that are of interest to the system designer – the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the devices. The associated transient voltage peaks can be suppressed by complying with Two–Line Control and by properly selected decoupling capacitors.

It is recommended that a 0.1µF ceramic capacitor be used on every device between $V_{CC}$ and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between $V_{CC}$ and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PC board traces.

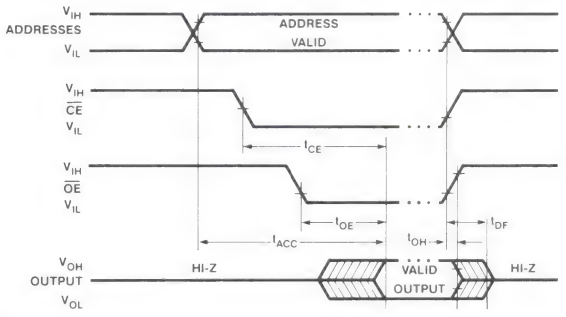
## ERASURE CHARACTERISTICS

The erasure characteristics of the 27C256 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å Range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C256 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C256 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 27C256 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15Wsec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm$^2$ power rating. The 27C256 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C256 can be exposed to without damage is 7258W/cm$^2$ (1 week @ 1200µW/cm$^2$). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

# 256K CMOS UV Erasable PROM (32Kx8) — 27C256

## AC WAVEFORMS




Input Pulse Characteristics: $t_r$, $T_f \leq 5ns$, $P_{RR} = 1MHz$

## PROGRAMMING MODES

| MODES | PINS | | | | | | |
|---|---|---|---|---|---|---|---|
| | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $A_9$ (24) | $A_0$ (10) | $V_{PP}$ (1) | $V_{CC}$ (28) | OUTPUTS (11–13, 15–19) |
| Intelligent programming | $V_{IL}$ | $V_{IH}$ | $X^{13}$ | $X^{13}$ | $V_{PP}$ | 6.0V[16] | $D_1$ |
| Program verify | $V_{IH}$ | $V_{IL}$ | $X^{13}$ | $X^{13}$ | $V_{PP}$ | 6.0V[16] | $D_2$ |
| Program inhibit | $V_{IH}$ | $V_{IH}$ | $X^{13}$ | $X^{13}$ | $V_{PP}$ | 6.0V[16] | Hi–Z |
| Intelligent identifier–manufacturer[15] | $V_{IL}$ | $V_{IL}$ | $V_H$[14] | $V_{IL}$ | $V_{CC}$ | $V_{CC}$ | 15H |
| Intelligent identifier[15] | $V_{IL}$ | $V_{IL}$ | $V_H$[14] | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | 8CH |

## CMOS NOISE CHARACTERISTICS

Special epitaphial processing techniques have enabled Signetics to build CMOS with features adding to system reliability. These include Input/Output protection to latch–up. Each of the data and address pins will not latch–up with currents up to 100mA and voltages from –1V to $V_{CC}$ + 1V.

Additionally, the $V_{PP}$ (Programming) pin is designed to resist latch–up to the 14V maximum device limit.

## PROGRAMMING

***Caution:*** Exceeding 14.0V on $V_{PP}$ Pin may permanently damage the 27C256.

Initially, and after each erasure, all bits of the 27C256 are in the "1" state. Data is introduced by selectively programming "0" into the desired bit location. Although only "0" will be programmed, both "1" and "0" can be present in the data word. The only way to change an "0" to a "1" is by ultraviolet light erasure.

The 27C256 is in the programming mode when the $V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL–Low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

## INTELLIGENT PROGRAMMING™ ALGORITHM

The 27C256 intelligent programming algorithms rapidly program Signetics CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of five minutes. Actual programming times may vary due to differences in programming equipment.

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flow–chart of the 27C256 intelligent program algorithm is shown in Figure 1.

The intelligent programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3Xms. X is a duration counter and is equal to the number of the initial 2ms pulses applied to a particular 27C256 location, before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram is applied.

The entire sequence of program pulses and byte verifications is performed at $V_{CC}$ = 6.0V and $V_{PP}$ = 12.5V.

When the intelligent programming cycle has been completed, all bytes should be compared to the original data with $V_{CC}$ = 5.0V.

## PROGRAM INHIBIT

Programming of multiple 27C256 EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high–level $\overline{CE}$ input inhibits other 27C256 EPROMs from being programmed.

Except for $\overline{OE}$ or $\overline{CE}$, all inputs of the parallel 27C256s may be common. A TTL low–level pulse applied to the $\overline{CE}$ or ALE/$\overline{CE}$ input with $V_{PP}$ at 12.5V will program the selected 27C256.

## VERIFY

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at $V_{IL}$ and $\overline{CE}$ at $V_{IH}$ and $V_{PP}$ at 12.5V.

Data should be verified a minimum of $T_{OEV}$ after the falling edge of $\overline{OE}$.

# 256K CMOS UV Erasable PROM (32Kx8) — 27C256

## INTELLIGENT IDENTIFIER MODE

The intelligent identifier mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C256.

To activate this mode the programming equipment must force 11.5V to 12.5V on address line $A_9$ of the 27C256. Two bytes may then be sequenced from the device outputs by toggling address line $A_0$ from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during intelligent identifier mode.

## INTELLIGENT PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

$T_A$ = 25°C ± 5°C, $V_{CC}$ = 6.0V ± 0.25V, $V_{PP}$ = 12.5V ± 0.5V

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{IH}$ | Input current (all inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | 1.0 | µA |
| $V_{IL}$ | Input Low level (all inputs) | | –0.1 | 0.8 | V |
| $V_{IH}$ | Input High level | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low voltage during verify | $I_{OL}$ = 2.1mA | | 0.45 | V |
| $V_{OH}$ | Output High voltage during verify | $I_{OH}$ = –2.5mA | 3.5 | | V |
| $I_{CC2}$ | $V_{CC}$ supply current | $O_0 - O_7$ = 0mA | | 30 | mA |
| $I_{PP2}$ | $V_{PP}$ supply current (program) | $\overline{CE} = V_{IL}$ | | 50 | mA |

## AC PROGRAMMING CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS[17] | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{CES}$ | $\overline{CE}$ setup time | | 2 | | | µs |
| $t_{AS}$ | Address setup time | | 2 | | | µs |
| $t_{OES}$ | $\overline{OE}$ setup time | | 2 | | | µs |
| $t_{DS}$ | Data setup time | | 2 | | | µs |
| $t_{AH}$ | Address hold time | | 0 | | | µs |
| $t_{DH}$ | Data hold time | | 2 | | | µs |
| $t_{DFP}$[20] | $\overline{OE}$ High to output float delay | | 0 | | 130 | µs |
| $t_{VPS}$ | $V_{PP}$ setup time | | 2 | | | µs |
| $t_{VCS}$ | $V_{CC}$ setup time | | 2 | | | µs |
| $t_{PW}$ | $\overline{CE}$ initial program pulse width | (See note 18) | 0.95 | 1.0 | 1.05 | ms |
| $t_{OPW}$ | $\overline{CE}$ overprogram pulse width | (See note 19) | 2.85 | | 78.75 | ms |
| $t_{OE}$ | Data valid from $\overline{OE}$ | | | | 150 | ns |

# 256K CMOS UV Erasable PROM (32Kx8) 27C256

**NOTES:**

1. Erase characteristics do not apply for one time programming (OT).
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Minimum DC input voltage is –0.5V. during transitions, the inputs may undershoot to –2.0V for periods less than 20ns.
4. Typical limits are at $V_{CC}$ = 5V, $T_A$ = + 25°C.
5. Other inputs can have any value within spec.
6. Maximum active power usage is the sum $I_{PP}$ + $I_{CC}$ and is measured at 5MHz.
7. Output shorted for no more than one second. No more than one output shorted at a time. $I_{OS}$ is sampled but not 100% tested.
8. $V_{PP}$ may be one diode voltage drop below $V_{CC}$. It may be connected directly to $V_{CC}$. Also, $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
9. TTL inputs: spec TTL at $V_{IL}$, $V_{IH}$ levels. CMOS inputs: GND ± 0.2V to $V_{CC}$ ± 0.2V.
10. Guaranteed, but not tested.
11. X can be $V_{IH}$ or $V_{IL}$.
12. AC characteristics tested at $V_{IH}$ = 2.4V and $V_{IL}$ = 0.45V. Timing measurements made at $V_{OL}$ = 0.8V and $V_{OH}$ = 2.0V.
13. X can be $V_{IL}$ or $V_{IH}$.
14. $V_H$ = 12.0V ± 0.5V.
15. $A_1 - A_9$, $A_{10} - A_{12} = V_{IL}$.
16. $V_{CC}$ = 6.0V ± 0.25V.
17. AC Conditions of Test:
    Input Rise and Fall Times (100% to 90%): 20ns
    Input Pulse Levels: 0.45V to 2.4V
    Input Timing Reference Level: 0.8V to 2.0V
    Output Timing Reference Level: 0.8V to 2.0V
18. Initial Program Pulse width tolerance is 1msec ± 5%.
19. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
20. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven (see Timing Diagram).

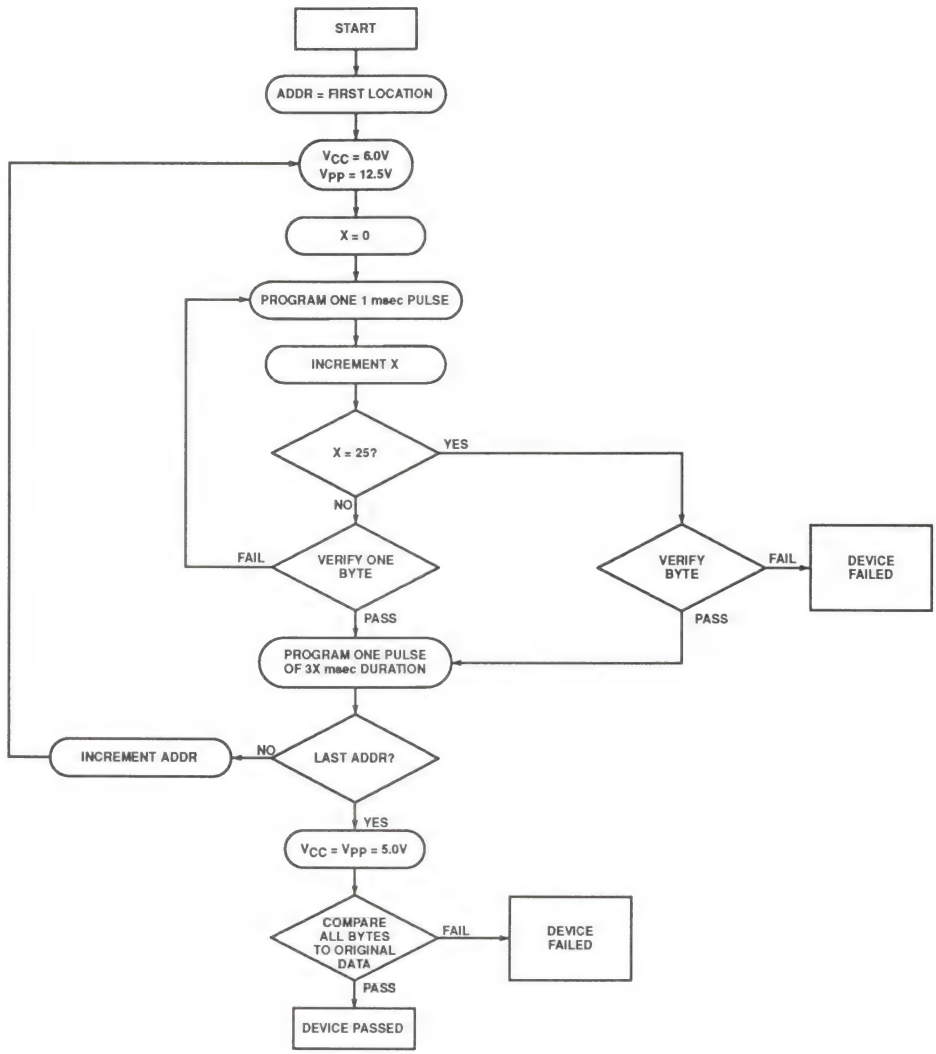
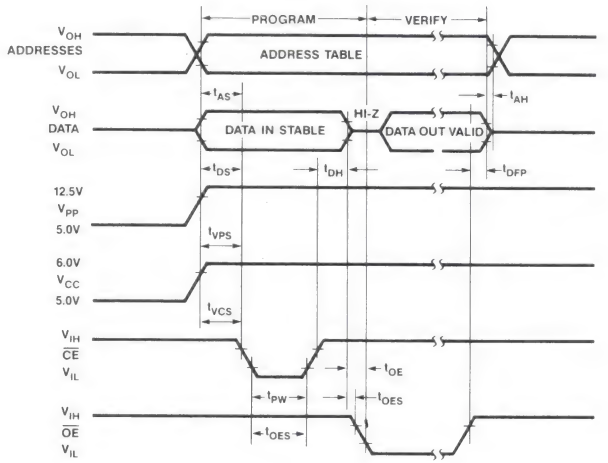



**Figure 4. Intelligent Programming Flowchart**




**NOTES:**
1. The Input Timing Reference Level is 0.8V for $V_{IL}$ and 2V for a $V_{IH}$, input pulse levels are 0.45V and 2.4V.
2. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer.
3. When programming 27C256, a 0.1uF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients which can damage the device.

**Figure 5. Intelligent Programming Waveforms**

Signetics

# 27C512

## 512K CMOS UV Erasable PROM (64K×8)

*Product Specification*

**Military Standard Products**

### DESCRIPTION

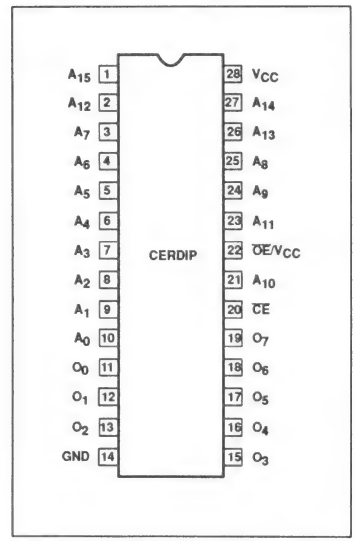
The Signetics 27C512 CMOS EPROM is a 512K-bit, 5V-only memory organized as 65,536 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds and immunity to noise. The 27C512 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27512.

The 27C512, available in a ceramic DIP package, achieves both high performance and low power consumption, making it ideal for high-performance, portable equipment. This device can be programmed with standard EPROM programmers.

### FEATURES

- **CMOS/NMOS microcontroller and microprocessor compatible**
  - **Universal 28–pin memory site, 2–line control**
- **Low power consumption**
- **Noise Immunity features**
  - **±10% $V_{CC}$ tolerance**
  - **Maximum latch–up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **12.5V $V_{PP}$, HCMOS 11–E compatible**

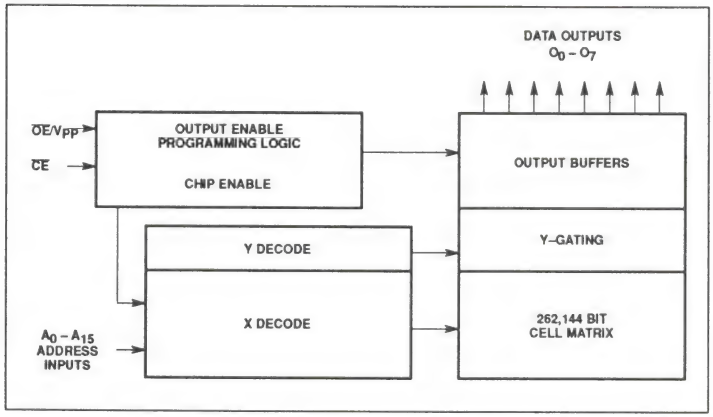
### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | |
|---|---|---|
| | 200ns | 250ns |
| 28–Pin Ceramic DIP w/Quartz Window | 27C512/BXA–20 | 27C512/BXA–25 |

### BLOCK DIAGRAM




### PIN NAMES

| | |
|---|---|
| $A_0 - A_{15}$ | Addresses |
| $O_0 - O_7$ | Outputs |
| $\overline{OE}/V_{CC}$ | Output Enable/ Programming Voltage |
| $\overline{CE}$ | Chip Enable |
| GND | Ground |
| $V_{CC}$ | Power Supply |

# 512K CMOS UV Erasable PROM (64K×8) — 27C512

## ABSOLUTE MAXIMUM RATINGS[2]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_I$, $V_O$ | Voltage on any pin with respect to ground | –2.0 to $V_{CC}$ +1.0 | V |
| $V_I$ | Voltage on $\overline{CE}$ Pin with respect to ground | –2.0 to +13.5 | V |
| $V_{PP}$ | Supply voltage with respect to ground during programming | –2.0 to 14.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$[3,9] | High–level input voltage | 2.0 | | $V_{CC}$ + 0.5[12,10] | V |
| $V_{IH}$[3,9] | High–level input voltage CMOS | $V_{CC}$ – 0.2 | | $V_{CC}$ + 0.2[12,10] | V |
| $V_{IL}$[3,9] | Low–level input voltage | –0.5[12,10] | | 0.8 | V |
| $V_{IL}$[3,9] | Low–level input voltage CMOS | –0.2[12,10] | | 0.2 | V |
| $I_{OH}$ | High–level output current | | | –400 | µA |
| $I_{OL}$ | Low–level output current | | | 2.1 | mA |
| $T_A$ | Operating temperature range | –55 | | +125 | °C |

## READ OPERATION DC CHARACTERISTICS –55 °C ≤ $T_A$ ≤ + 125°C, $V_{CC}$ = 5V ± 10%

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[4] | Max | |
| $I_{LIH}$ | Input leakage current | $V_I = V_{CC}$ = MAX | | 0.01 | 10 | µA |
| $I_{LIL}$ | | $V_I$ = 0.0V, $V_{CC}$ = MAX | | | –10 | µA |
| $I_{OIH}$ | Output leakage current | $V_I = V_{CC}$ = MAX | | 0.01 | +1.0 | µA |
| $I_{OIL}$ | | $V_I$ = 0.0V, $V_{CC}$ = MAX | | | –1.0 | µA |
| $I_{CC}$TTL[6,8] | Operating current TTL inputs | $\overline{CE} = \overline{OE} - V_{IL}$, $V_{PP} = V_{CC}$ = MAX<br>$O_0 - O_7$ = 0mA, f = $1/T_{ACC\ MAX}$ | | | 30 | mA |
| $I_{SB}$TTL[8] | Standby current TTL inputs | $\overline{CE} = V_{IH}$, $V_{CC}$ = MAX | | | 2 | mA |
| $I_{SB}$CMOS[5] | Standby current CMOS inputs | $\overline{CE} = V_{IH}$, $V_{CC}$ = MAX | | | 100 | µA |
| $V_{OL}$ | Output Low voltage | $I_{OL}$ = MAX, $V_{CC}$ = MIN | | | 0.45 | V |
| $V_{OH}$ | Output High voltage | $I_{OH}$ = MAX, $V_{CC}$ = MIN | 2.4 | | | V |
| $I_{OS}$[7] | Output short–circuit current | $V_{CC}$ = MAX, $I_O$ = 0V | | | –100 | mA |

## CAPACITANCE $T_A$ = 25°C, f = 1.0MHz

| SYMBOL | PARAMETER | CONDITIONS | MAX | UNIT |
|---|---|---|---|---|
| $C_I$[10] | Address/control capacitance | $V_I$ = 0V | 6 | pF |
| $C_O$[10] | Output capacitance | $V_O$ = 0V | 12 | pF |
| $C_{IN}$[10] | $\overline{OE}/V_{PP}$ | $V_I$ = 0V | 25 | pF |

# 512K CMOS UV Erasable PROM (64K×8) — 27C512

## READ OPERATION – AC CHARACTERISTICS $-55\ °C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$[12]

| SYMBOL | PARAMETER | 27C512–20 | | 27C512–25 | | UNITS |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to output delay | | 200 | | 250 | ns |
| $t_{CE}$ | $\overline{CE}$ to output delay | | 200 | | 250 | ns |
| $t_{OE}$ | $\overline{OE}$ to output delay | | 75 | | 100 | ns |
| $t_{OP}$[10] | $\overline{OE}$ or $\overline{CE}$ High to output Hi–Z | | 55 | | 60 | ns |
| $t_{OH}$[10] | Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change – whichever is first | 0 | | 0 | | ns |

**NOTES:**
1. Erase characteristics do not apply for one time programming (OT).
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Minimum DC input voltage is –0.5V. during transitions, the inputs may undershoot to –2.0V for periods less than 20ns.
4. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$.
5. Other inputs can have any value within spec.
6. Maximum active power usage is the sum $I_{PP} + I_{CC}$ and is measured at 5MHz.
7. Output shorted for no more than one second. No more than one output shorted at a time. $I_{OS}$ is sampled but not 100% tested.
8. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
9. TTL inputs: spec TTL at $V_{IL}$, $V_{IH}$ levels. CMOS inputs: GND ± 0.2V to $V_{CC}$ ± 0.2V.
10. Guaranteed, but not tested.
11. X can be $V_{IH}$ or $V_{IL}$.
12. AC characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.

## DEVICE OPERATION – START

| MODE | $\overline{CE}$ | $\overline{OE}/V_{PP}$ | OUTPUT |
|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $D_{OUT}$ |
| Output disable | $V_{IL}$ | $V_{IH}$ | Hi–Z |
| Standby | $V_{IH}$ | X[11] | Hi–Z |

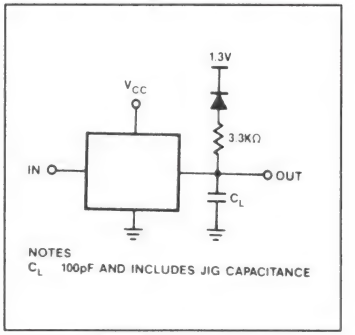
## READ MODE

The 27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable $\overline{OE}/V_{PP}$ is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of $t_{OE}$ from the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC}–t_{OE}$.

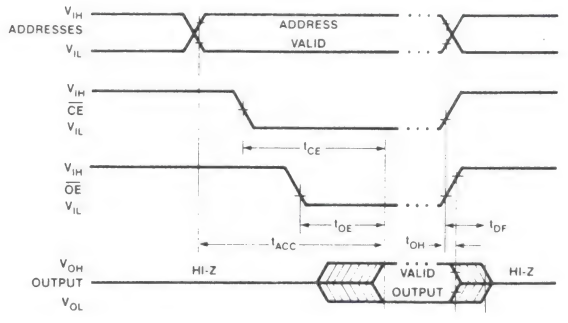
## STANDBY MODE

The 27C512 has a standby mode which reduces the maximum $V_{CC}$ current to 100µA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high–impedance state, independent of the $\overline{OE}/V_{PP}$ pin.

## AC TESTING LOAD CIRCUIT



## AC VOLTAGE WAVEFORMS




Input Pulse Characteristics: $t_r$, $T_f \leq 5ns$, $P_{RR} = 1MHz$

## PROGRAMMING INFORMATION

Complete programming system specifications for the quick-pulse programming program method are available upon request from Signetics Military Marketing.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of PROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available upon request from Signetics Military Memory Marketing.

## PROGRAMMING THE 27C512

*Caution:* Exceeding 14.0V on $\overline{OE}/V_{PP}$ Pin may permanently damage the 27C512.

The 27C512 Quick Pulse programming algorithms rapidly program CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Actual programming times may vary due to differences in programming equipment.

Initially, all bits of the 27C512 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.

The 27C512 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.75V and $\overline{CE}$ is at TTL Logic Low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

## INTELLIGENT IDENTIFIER

The intelligent identifier provides the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is functional in the 25°±5°C ambient temperature range. To activate this mode, the equipment must force 11.5V to 12.5V on address $A_9$ of the 27C512. Two bytes may then be read from the device outputs by toggling address line $A_0$ from $V_{IL}$ to $V_{IH}$. The $\overline{CE}$, $\overline{OE}/V_{PP}$ and all other address lines must be at $V_{IL}$ during interrogation.

The identifier information for Signetics 27C512 is as follows:

| | |
|---|---|
| When $A_0 = V_{IL}$ data is "Manufacturer" | $15_{(HEX)}$ |
| When $A_0 = V_{IH}$ data is "Product" | $1D_{(HEX)}$ |

## ERASURE CHARACTERISTICS

The erasure characteristics of the 27C512 are such that erasure begins to occur upon exposure to light with wavelengths shorter than aproximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C512 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C512 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure or the windowless OTP device can be used.

The recommended erasure procedure for the 27C512 is exposure to shortwave ultraviolet light which has a wave length of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15Wsec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm$^2$ power rating. The 27C512 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C512 can be exposed to without damage is 7258W/cm$^2$ (1 week @ 1200µW/cm$^2$). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

Signetics

# 27HC641

## 64K-Bit CMOS PROM (8K× 8)

*Product Specification*

**Military CMOS Memory Products**

### DESCRIPTION

The 27HC641 is a CMOS, high-speed UV erasable, electronically programmed Read Only Memory. It is organized as 8192 words of 8 bits and operates from a single 5 volts +/– 10% power supply. All outputs offer 3-State operation and are fully TTL compatible.

The 27HC641 uses advanced CMOS circuitry which allows operation at bipolar PROM speeds while consuming lower power. The highest degree of protection against latch-up is achieved through epitaxial processing, simplifying the design of electronic equipment which is subject to a high noise environment.

The 27HC641 is available in the industry standard 24-pin Dual-In-Line (DIP) package with the same pin out as most 64K bipolar PROMs, thereby making it easier to upgrade systems currently using higher power bipolar PROMs, and allowing the designer to provide a lower power memory system solution. Also available in a standard 32-Pin LLCC.

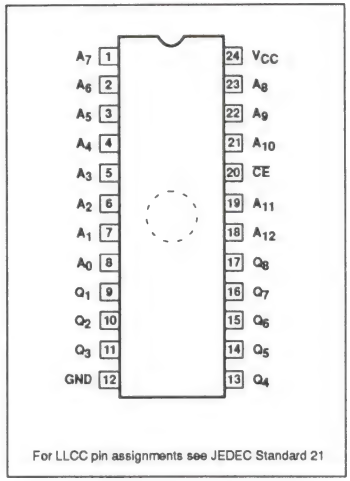
### FEATURES

- **Address access times 55ns and 70ns**
- **Max operating ICC of 110mA**
- **3-State outputs**
- **Direct replacement of Bipolar PROMs**
- **Programmed on industry standard EPROM programmers**
- **Fully TTL compatible**

### APPLICATIONS

- **Prototyping and volume production**
- **High performance memory systems**
- **Sequential controllers**
- **Microprogramming**
- **Random Logic Replacement**

### PIN CONFIGURATION



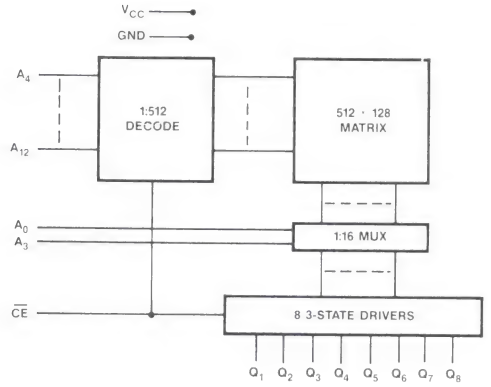

For LLCC pin assignments see JEDEC Standard 21

### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | |
|---|---|---|
| | 55 nsec | 70 nsec |
| 24-Pin 600mil wide Cerdip w/Quartz Window | 27HC641/BJA-55 | 27HC641/BJA-70 |
| 24-Pin Cerdip w/o Window[1] | 27HC641/BXA-55 OT | 27HC641/BXA-70 OT |
| 28-Pin LLCC w/Quartz Window | 27HC641/B3A-55 | 27HC641/B3A-70 |

# 64K–Bit CMOS PROM (8K×8) — 27HC641

## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS[2]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Operating temperature range | –55 to +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $V_I$[3] | Voltage on $\overline{CE}$ pin with respect to GND | –0.5 to +13.5 | V |
| $V_I$[3] | Voltage on any other pin with respect to GND | –0.5 to +7 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | Input voltage High | 2.0 | | VCC + 1 | V |
| $V_{IL}$ | Input voltage Low | –0.1 | | 0.8 | V |

# 64K–Bit CMOS PROM (8K×8) — 27HC641

## DC CHARACTERISTICS $-55° \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{IL}$ | Input leakage current Low | $V_I$ =+0.45V, $V_{CC}$ = MAX | | ±10 | µA |
| $I_{IH}$ | Input leakage current High | $V_I = V_{CC}$, $V_{CC}$ = MAX | | ±10 | µA |
| $I_{OZ}$ | Output current Hi–Z State | $V_O$ = 0.45V, $V_{CC}$ = MAX | | –10 | µA |
| | | $V_O = V_{CC}$, $V_{CC}$ = MAX | | 10 | µA |
| $V_{OL}$ | Output voltage Low | $V_{CC}$ = MIN, $I_{OL}$ = 16mA | | 0.45 | V |
| $V_{OH}$ | Output voltage High | $V_{CC}$ = MIN, $I_{OH}$ = –2mA | 2.4 | | V |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX | | 110 | mA |
| $V_{IK}$ | Input clamp voltage (All input pins except $\overline{CE}$) | $V_I$ = –18mA, $V_{CC}$ = MIN | | –1.2 | V |
| $V_{IK}$ | Input clamp voltage ($\overline{CE}$) | $V_I$ = –12mA, $V_{CC}$ = MIN | | –1.2 | V |
| $I_{OS}$ | Short circuit output current[6] | $V_O$ = 0V, $V_{CC}$ = MAX | –10 | –85 | mA |
| $C_{IN}$ | Input capacitance[4] | $V_{IN}$ = 0V, $V_{CC}$ = NOM | | 10 | pF |
| $C_{OUT}$ | Output capacitance[4] | $V_{OUT}$ = 0V, $V_{CC}$ = NOM | | 15 | pF |

## AC ELECTRICAL CHARACTERISTICS[5] $-55° \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | –55 LIMITS | | –70 LIMITS | | UNIT |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{AA}$ | Address access time | | 55 | | 70 | ns |
| $t_{CE}$ | Chip enable access time | | 35 | | 40 | ns |
| $t_{CD}$ | Output disable time from chip enable | | 35 | | 40 | ns |

## AC ELECTRICALS DURING PROGRAMMING $T_A$ =25° C ± 5°C, $V_{CC}$ = 5V± 5%, $V_{PP}$ = 12.5V ± 0.5V

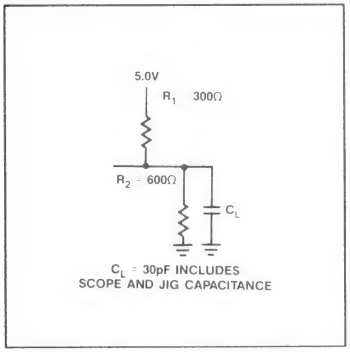
| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $t_W$ | Write pulse width | 10 | | ms |
| $t_R$ | Rise time | 10 | | µs |
| $t_F$ | Fall time | 10 | | µs |
| $t_{AS}$ | Address setup time | 10 | | µs |
| $t_{DS}$ | Data setup time | 10 | | µs |
| $t_{CS}$ | Chip enable setup time | 10 | | µs |
| $t_{AH}$ | Address hold time | 10 | | µs |
| $t_{DH}$ | Data hold time | 10 | | µs |
| $t_{CH}$ | Chip enable hold time | 10 | | µs |

**NOTES:**

1. Erase characteristics do not apply for one time programming (OT).
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
3. Minimum DC input voltage is –0.5V during transitions. The inputs may undershoot to –2.0V for periods less than 20ns.
4. $C_{IN}$ and $C_{OUT}$ are measured initially and after any design changes which may affect capacitance.
5. Test conditions ($C_L$ = 30pF, $R_1$ = 300Ω, and $R_2$ = 600Ω.).
6. Duration of short circuit should not exceed 1 second and short only one output at a time.

# 64K–Bit CMOS PROM (8K×8) 27HC641

## EQUIVALENT AC TEST LOAD CIRCUIT




## ERASURE CHARACTERISTICS

The 27HC641 is erased by exposure to ultraviolet light. The recommended erasure procedure is exposure to short–wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15Wsec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12,000µW/cm$^2$ power rating.

The 27HC641 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27HC641 can be exposed to without damage is 7258Wsec/cm$^2$ (1 week @ 12000µW/cm$^2$). Exposure of this CMOS EPROM to high–intensity UV light for longer periods may cause permanent damage. Some erasure may occur with exposure to light sources having wavelengths shorter than 4000 (Å) such as sunlight or fluorescent light. For maximum system reliability, precautions should be taken by placing opaque labels over the quartz window when used in these environments.

## PROGRAMMING THE 27HC641

Initially, and after each erasure, all bits of the 27HC641 are in an undefined state. Data is introduced by programming "1"s and "0"s into the desired bit locations. Both "1"s and "0"s must be present in the data word to define each bit. The only way to change a bit to the opposite state is by ultraviolet light erasure and programming it to the desired state.

The 27HC641 is in the programming mode when the Output Enable ($\overline{G}$) pin is at 12.5V. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

## INTELLIGENT IDENTIFIER

The intelligent identifier mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27HC641.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line $A_9$ (Pin 22) of the 27HC641. Two bytes may then be read from the device outputs by toggling address line $A_0$ (Pin 8) from $V_{IL}$ to $V_{IH}$.

The $\overline{G}$ and all other address lines must be held at $V_{IL}$ during interrogation.

The identifier information for Signetics 27HC641 is as follows:

When $A_0 = V_{IL}$
data is "Manufacturer" $15_{[HEX]}$
When $A_0 = V_{IH}$
data is "Product" $21_{[HEX]}$

## PROGRAMMING INFORMATION

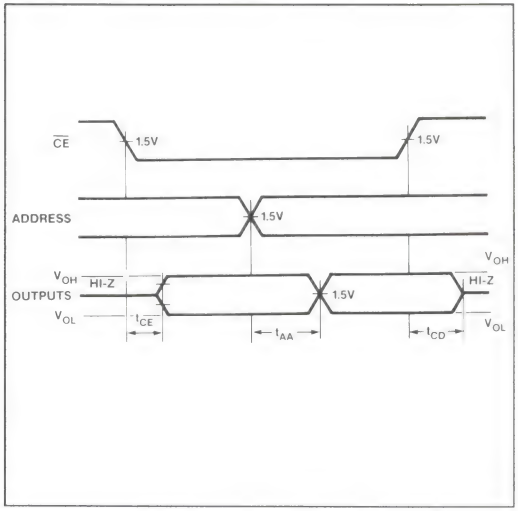
Complete programming system specifications for the Programming Algorithm are available upon request form Signetics Memory Marketing.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of PROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available upon request from Signetics Memory Marketing.

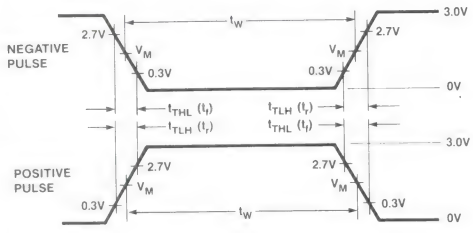
## SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Signetics warranty for programmability extends only to product that has been programmed on certified equipment that has been serviced to the manufacturer's recommendations.

## AC VOLTAGE WAVEFORMS




## VOLTAGE WAVEFORMS




| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| VM | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ≤5ns | ≤5ns |

Signetics

# Section 6
# Standard Products

Military Products

## INDEX


| | | |
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Signetics

# PLHS18P8A

## Programmable AND Array Logic (18×72×8)

*Product Specification*

**Military**
**Standard Products**

### DESCRIPTION

The PLHS18P8A is a two-level logic element consisting of 72 AND gates and 8 OR gates with fusible connections for programming I/O polarity and direction.

All AND gates are linked to 10 inputs (I) and 8 bidirectional I/O lines (B). These yield variable I/O gate configurations via 8 directional control gates, ranging from 18 inputs to 8 outputs.

On-chip T/C buffers couple either True ($I$, $\overline{B}$) or Complement ($\overline{I}$, B) input polarities to all AND gates. The 72 AND gates are separated into 8 groups of 9 each. Each group of 9 is associated with one bidirectional pin. In each group, eight of the AND terms are ORed together, while the ninth is used to establish I/O direction. All outputs are individually programmable via an EX-OR gate to allow implementation of AND/OR or NAND/NOR logic functions.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which will act as open connections.

Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

The PLHS18P8A is field-programmable, allowing the user to quickly generate custom pattern using standard programming equipment.

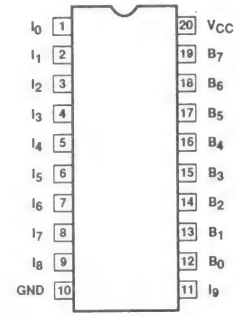
### FEATURES

- **100% functionally compatible with AmPAL18P8A**
- **Field Programmable**
- **10 Inputs**
- **8 bidirectional I/O lines**
- **72 AND gates/product terms – configured into eight groups of nine**
- **Programmable output polarity (3-State output)**
- **I/O propagation delay: 30ns (max)**
- **Power dissipation: 750mW (nominal)**
- **TTL compatible**
- **Verify Lock Fuse**
- **On-chip test features for extensive AC and DC parametric testing**

### APPLICATIONS

- **100% functional replacement for all 20-pin combinatorial PALs**
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

### PIN CONFIGURATION




**For LLCC Pin Assignments see Jedec Standard 21A**

### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 20–Pin Ceramic DIP 300mil-wide | PLHS18P8A/BRA |
| 20–Pin Ceramic LLCC | PLHS18P8A/B2A |
| 20–Pin Ceramic Flat Pack | PLHS18P8A/BSA |

# Programmable AND Array Logic (18×72×8) — PLHS18P8A

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | –0.5 | +7 | $V_{DC}$ |
| $V_I$ | Input voltage range | –0.5 | +5.5 | $V_{DC}$ |
| $V_O$ | Output voltage range | –0.5 | $V_{CC}$MAX | $V_{DC}$ |
| $V_{OUTPRG}$ | Output voltage range (programming) | | +21 | $V_{DC}$ |
| $I_I$ | Input current range | –30 | +5 | mA |
| $I_O$ | Output current range | | +100 | mA |
| $I_{OUTPGR}$ | Output current range (programming) | | +170 | mA |
| $T_{STG}$ | Storage temperature range | –65 | +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High level input voltage[3] | 2.0 | | | V |
| $I_{IL}$ | Low level input voltage[3] | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High level output current | | | –2 | mA |
| $I_{OL}$ | Low level output current | | | 24 | mA |
| $T_A$ | Operating free–air temperature range | –55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = Min, $I_{IN}$ = max | | –0.9 | –1.2 | V |
| $V_{OL}$ | Output low voltage[10] | $V_{CC}$ = min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$[8], $I_{OL}$ = max | | | +0.50 | V |
| $V_{OH}$ | Output high voltage[10] | $V_{CC}$ = min, $I_{OH}$ = 2.0mA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | +2.4 | +3.5 | | V |
| $I_{IL}$ | Input low current | $V_{CC}$ = max, $V_I$ = +0.40V | | –20 | –100 | µA |
| $I_{IH}$ | Input high current | $V_{CC}$ = max, $V_I$ = +2.7V | | | +25 | µA |
| $I_I$ | Input high current | $V_{CC}$ = max, $V_I$ = +5.5V | | | +1.0 | mA |
| $I_{OHZ}$ | Offstate output current high level[7] | $V_{CC}$ = max, $V_{IL}$ = max, $V_{IH}$ = min[8], $V_O$ = +2.7V | | | +100 | µA |
| $I_{OLZ}$ | Offstate output current low level[7] | $V_{CC}$ = max, $V_O$ = +0.40V, $V_{IL}$ = max, $V_{IH}$ = min | | | –250 | µA |
| $I_{SC}$ | Output short circuit current[4,9] | $V_{CC}$ = max, $V_O$ = +0.5V | –30 | –60 | –90 | mA |
| $I_{CC}$ | $V_{CC}$ Supply current[6] | $V_{CC}$ = Max | | 100 | 180 | mA |
| $C_{IN}$ | Input capacitance[5] | $V_{CC}$ = +5V, $V_I$ = 2.0V | | 9 | | pF |
| $C_{OUT}$ | I/O capacitance[5] | $V_{CC}$ = +5V, $V_O$ = 2.0V | | 13 | | pF |

## AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$ R1 = 200Ω, R2 = 390Ω

| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ[2] | Max | |
| $t_{PD}$[11] | Propagation delay | Input ± | Output ± | $C_L$ = 50pF | | 15 | 30 | ns |
| $t_{EA}$[12] | Output enable | Input ± | Output ± | $C_L$ = 50pF | | 15 | 30 | ns |
| $t_{ER}$[12] | Output disable | Input ± | Output ± | $C_L$ = 50pF | | 15 | 30 | ns |

**NOTES:**

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = +25°C.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included. Testing these values requires special equipment.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_O$ = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. These parameters are not tested.
6. $I_{CC}$ is measured with all inputs grounded.
7. On unprogrammed devices, Pins 8 & 9 = 10V. On programmed device, Pin 4 = 0.4V.
8. $V_{IL}$ and $V_{IH}$ only tested on a programmed device.
9. Pin 11 = 10V for testing unprogrammed device.
10. Pin 11 = 0V for testing unprogrammed device.
11. $t_{PD}$ is tested with switch $S_1$ closed and $C_L$ = 50pF.
12. For Tri–state output; output enable times are tested with $C_L$ = 50pF to the 1.5 V level, and $S_1$ is open of high–impedance to High tests and closed for high–impedance to Low tests. High–to–High impedance tests are made to an output voltage of $V_{OH}$ = –0.5V with $S_1$ open, and Low–to–High impedance tests are made to the $V_{OL}$ = +0.5V level with $S_1$ closed.

## VIRGIN STATE

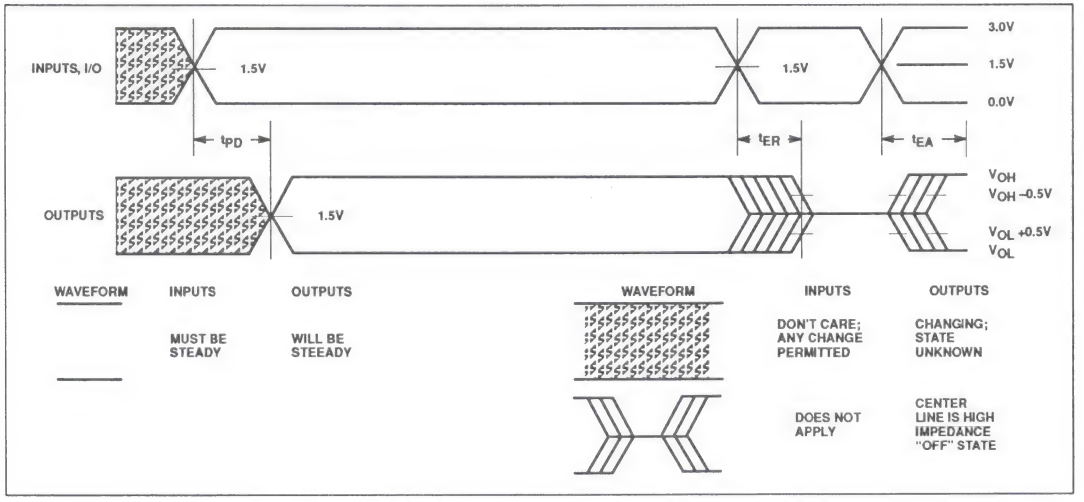
A factory shipped virgin device contains all fusible links open, such that:

1. All outputs are at "H" polarity.
2. All outputs are enabled.
3. All p–terms are enabled.

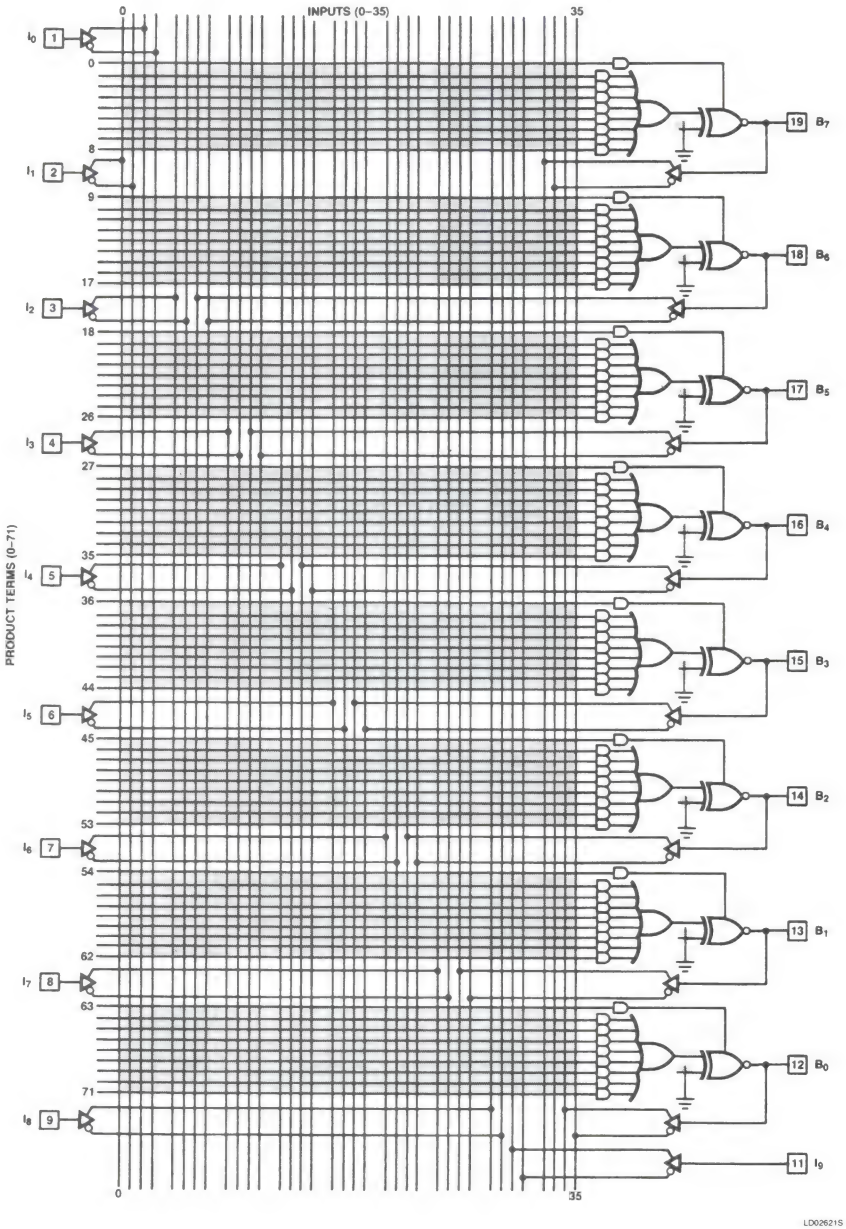
## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{PD}$ | Input to output propagation delay. |
| $t_{ER}$ | Input to output disable (3–State) delay (Output Disable). |
| $t_{EA}$ | Input to Output Enable delay (Output Enable). |

## TIMING DIAGRAM

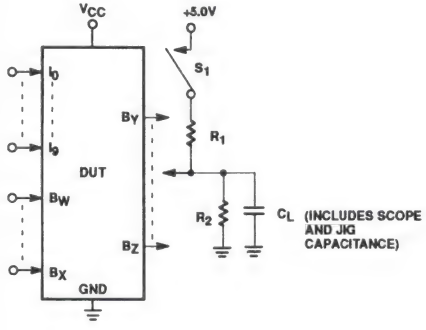


## FPLA LOGIC DIAGRAM

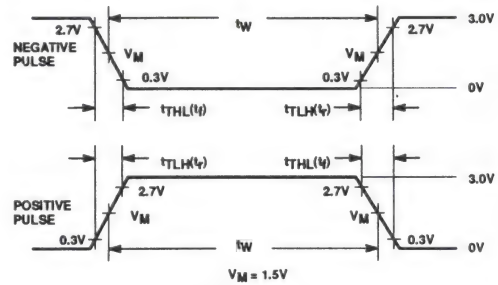



**NOTES:**
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. ⁘ Programmable connections.

## TEST LOAD CIRCUIT




## VOLTAGE WAVEFORM




Input Pulse Definitions

| INPUT PULSE CHARACTERISTICS | | | |
|---|---|---|---|
| Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1MHz | 500ns | ≤5ns | ≤5ns |

Signetics

# PLHS473

## Field–Programmable Logic Array (20×24×11)

**Signetics Programmable Logic**

***Product Specification***

**Military Application Specific Products**

### DESCRIPTION

The PLHS473 is a two level logic device consisting of 24 AND gates and 22 OR gates with fusible link connections for programming I/O polarity and direction. The Signetics state-of-the-art Oxide-Isolated Bipolar process is used to produce performance not yet achieved in devices of this complexity.

All AND gates are linked to 11 input pins, 9 bidirectional I/O pins, and 2 dedicated output pins. The bidirectional pins are controlled via the OR array. Using these features, the PLHS473 can be configured with up to 20 inputs and as many as 11 outputs.

The AND array input buffers provide both the True and Complement of the inputs ($I_X$) and the bidirectional signals ($B_X$) as programmable connections to the AND gates. All 24 AND gates can then be optionally linked to all 22 OR gates (a feature known as Product Term sharing not found in PALs® or most macrocell architectures). The OR array drives 11 output buffers which can be programmed as Active-High for AND-OR functions or Active-Low for AND-NOR functions. In addition, the I/O configuration of each bidirectional pin is individually controlled by a sum-of-products (AND-OR) function which may also contain any of the 24 AND gate outputs. This allows dynamic I/O configuration of all 9 bidirectional pins.

The PLHS473 contains two new features of significance. A code verification lock has been incorporated to improve user security. The addition of three test columns and one test row enables the user to test the device in an unprogrammed state.

The PLHS473 is field programmable using Vertical Avalanche Migration Programmed (VAMP™) fuses to program the cells. This enables the generation of custom logic patterns using standard programming equipment..

Order codes for this device are contained in the pages following.

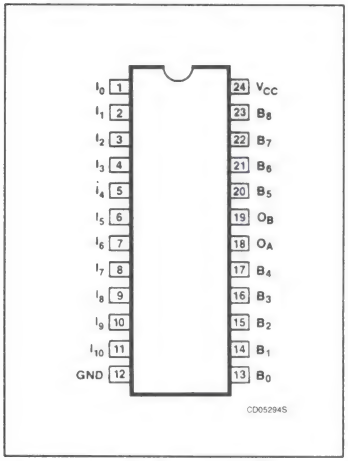
### FEATURES

- **Field-Programmable**
- **11 dedicated inputs**
- **2 dedicated outputs**
- **9 bidirectional I/O lines**
- **24 product terms**
- **22 OR gates**
- **I/O direction decoded in OR array**
- **Output Enable decoded in OR array**
- **I/O propagation delay: 20ns (max)**
- **Input loading: -100μA (max)**
- **Power dissipation: 700mW (typ)**
- **Security fuse**
- **Testable in unprogrammed state**
- **Programmable as 3-state or Open-Collector outputs**
- **TTL compatible**

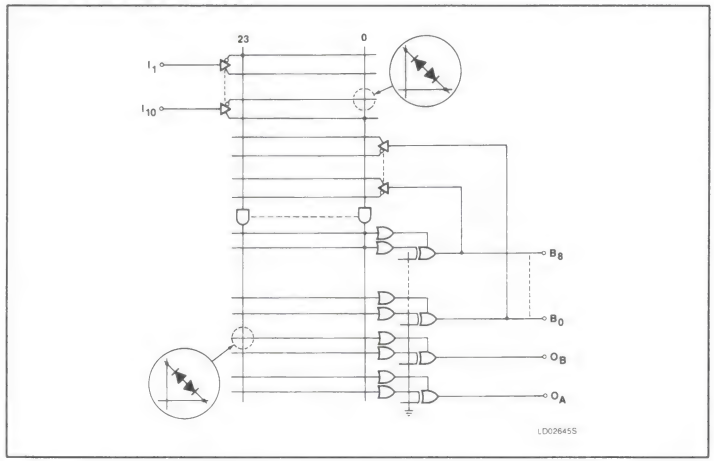
### APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

### PIN CONFIGURATION



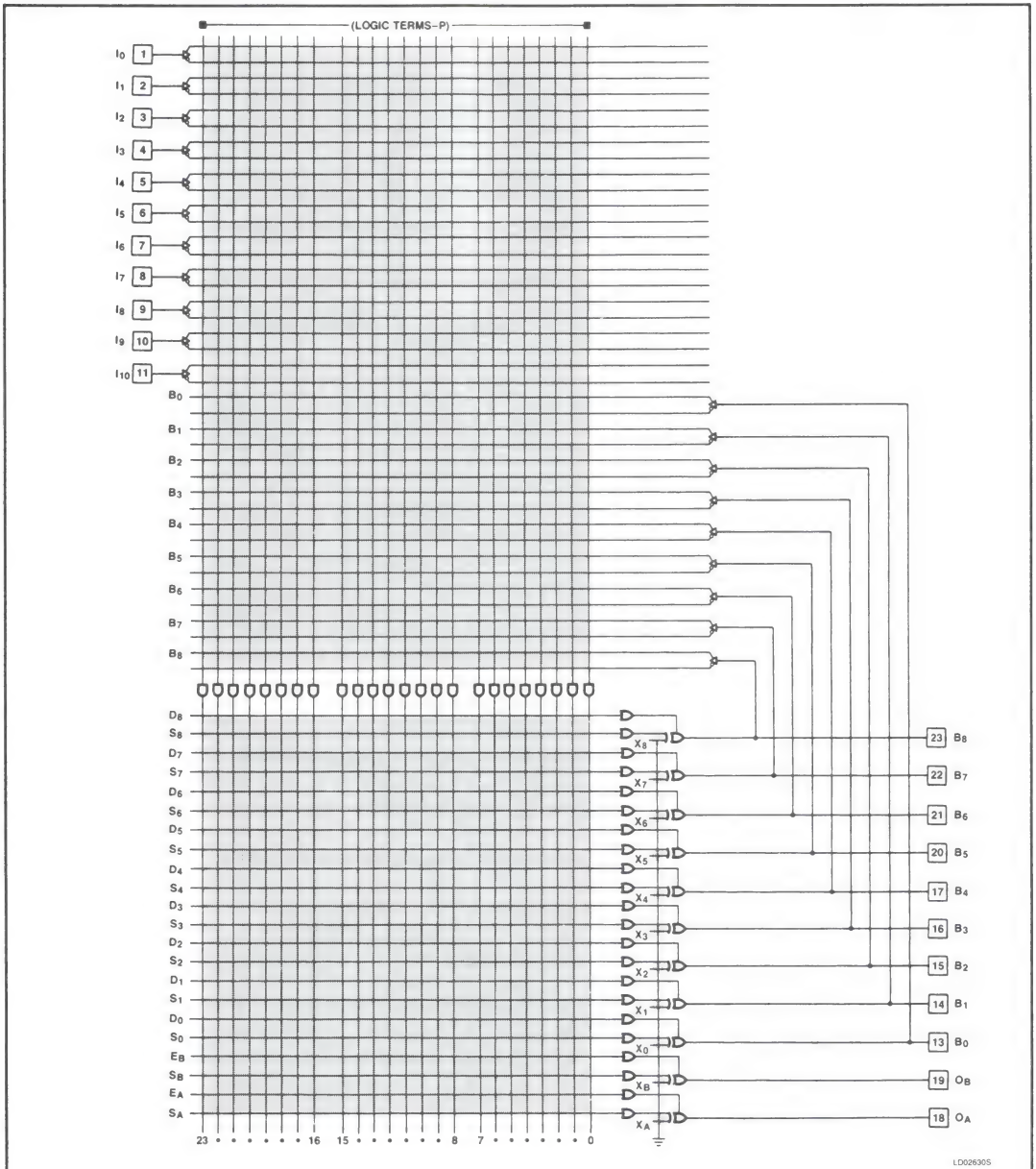

### FUNCTIONAL DIAGRAM




PAL is a registered trademark of Monolithic Memories, Inc., a wholly owned subsidiary of Advanced Micro Devices, Inc.

# Field–Programmable Logic Array (20×24×11) PLHS473

## FPLA LOGIC DIAGRAM




**NOTES:**
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. All unprogrammed or virgin "OR" gate locations are pulled to logic "0".
3. ● Programmable connection.

# Field–Programmable Logic Array (20×24×11) — PLHS473

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 24–pin Ceramic DIP 300mil–wide | PLHS473/BLA |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | | +7 | $V_{DC}$ |
| $V_{IN}$ | Input voltage | | +5.5 | $V_{DC}$ |
| $V_{OUT}$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_{IN}$ | Input currents | –30 | +30 | mA |
| $I_{OUT}$ | Output currents | | +100 | mA |
| $T_{STG}$ | Storage temperature range | –65 | +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$[12] | High level input voltage | 2.2 | | | V |
| $V_{IL}$[12] | Low level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High level output current | | | –2 | mA |
| $I_{OL}$ | Low level output current | | | 15 | mA |
| $T_A$ | Operating free–air temperature range | –55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| $V_{IK}$ | Input clamp voltage[3,4] | $V_{CC}$ = Min, $I_{IN}$ = $I_{IK}$ | | –0.8 | –1.2 | V |
| $V_{OL}$ | Output Low voltage[3,5] | $V_{CC}$ = Min, $V_{IL}$ = Max, $V_{IH}$ = Min<br>$I_{OL}$ = Max | | | 0.5 | V |
| $V_{OH}$ | Output High voltage[3,6] | $I_{OH}$ = Min | 2.4 | | | V |
| $I_{IL}$ | Input Low current | $V_{CC}$ = Max<br>$V_{IN}$ = 0.45V | | | –100 | µA |
| $I_{IH}$ | Input High current | $V_{IN}$ = 5.5V | | | 40 | µA |
| $I_{OHZ}$ | Output Tri–state current[10] | $V_{CC}$ = Max, $V_{OUT}$ = 5.5V | | | 40 | µA |
| $I_{OLZ}$ | Output Tri–state current[10] | $V_{CC}$ = Max, $V_{OUT}$ = 0.45V | | | –100 | µA |
| $I_{OS}$ | Output short circuit[4,6,7] | $V_{CC}$ = Max, $V_{OUT}$ = 0V | –15 | | –85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[8] | $V_{CC}$ = Max | | 140 | 155 | mA |
| $I_{IN}$ | Input capacitance[11] | $V_{CC}$ = 5V<br>$V_{IN}$ = 2.0V | | 8 | 12 | pF |
| $C_B$ | I/O capacitance[11] | $V_B$ = 2.0V | | 15 | 19 | pF |

# Field–Programmable Logic Array (20×24×11) — PLHS473

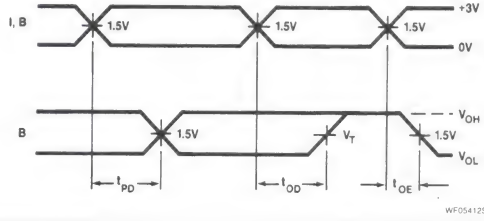
## AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | LIMITS Min | LIMITS Typ | LIMITS Max | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Propagation delay | Output± | Input± | $C_L$ = 50pF | | 25 | 30 | ns |
| $t_{OE}$ | Output enable | Output– | Input± | $C_L$ = 50pF | | 25 | 30 | ns |
| $t_{OD}$ | Output disable[9,11] | Output+ | Input± | $C_L$ = 5pF | | 25 | 30 | ns |

**NOTES:**

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with Pins 1 – 5 = 0V, Pins 6, 8 = 4.5V, and Pins 7, 9 – 11 = 10V.
6. Same conditions as Note 5, except Pin 9 = 4.5V.
7. Duration of short circuit should not exceed 1 second.
8. $I_{CC}$ is measured with all inputs and bidirectional pins at 4.5V. Part in Virgin State.
9. Measured at $V_T = V_{OL} + 0.5V$, and with $C_L$ = 30pF.
10. Leakage values are a combination of input and output leakage.
11. Guaranteed, but not tested.
12. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.

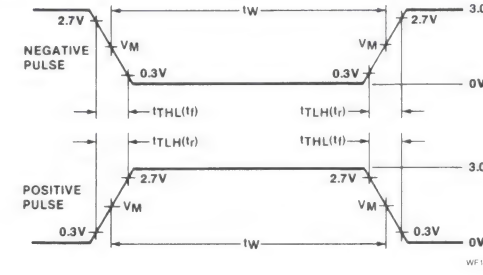
## TIMING DIAGRAM




## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{PD}$ | Propagation delay between input and output. |
| $t_{OD}$ | Delay between input change and when output is off (Hi–Z or High). |
| $t_{OE}$ | Delay between input change and when output reflects specified output level. |

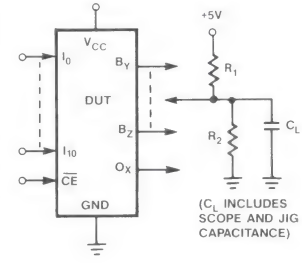
## VOLTAGE WAVEFORM




**Input Pulse Definitions**

| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| $V_M$ | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ≤ 5ns | ≤ 5ns |

## TEST LOAD CIRCUIT




NOTE:
$R_1$ = 470Ω, $R_2$ = 1kΩ, $C_L$ = 50pF

# Field–Programmable Logic Array (20×24×11) — PLHS473

## LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR/EX–OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this table, the logic state of variables I, P and B, associated with each SumTerm S is assigned a symbol which results in the proper fusing pattern of corresponding links, defined as follows:

## LOGIC FUNCTION

**TYPICAL PRODUCT TERM:**

$Pn = A \bullet \overline{B} \bullet C \bullet D \bullet \ldots$

**TYPICAL LOGIC FUNCTION:**
**AT OUTPUT POLARITY = H**

$Z = P0 + P1 + P2 \ldots$

**AT OUTPUT POLARITY = L**

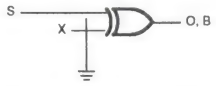
$\overline{Z} = \overline{P0} + \overline{P1} + \overline{P2} + \ldots$

$Z = \overline{P0} \bullet \overline{P1} \bullet \overline{P2} \bullet \ldots$

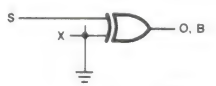
**NOTES:**

1. For each of the 11 outputs, either function Z (Active–High) or $\overline{Z}$ (Active–Low) is avialable, but not both. The desired output polarity is programmed via the Ex–OR gates.
2. Z, A, B, C, etc., are user defined connections to fixed inputs (I), fixed output pins (O) and bidirectional pins (B).

## OUTPUT POLARITY – (O, B)

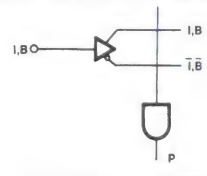



| ACTIVE LEVEL | CODE |
|---|---|
| LOW[13] (INVERTING) | L |



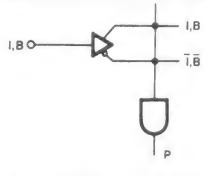

| ACTIVE LEVEL | CODE |
|---|---|
| HIGH (NON-INVERTING) | H |

## "AND" ARRAY – (I, B)



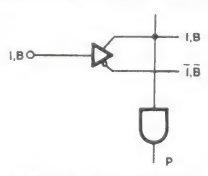

| STATE | CODE |
|---|---|
| DON'T CARE[13] | – |

TC02603S



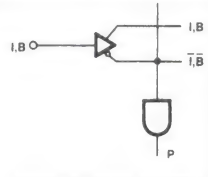

| STATE | CODE |
|---|---|
| INACTIVE[14] | O |

TC02634S




| STATE | CODE |
|---|---|
| I, B | H |

TC02610S




| STATE | CODE |
|---|---|
| $\overline{I}$, $\overline{B}$ | L |

TC02620S

## "OR" ARRAY – (O, B)

| $P_n$ STATUS | CODE |
|---|---|
| INACTIVE[13] | • |

TC02583S

| $P_n$ STATUS | CODE |
|---|---|
| ACTIVE | A |

TC02591S

## VIRGIN STATE

A factory shipped virgin device contains all fusible links open, such that:

1. All outputs at "L" polarity.
2. All $P_n$ terms are enabled. (Don't Care).
3. All $P_n$ terms are inactive on all outputs.

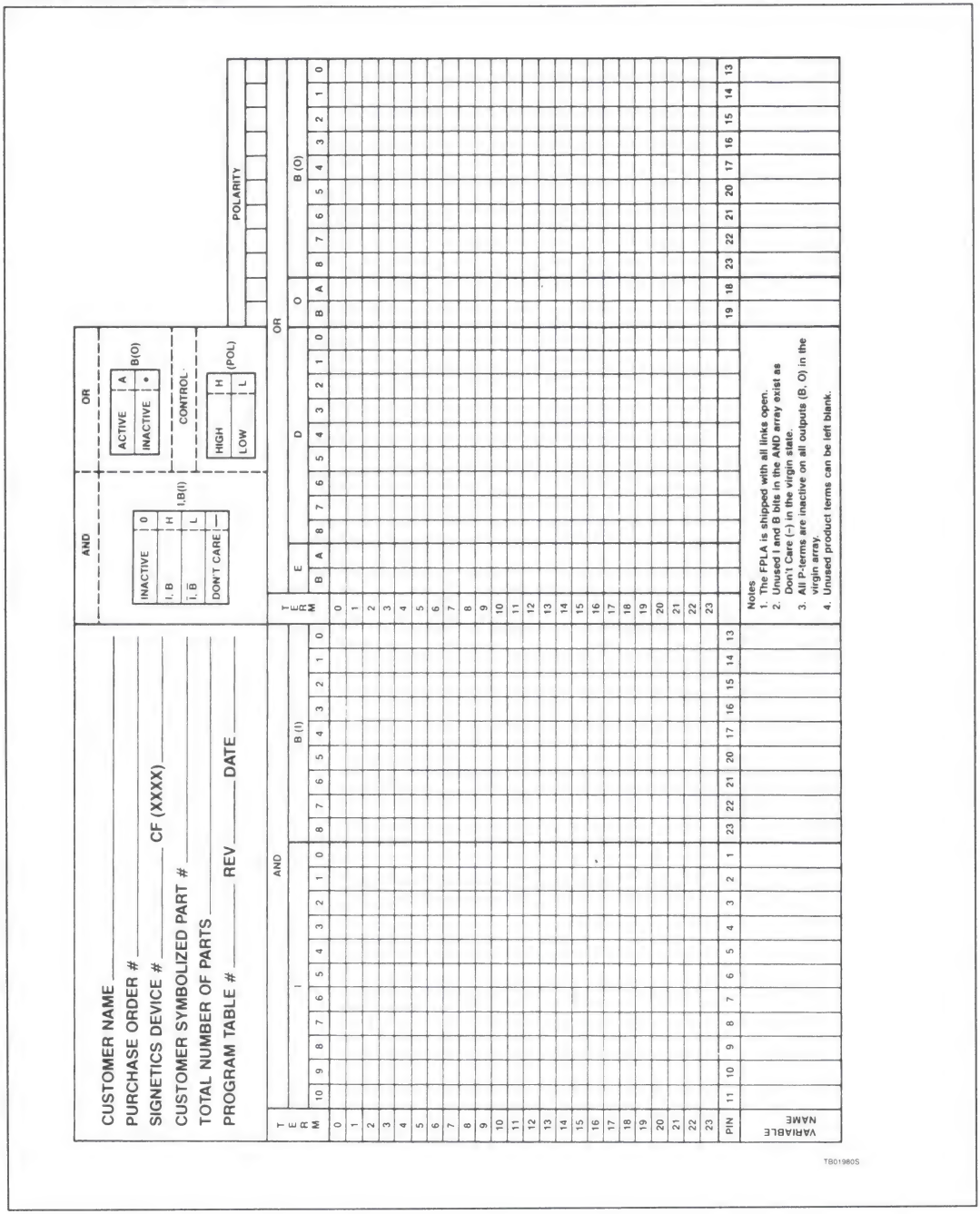
**NOTES:**

13. This is the initial unprogrammed state of all links.
14. Any gate $P_n$ will unconditionally inhibited if the true and complement of either input (I or B) are both programmed for a connection.

# Field–Programmable Logic Array (20×24×11)

# PLHS473

## FPLA PROGRAM TABLE



Signetics

# PLHS501

## Programmable Macro Logic
## Random Logic Unit (32×72×24)

*Product Specification*

**Military Application Specific Products**

### DESCRIPTION

The PLHS501 is a member of the Signetics Programmable Macro Logic family. PML is unique in its capability of performing other than two level logic functions without incurring I/O buffer delays. This allows the logic or system designer to imbed logical operations or macro structures within the framework of the I/O pins. Since the imbedded functions are independent of the delays created by the I/O buffers, they can be performed at speeds lesser architectures cannot reproduce.

The technique used to perform this operation is a NAND foldback network which allows the direct interconnection of any number of logic nodes within the single fuse matrix. Macros can be formed and then interconnected to the I/O structure. In addition, single-level and multi-level logic can be performed at speeds which reflect only the logic path utilized. Therefore, a single-level logic function has a very short path through the device. Additional levels incur only one NAND foldback delay per level. This delay is less than the combined delay created by previous generations of devices which stipulate that the logic signal must pass through I/O buffers after one or two levels of logic are performed.

The PLHS501 is fabricated with Signetics ZA Oxide-Isolated Bipolar Process. ZA utilizes Vertical Avalanche Migration Programmed (VAMP) fuses as programming elements. These fuses provide high programming yield and reliability. Proprietary onboard test circuitry allows the PLHS501 to be thoroughly tested prior to programming.

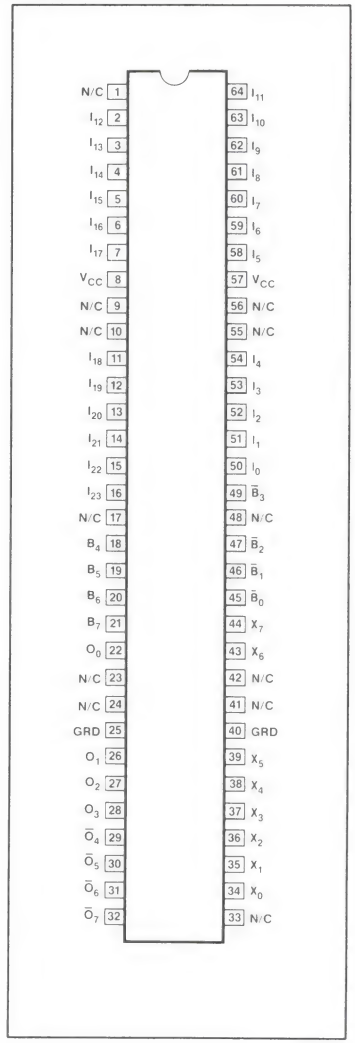
### FEATURES

- Signetics NAND foldback architecture
- Field-Programmable
- 24 dedicated inputs
- Fixed and programmable output buffers
  - 8 I/O buffers
  - 8 EX-OR buffers
  - 4 active-Low buffers
  - 4 active-High buffers
- 72 internal NAND foldback terms
- Supported by AMAZE Development System
- Testable in unprogrammed state
- Verify Lock Fuse
- TTL compatible
- Power dissipation: 1.25W (typ)
- Logic delay times
  - Single-level = 35ns (max)
  - Two-level = 45ns (max)
  - Internal NAND delay = 10ns (max)

### ARCHITECTURE

- 24 dedicated inputs: $I_0$ - $I_{23}$
- 4 active-High I/Os with individual enable: $B_4$ - $B_7$
- 4 active-Low I/Os with individual fused enable: $\overline{B}_0$ - $\overline{B}_3$
- 2 active-High output pairs; each pair with common enable: $O_0$ - $O_3$
- 2 active-Low output pairs; each pair with common enable: $\overline{O}_4$ - $\overline{O}_7$
- 4 Ex-OR output pairs; each pair with common enable: $X_0$ - $X_7$
- 72 internal NAND foldback terms

### PIN CONFIGURATION



# Programmable Macro Logic
# Random Logic Unit (32×72×24)

# PLHS501

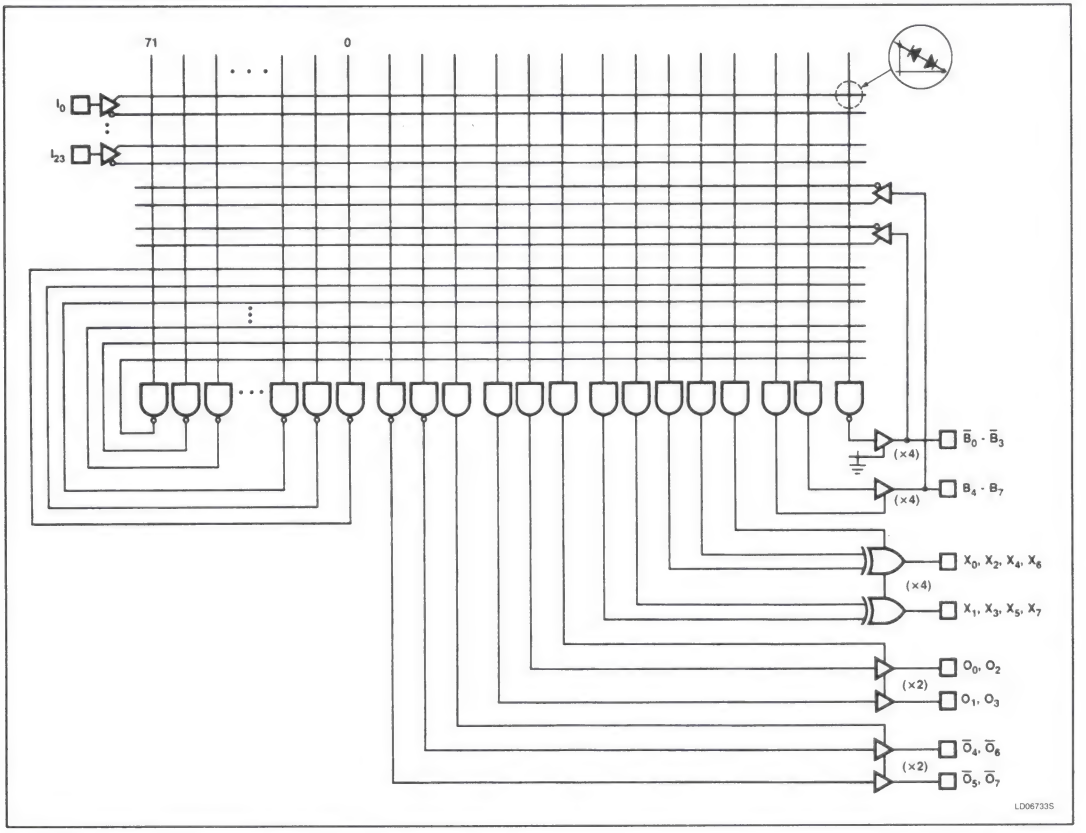
## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 64–Pin Ceramic DIP | PLHS501/BXA |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage range | –0.5V to +7.0 | V |
| $V_I$ | Input voltage range | –0.5V to +5.5 | V |
| $I_I$ | Input current range | –30 to +30 | mA |
| $V_O$ | Voltage range applied to output in High output state | –0.5 to +$V_{CC}$ | V |
| $I_O$ | Current range applied to output in Low output state | 100 | mA |
| $T_A$ | Operating temperature range | –55 to +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

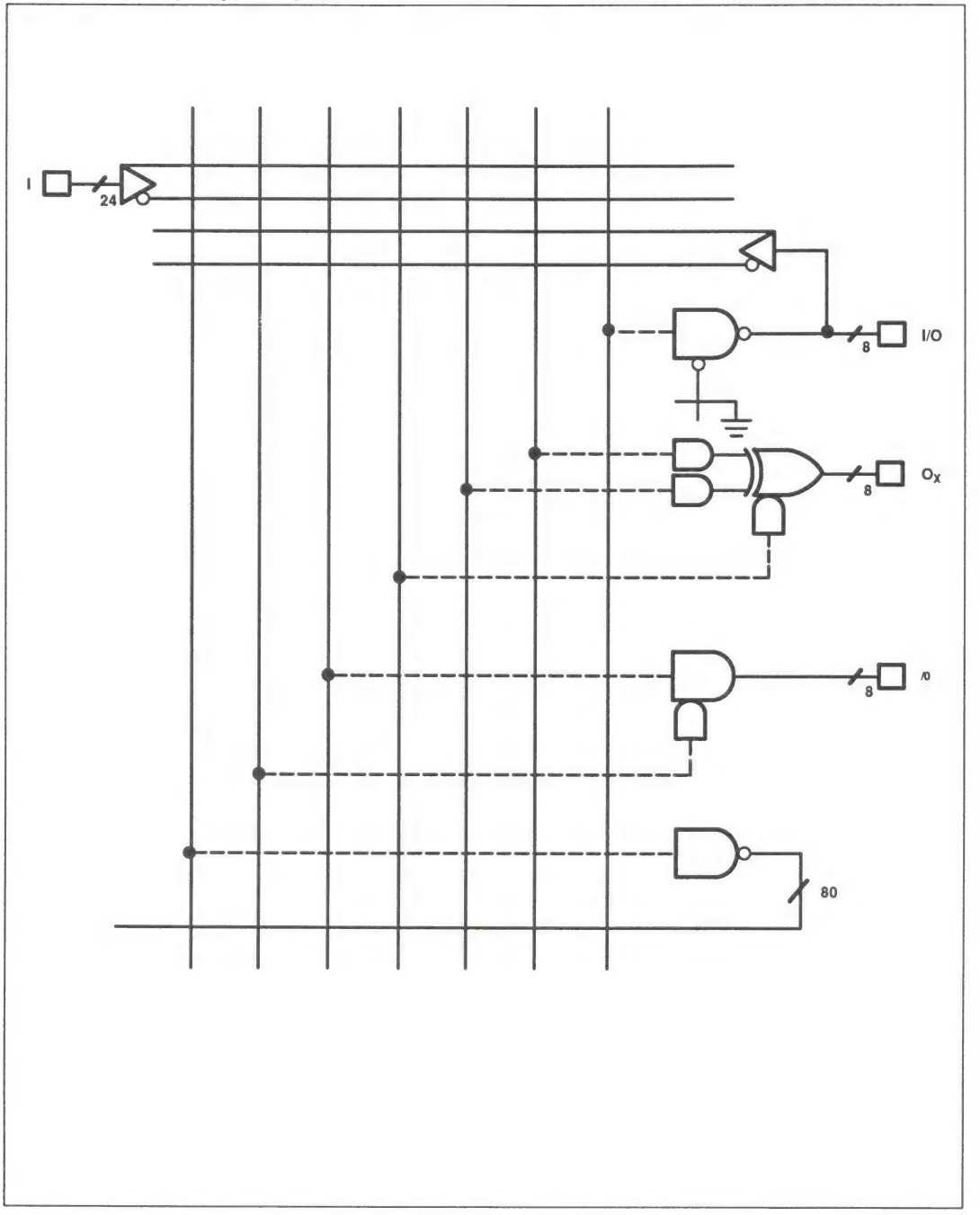
## FUNCTIONAL DIAGRAM



# Programmable Macro Logic
# Random Logic Unit (32×72×24)

**PLHS501**

## LOGIC DIAGRAM (Compressed)



# Programmable Macro Logic
# Random Logic Unit (32×72×24)

# PLHS501

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| **Input Voltage[2]** | | | | | | |
| $V_{IL}$ | Low | $V_{CC}$ = Min | | | 0.8 | V |
| $V_{IH}$ | High | $V_{CC}$ = Max | 2.0 | | | V |
| $V_{IC}$ | Clamp[3,4] | $V_{CC}$ = Min, $I_{IN}$ = −18mA | | −0.8 | −1.2 | V |
| **Output voltage** | | | | | | |
| | | $V_{CC}$ = Min | | | | |
| $V_{OL}$ | Low[3,5] | $I_{OL}$ = 10mA | | | .5 | V |
| $V_{OH}$ | High[3,6] | $I_{OH}$ = −2mA | 2.4 | | | V |
| **Input current** | | | | | | |
| | | $V_{CC}$ = Max | | | | |
| $I_{IL}$ | Low | $V_{IN}$ = 0.4V | | | −100 | µA |
| $I_{IH}$ | High | $V_{IN}$ = 5.5V | | | 40 | µA |
| **Output current** | | | | | | |
| | | $V_{CC}$ = Max | | | | |
| $I_{O(OFF)}$ | Hi–Z state[10] | $V_{OUT}$ = 5.5V | | | 80 | µA |
| | | $V_{OUT}$ = 0.4V | | | −140 | |
| $I_{OS}$ | Short circuit[4,6,7] | $V_{OUT}$ = 0V | −15 | | −85 | mA |
| $I_{CC}$ | $V_{CC}$ supply circuit[8] | $V_{CC}$ = Max | | 225 | 295 | mA |
| **Capacitance** | | | | | | |
| | | $V_{CC}$ = 5V | | | | |
| $I_{IN}$ | Input | $V_{IN}$ = 2.0V | | 8 | | pF |
| $C_B$ | I/O | $V_{OUT}$ = 2.0V | | 15 | | pF |

## AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$, $R_1 = 470\Omega$, $R_2 = 1K\Omega$

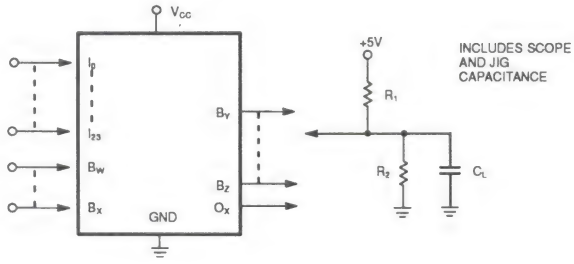
| SYMBOL | PARAMETER | | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | TO | FROM | | Min | Typ[2] | Max | |
| $t_{PD1}$ | Output ± | Input ± | $C_L$ = 50pF | | | 35 | ns |
| $t_{PD2}$ | Output ± | Input ± | | | | 35 | ns |
| $t_{PD3}$ | Output ± | Input ± | | | | 35 | ns |
| $t_{PD4}$[11] | Output ± | Input ± | | | | 45 | ns |
| $t_{PD5}$[11,12] | Output ± | Input ± | | | | 45 | ns |
| $t_{PD6}$[11,12] | Output ± | Input ± | | | | 45 | ns |
| $t_{PD7}$[12] | Internal | | | | 8 | | ns |
| $t_{OE}$ | Output − | Input ± | | | | 40 | ns |
| $t_{OD}$[9] | Output + | Input ± | | | | 40 | ns |

# Programmable Macro Logic
# Random Logic Unit (32×72×24)

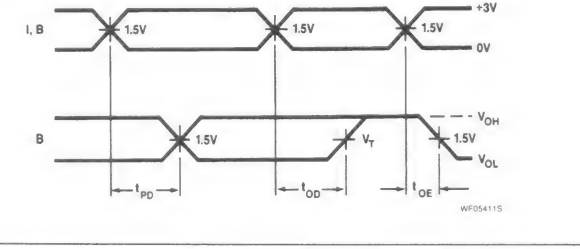
# PLHS501

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. For Pins 18–22, 26–32 and 45–47, 49, $V_{OL}$ is measured with Pins 5 and 50 = 9.5V, Pin 52 = 0V and Pins 51 and 53 = 4.5V. For Pins 34–39 and 43–44, $V_{OL}$ is measured under same conditions EXCEPT Pin 53 = 0V.
6. $V_{OH}$ is measured with Pins 5 and 50 = 9.5V, Pins 51 and 52 = 4.5V and Pin 53 = 0V.
7. Duration of short circuit should not exceed 1 second.
8. $I_{CC}$ is measured with all dedicated inputs at 0V and bidirectional and output pins open.
9. Measured at $V_T = V_{OL} + 0.5V$, $V_{OH} - 0.5V$.
10. Leakage values are a combination of input and output leakage.
11. Limits are guaranteed with internal feedback buffers simultaneously switching cumulative maximum of eight outputs.
12. Only tested on a programmed device if applicable.

## TEST LOAD CIRCUITS




## TIMING DIAGRAMS




## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{PD1}$ | Input to Output delay, one pass, through X outputs |
| $t_{PD2}$ | Input to Output delay, one pass, through $\overline{B}$ outputs |
| $t_{PD3}$ | Input to Output delay, one pass, through O, $\overline{O}$ and B outputs |
| $t_{PD4}$ | Input to Output delay, two passes, through X outputs |
| $t_{PD5}$ | Input to Output delay, two passes, through $\overline{B}$ outputs |
| $t_{PD6}$ | Input to Output delay, two passes, through O, $\overline{O}$ and B outputs |
| $t_{PD7}$ | Feedback delay per internal NAND function performed |
| $t_{OD}$ | Delay between output change and when output is off (Hi–Z or High) |
| $t_{OE}$ | Delay between input change and when the output reflects specified output level |

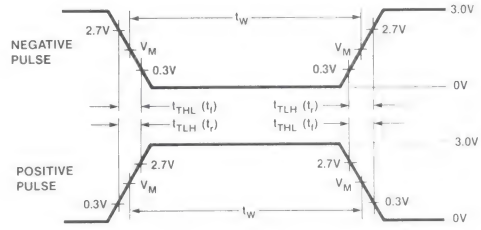
## VIRGIN STATE

A factory shipped virgin device contains all fusible links open, such that:
1. All product terms are enabled.
2. All bidirectional (B) pins are outputs.
3. All outputs are enabled.
4. All outputs are active–High **except**
   $\overline{B}_0 - \overline{B}_3$ (fusible I/O) and $\overline{O}_4 - \overline{O}_7$ which are active–Low.

# Programmable Macro Logic
# Random Logic Unit (32×72×24)

# PLHS501

## VOLTAGE WAVEFORMS




| INPUT PULSE CHARACTERISTICS | | | |
|---|---|---|---|
| Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1MHz | 500ns | ≤2.5ns | ≤2.5ns |

Signetics

# PLS159A

## Field-Programmable Logic Sequencer (16×45×12)

*Product Specification*

**Military Application Specific Products**

### DESCRIPTION

The PLS159A is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "foldback" inverting buffer and control gate $F_C$. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). There are 8 dedicated inputs. These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), 4 bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

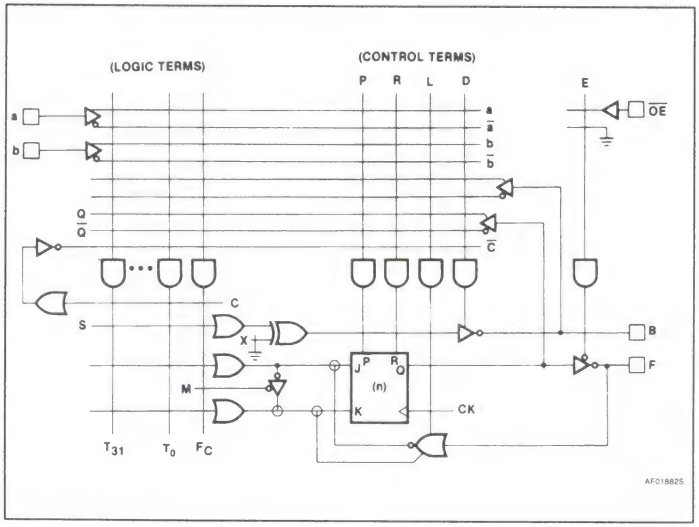
### FEATURES

- High-speed version of PLS159
- Field-programmable (NI-Cr link)
- $F_{MAX}$ = 16MHz
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J-K, T, or D-type flip-flops
- Power-on reset feature on all flip-flops ($F_n$ = 1)
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge triggered clock
- Input loading: -100μA (max)
- Power dissipation: 750mW (typ)
- TTL Compatible
- 3-State outputs

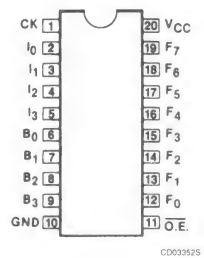
### APPLICATIONS

- Random sequential logic
- Synchronous Up/Down counters
- Shift Registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

### FUNCTIONAL DIAGRAM




### PIN CONFIGURATION



# Field-Programmable Logic Sequencer (16×45×12) — PLS159A

## ORDERING INFORMATION

| PACKAGE | ORDER CODE |
|---|---|
| 24–Pin Ceramic Dip 300mil–wide | PLS159A/BRA |

On–chip T/C buffers couple either True (I, B, Q) or complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates.One group of AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX–OR gates for implementing AND–OR or AND–NOR logic functions. Another group drives the J–K inputs of all flip–flops, as well as asynchronous Preset and Reset lines (P, R).

All flip–flops are positive edge–triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS159A is field–programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

## VIRGIN STATE

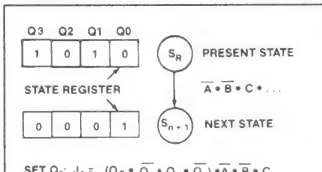
The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip–flops are in D–mode unless otherwise programmed to J–K only or J–K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

## CAUTION: PLS159A PROGRAMMING ALGORITHM

The programming voltage required to program the PLS159A is higher (17.5V) than that required to program the PLS159 (14.5V). Consequently, the PLS159 programming algorithm will not program the PLS159A. Please exercise caution when accessing programmer device codes to ensure that the correct algorithm is used.

## LOGIC FUNCTION




SET $Q_0$: $J_0 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_0 = 0$

RESET $Q_1$: $J_1 = 0$

$K_1 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

HOLD $Q_2$: $J_2 = 0$

$K_2 = 0$

TOGGLE $Q_3$: $J_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

$K_3 = (Q_3 \bullet \overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$

**NOTE:**
Similar logic functions are applicable for D and T mode flip–flops.

## FLIP–FLOP TRUTH TABLE

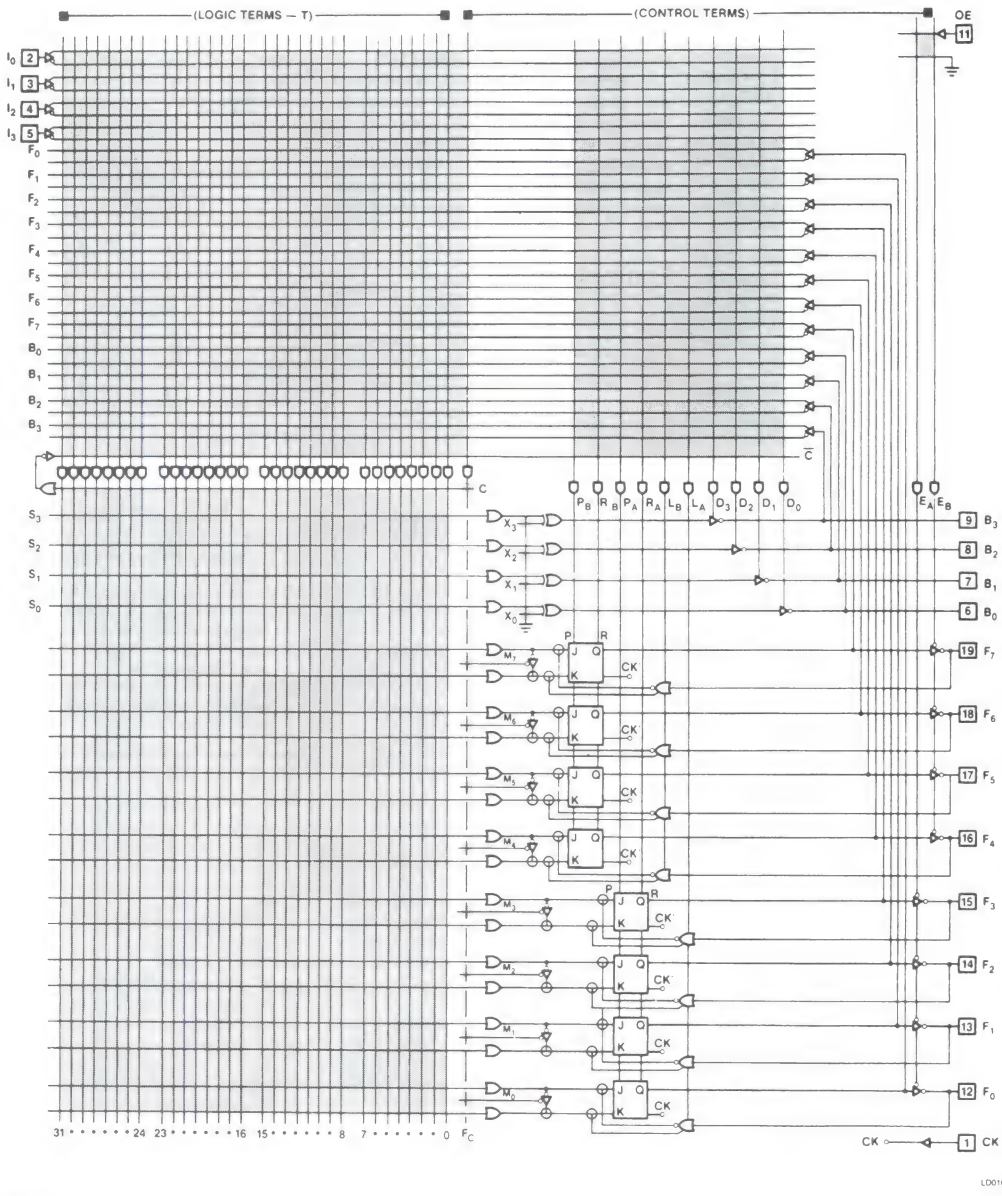
| $\overline{OE}$ | L | CK | P | R | J | K | Q | F |
|---|---|---|---|---|---|---|---|---|
| H | | | | | | | | Hi–Z |
| L | X | X | L | X | X | X | L | H |
| L | X | X | H | L | X | X | H | L |
| L | X | X | L | H | X | X | L | H |
| L | L | ↑ | L | L | L | L | Q | $\overline{Q}$ |
| L | L | ↑ | L | L | L | H | L | H |
| L | L | ↑ | L | L | H | L | H | L |
| L | L | ↑ | L | L | H | H | $\overline{Q}$ | Q |
| H | H | ↑ | L | L | L | H | L | H* |
| H | H | ↑ | L | L | H | L | H | L* |
| +10V | X | ↑ | X | X | L | H | L | H** |
| +10V | X | ↑ | X | X | H | L | H | L** |

**NOTES:**

1. Positive Logic:
   $J–K = T_0 + T_1 + T_2 + \ldots + T_{31}$
   $T_n = \overline{C} \bullet (I_0 \bullet I_1 \bullet I_2 \ldots) \bullet (Q_0 \bullet Q_1 \ldots) \bullet (B_0 \bullet B_1 \ldots)$
2. ↑ denotes transition for Low to High level.
3. X = Don't care
4. * = Forced at $F_n$ pin for loading J–K flip–flop in I/O mode. L must be enabled, and other active $T_R$ disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at $F_n$ pin to load J/K flip–flop independent of program code (Diagnostic mode). 3–State B outputs.

# Field–Programmable Logic Sequencer (16×45×12) PLS159A

## FPLS LOGIC DIAGRAM




**NOTES:**
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ⊗ Programmable connection.

# Field-Programmable Logic Sequencer (16×45×12) PLS159A

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | | +7 | $V_{DC}$ |
| $V_I$ | Input voltage | | +5.5 | $V_{DC}$ |
| $V_O$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_I$ | Input current | –30 | +30 | mA |
| $I_O$ | Output current | | +100 | mA |
| $T_{STG}$ | Storage temperature range | –65 | +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMIT | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IN}$[9] | High level Input voltage | 2.2 | | | V |
| $V_{IL}$[9] | Low level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High level output current | | | –2 | mA |
| $I_{OL}$ | Low level output current | | | 10 | mA |
| $T_A$ | Operation free–air temperature range | –55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER[3] | TEST CONDITIONS[3] | LIMIT[3] | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = Min, $I_I$ = Max | | –0.8 | –1.2 | V |
| $V_{OH}$ | Output High voltage | $V_{CC}$ = Min, $I_{OH}$ = Max | 2.4 | | | V |
| $V_{OL}$ | Output Low voltage | $V_{CC}$ = Min, $I_{OL}$ = Max | | 0.35 | 0.5 | V |
| $I_{IH}$ | Input High current | $V_{CC}$ = Max, $V_I$ = 5.5V | | <1 | 40 | µA |
| $I_{IL}$ | Input Low current | $V_{CC}$ = Max, $V_I$ = 0.45V | | –10 | –100 | µA |
| $I_{OHZ}$ | OFF–State output[5,8] Current High | $V_{CC}$ = Max, $V_O$ = 5.5V | | | 80 | µA |
| $I_{OLZ}$ | OFF–State output[5,8] Current High | $V_{CC}$ = Max, $V_O$ = 0.45V | | | –140 | µA |
| $I_{OS}$ | Short circuit output current[4,6] | $V_{CC}$ = Max, $V_O$ = 0V | –15 | | –85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[7] | $V_{CC}$ = Max | | 150 | 190 | mA |
| $C_{IN}$ | Input capacitance[15] | $V_{CC}$ = 5.0V, $V_I$ = 2.0V | | 8 | 13 | pF |
| $C_{OUT}$ | Output capacitance[15] | $V_{CC}$ = 5.0V, $V_O$ = 2.0V | | 15 | 20 | pF |

# Field-Programmable Logic Sequencer (16×45×12) PLS159A

## AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

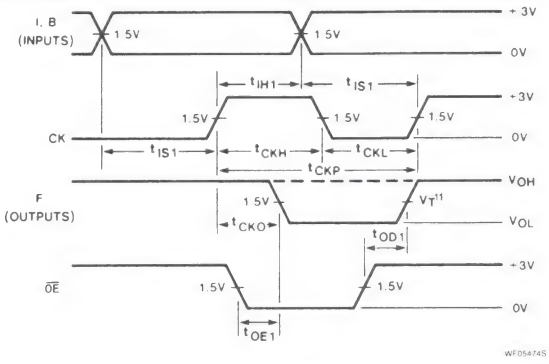
| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min[13] | Typ[2] | Max | |
| **Pulse Width** | | | | | | | | |
| $t_{CKH}$ | Clock high[10] | CK– | CK+ | $C_L$ = 50pF | 20 | 15 | | ns |
| $t_{CKL}$ | Clock low | CK+ | CK– | $C_L$ = 50pF | 20 | 15 | | ns |
| $t_{CKP}$ | CLK min Period ($t_{IS1} + t_{CKO}$) | CK+ | CK+ | $C_L$ = 50pF | 60 | 55 | | ns |
| $t_{PRH}$ | Preset/Reset pulse | (I, B)+ | (I, B)– | $C_L$ = 30pF | 35 | 30 | | ns |
| **Setup Time** | | | | | | | | |
| $t_{IS1}$ | Input | CK+ | (I, B)± | $C_L$ = 50pF | 35 | 30 | | ns |
| $t_{IS2}$ | Input (through $F_n$) | CK+ | F± | $C_L$ = 50pF | 15 | 10 | | ns |
| $t_{IS3}$ | Input (through Complement Array)[12,14] | CK+ | (I, B)± | $C_L$ = 50pF | 55 | 45 | | ns |
| **Hold Time** | | | | | | | | |
| $t_{IH1}$ | Input | CK+ | (I, B)± | $C_L$ = 50pF | 0 | –5 | | ns |
| $t_{IH2}$ | Input (through $F_n$)[14] | CK+ | F± | $C_L$ = 50pF | 15 | 10 | | ns |
| **Propagation Delay** | | | | | | | | |
| $t_{CKO}$ | Clock | F± | CK+ | $C_L$ = 50pF | | 15 | 25 | ns |
| $t_{OE1}$ | Output enable[14] | F– | $\overline{OE}$– | $C_L$ = 50pF | | 20 | 35 | ns |
| $t_{OD1}$ | Output disable[12,14,15] | F+ | $\overline{OE}$+ | $C_L$ = 5pF | | 20 | 35 | ns |
| $t_{PD}$ | Output | B± | (I, B)± | $C_L$ = 50pF | | 25 | 45 | ns |
| $t_{OE2}$ | Output enable[14] | B± | (I, B)+ | $C_L$ = 50pF | | 20 | 35 | ns |
| $t_{OD2}$ | Output disable[11,14,15] | B+ | (I, B)– | $C_L$ = 5pF | | 20 | 35 | ns |
| $t_{PRO}$ | Preset/Reset[14,15] | F+ | (I, B)+ | $C_L$ = 50pF | | 35 | 45 | ns |
| $t_{PPR}$ | Power–on/preset[14,15] | F– | $V_{CC}$+ | $C_L$ = 50pF | | 0 | 10 | ns |

**NOTES:**

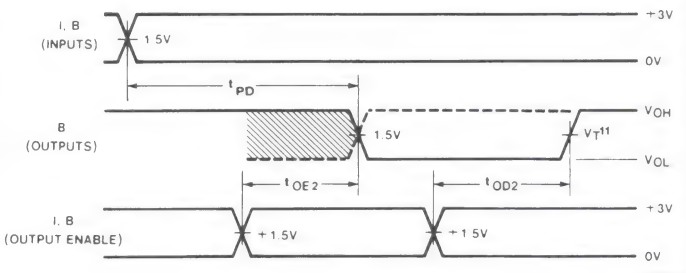
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with $V_{IH}$ applied to $\overline{OE}$.
6. Duration of short circuit should not exceed 1 second.
7. $I_{CC}$ is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V, and the outputs open.
8. Leakage values are a combination of input and output leakage.
9. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.
10. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 10ns.
11. Measured at $V_T = V_{OL}$ + 0.5V.
12. When using the Complement Array $T_{CKP}$ = 75ns (min).
13. Limits are guaranteed with 12 product terms maximum connected to each sum term line.
14. Not tested on an unprogrammed device.
15. Guaranteed, but not tested.

# Field-Programmable Logic Sequencer (16×45×12) — PLS159A

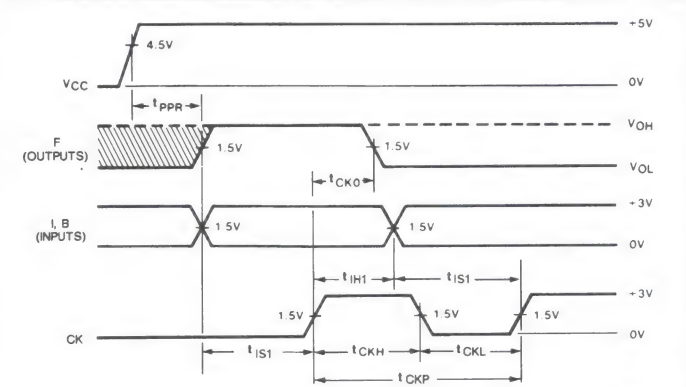
## TIMING DIAGRAMS




Flip-Flop Outputs




Gate Outputs

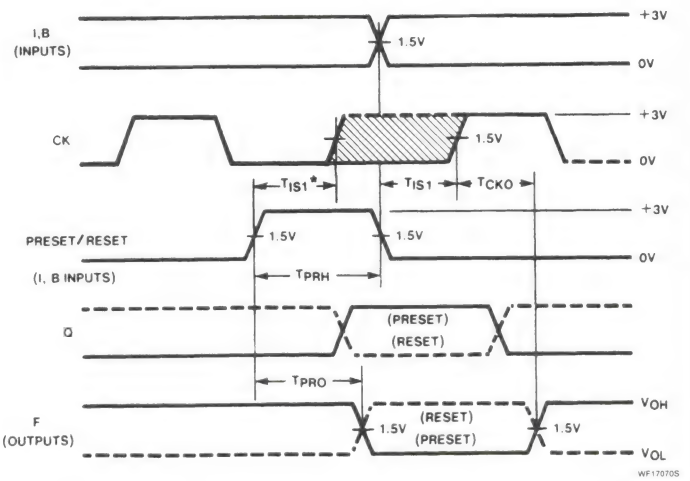



Power-On Reset

## TIMING DEFINITIONS

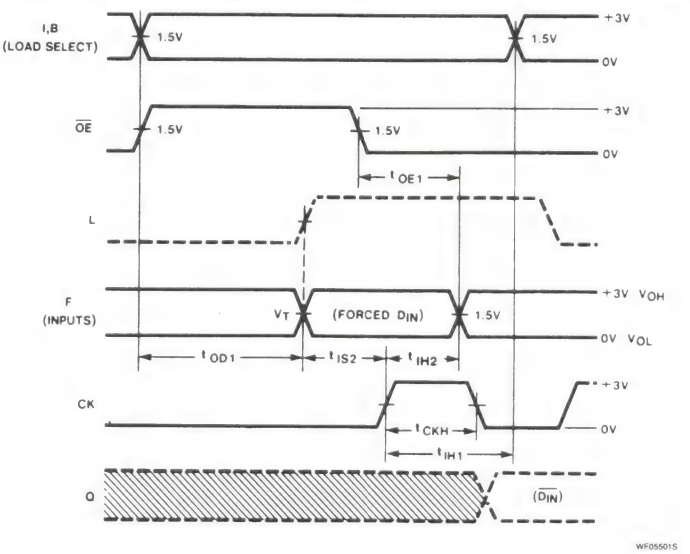
| SYMBOL | PARAMETER |
|---|---|
| $t_{CKH}$ | Width of input clock pulse when High. |
| $t_{CKL}$ | Width of input clock pulse when Low. |
| $t_{CKP}$ | Clock period. |
| $t_{PRH}$ | Width of preset input pulse. |
| $t_{IS1}$ | Required delay between beginning of valid input and positive transition of clock. |
| $t_{IS2}$ | Required delay between beginning of valid input forced at flip–flop output pins and positive transition of clock. |
| $t_{IH1}$ | Required delay between positive transition of clock and end of valid input data. |
| $t_{IH2}$ | Required delay between positive transition of clock and end of valid input data forced at flip–flop output pins.. |
| $t_{CKO}$ | Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low). |
| $t_{OE1}$ | Delay between beginning of Output Enable Low and when outputs become valid. |
| $t_{OD1}$ | Delay between beginning of Output Enable High and when outputs are in the Off–State. |
| $t_{PPR}$ | Delay between $V_{CC}$ (after power–on) and when flip–flop outputs become preset at "1" (internal Q outputs at "0"). |
| $t_{PD}$ | Propagation delay between combinational inputs and outputs. |
| $t_{OE2}$ | Delay between predefined Output Enable High, and when combinational outputs become valid. |
| $t_{OD2}$ | Delay between predefined Output Enable Low and when combinational outputs are in the OFF–State. |
| $t_{PRO}$ | Delay between positive transition of predefined Preset/Reset input and when flip–flop outputs become valid. |

## TIMING DIAGRAMS (Continued)




* Preset and Reset functions override Clock. However, F outputs may glitch with the first positive Clock Edge if $T_{IS1}$ cannot be guaranteed by the user.

**Asynchronous Preset/Reset**




**Flip-Flop Input Mode**

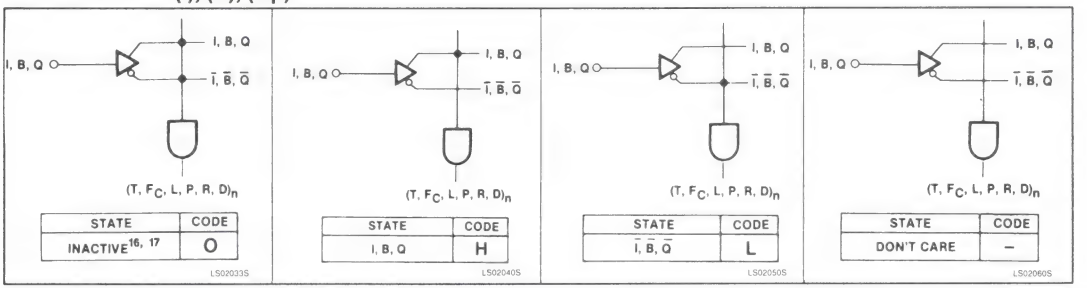
# Field-Programmable Logic Sequencer (16×45×12) — PLS159A

The FPLS can be programmed by means of Logic Programming equipment.

With Logic Programming, the AND/OR–EX–OR input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Tables on the following pages.

In these Tables, the logic state or action of all I/O, control and state variables are assigned a symbol which results in the proper fusing pattern of corresponding links defined as follows:

## "AND" ARRAY – (I), (B), (Qp)




| STATE | CODE |
|---|---|
| INACTIVE[16, 17] | O |

LS02033S

| STATE | CODE |
|---|---|
| I, B, Q | H |

LS02040S

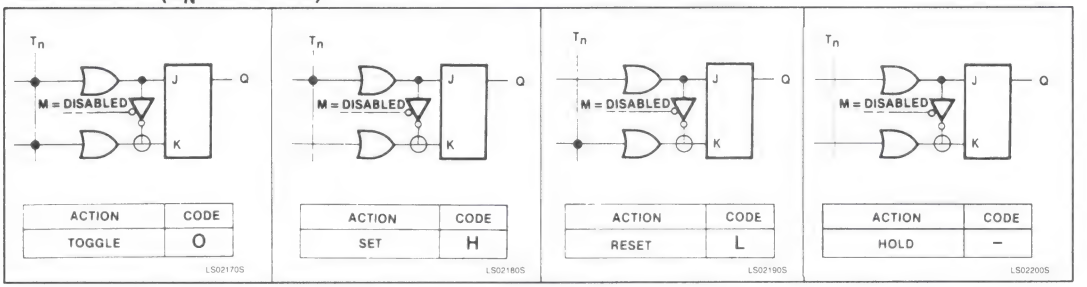
| STATE | CODE |
|---|---|
| $\bar{I}, \bar{B}, \bar{Q}$ | L |

LS02050S

| STATE | CODE |
|---|---|
| DON'T CARE | – |

LS02060S

## "OR" ARRAY – ($Q_N$ = J-K TYPE)




| ACTION | CODE |
|---|---|
| TOGGLE | O |

LS02170S

| ACTION | CODE |
|---|---|
| SET | H |

LS02180S

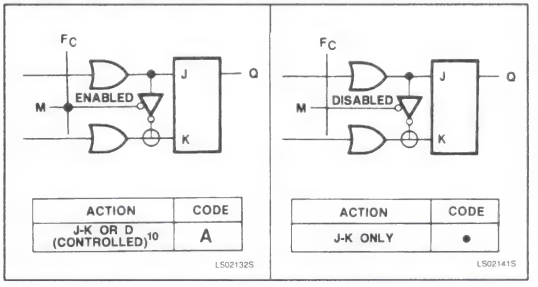
| ACTION | CODE |
|---|---|
| RESET | L |

LS02190S

| ACTION | CODE |
|---|---|
| HOLD | – |

LS02200S

## "OR" ARRAY – (MODE)



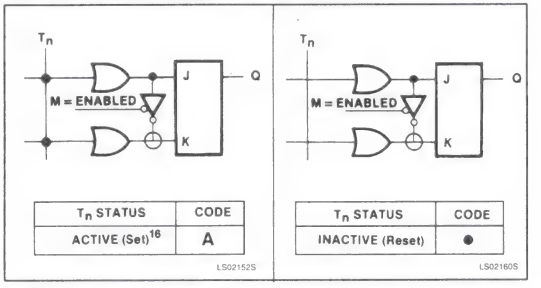

| ACTION | CODE |
|---|---|
| J-K OR D (CONTROLLED)[10] | A |

LS02132S

| ACTION | CODE |
|---|---|
| J-K ONLY | • |

LS02141S

## "OR" ARRAY – ($Q_N$ = D-TYPE)




| $T_n$ STATUS | CODE |
|---|---|
| ACTIVE (Set)[16] | A |

LS02152S

| $T_n$ STATUS | CODE |
|---|---|
| INACTIVE (Reset) | • |

LS02160S

**CAUTION:**
The PLS159A Programming Algorithm is different from the PLS159.

# Field-Programmable Logic Sequencer (16×45×12) — PLS159A

## "OR" ARRAY – (S or B)

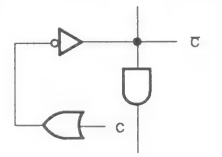
| $T_n$ STATUS | CODE |
|---|---|
| INACTIVE | • |

LS02221S

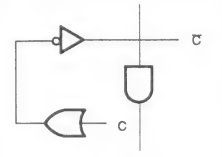
| $T_n$ STATUS | CODE |
|---|---|
| ACTIVE[16] | A |

LS02212S

## "COMPLEMENT" ARRAY – MODE

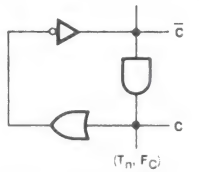



| ACTION | CODE |
|---|---|
| PROPAGATE | • |



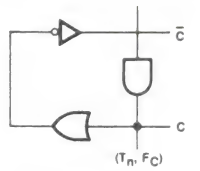

| ACTION | CODE |
|---|---|
| TRANSPARENT | — |

## "COMPLEMENT" ARRAY – (C)



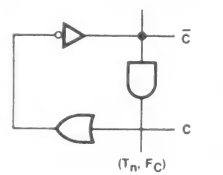

| ACTION | CODE |
|---|---|
| INACTIVE[16, 18, 20] | O |

LS02073S



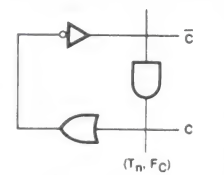

| ACTION | CODE |
|---|---|
| GENERATE[20] | A |

LS02082S




| ACTION | CODE |
|---|---|
| PROPAGATE | • |

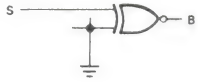
LS02090S




| ACTION | CODE |
|---|---|
| TRANSPARENT | – |

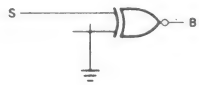
LS02100S

## "EX-OR" ARRAY – (B)




| POLARITY | CODE |
|---|---|
| LOW | L |

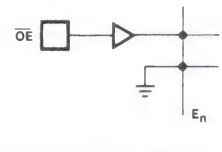
LS02230S




| POLARITY | CODE |
|---|---|
| HIGH | H |

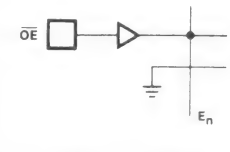
# Field-Programmable Logic Sequencer (16×45×12) PLS159A

## "OE" ARRAY – (E )



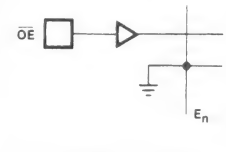

| ACTION | CODE |
|---|---|
| IDLE[16, 19] | O |

LS02253S



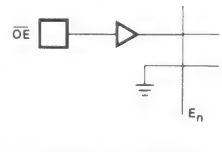

| ACTION | CODE |
|---|---|
| CONTROL | A |

LS02260S




| ACTION | CODE |
|---|---|
| ENABLE[19] | • |

LS02272S

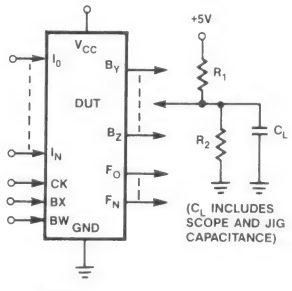



| ACTION | CODE |
|---|---|
| DISABLE | – |

LS02280S

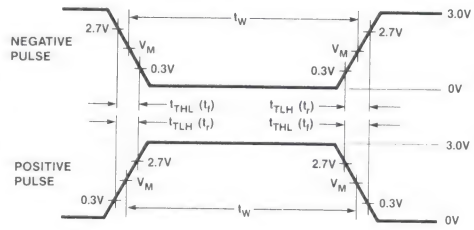
**NOTES:**
16. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
17. Any gate $(T, F_C. L, P, R, D)_n$ will be unconditionally inhibited if any one of the I, B, or Q link pairs are left intact.
18. To prevent oscillations, this state is not allowed for C link, pairs coupled to active gates $T_n$, $F_C$.
19. $E_n$ = O and $E_n$ = • are logically equivalent states, since both cause $F_n$ outputs to be unconditionally enabled.
20. These states are not allowed for control gates $(L, P, R, D)_n$ due to their lack of "OR" array links.

## TEST LOAD CIRCUITS




NOTE:
$R_1$ = 470Ω, $R_2$ = 1kΩ, $C_L$ = 50pF

## VOLTAGE WAVEFORMS




| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| $V_M$ | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ≤5ns | ≤5ns |

Signetics

# PLS167

## Field-Programmable Logic Sequencer (14×48×6)

*Product Specification*

**Military**
**Customer Specific Products**

### DESCRIPTION

The PLS167 is a bipolar, programmable state machine of the Mealy type. The Field-Programmable Logic Sequencer (FPLS) contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 8 $Q_p$, and 4 $Q_f$ edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND Array combines 14 external inputs, $I_{0\text{-}13}$, with 8 internal inputs, $P_{0\text{-}7}$, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, $P_0$ and $P_1$ of the internal state register are brought off-chip to allow extending the Output Register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR Array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable enable function, as an additional user programmable option.

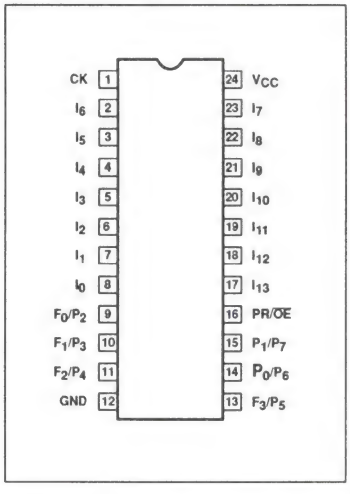
### APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Security locking systems

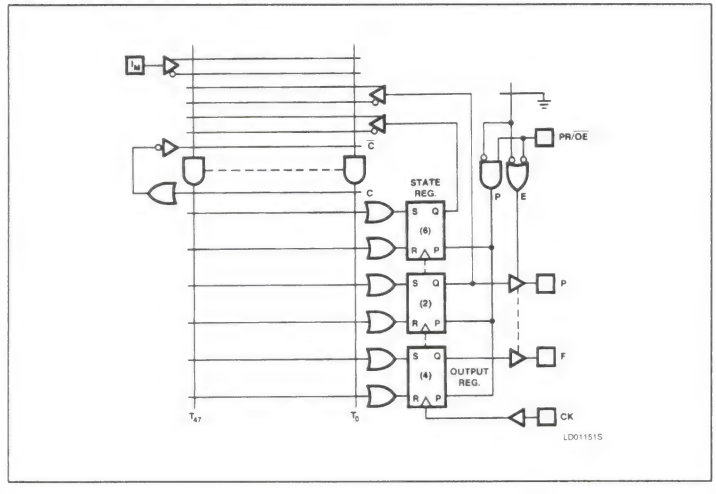
### FEATURES

- Field-programmable (Ni-Cr link)
- 14 True/Complement buffered inputs
- 48 programmable AND gates
- 25 programmable OR gates
- 8-bit State Register
- 2-bit shared State/Output Register
- 4-bit Output Register
- Transition Complement Array
- Programmable asynchronous preset/output enable
- Positive edge-trigger clock
- Power-on preset to logic "1" of all registers
- Automatic logic "HOLD" state via S/R flip-flops
- On-chip Test Array
- Power: 650mW (typ)
- TTL compatible
- Tri-state outputs
- Single +5V supply
- 300mil wide 24-Pin DIP

### PIN CONFIGURATION




### FUNCTIONAL DIAGRAM



# Field-Programmable Logic Sequencer (14×48×6) PLS167

## ORDERING INFORMATION

| PACKAGE | ORDER CODE |
|---|---|
| 24–Pin Ceramic Dip 300mil–wide | PLS167/BLA |

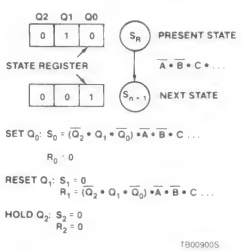
## PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION | POLARITY |
|---|---|---|---|
| 1 | CK | **Clock:** The Clock input to the state and output registers. A Low–to–High transition on this line is necessary to update the contents of both registers. | Active–High |
| 2 – 7<br>17 – 23 | $I_{1-13}$ | **Logic Inputs:** The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. | Active–High/Low |
| 8 | $I_0$ | **Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercised with standard TTL levels. When $I_0$ is held at +10V, device outputs $F_{0-3}$ and $P_{0-1}$ reflect the contents of state register bits $P_{2-7}$ (see Diagnostic Output Mode diagram). The contents of flip–flops $P_{0-1}$ and $F_{0-3}$ remain unaltered. | Active–High/Low |
| 9 – 11<br>13 | $F_{0-3}$ | **Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of output register bits $Q_{0-3}$ when enabled. When $I_0$ is held at +10V, $F_{0-3} = (P_{2-5})$. | Active–High |
| 14 – 15 | $P_{0-1}$ | **Logic/Diagnostic Outputs:** Two register bits with shared function as least significant state register bits, or most significant output register bits. When $I_0$ is held at +10V, $P_{0-1} = (P_{6-7})$. | Active–High |
| 16 | PR/$\overline{OE}$ | **Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function:<br>• **Preset:** Provides an asynchronous preset to logic "1" of all state and output register bits. Preset overrides Clock, and when held High, clocking is inhibited and $P_{0-1}$ and $F_{0-3}$ are High. Normal clocking resumes with the first full clock pulse following a High–to–Low clock transition, after Preset goes Low.<br>• **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers. | Active–High (H)<br>Active–Low (L) |

# Field-Programmable Logic Sequencer (14×48×6) PLS167

## LOGIC FUNCTION

**Typical State Transition:**


Q2 Q1 Q0
0 1 0
$S_R$
PRESENT STATE
STATE REGISTER
$\overline{A} \cdot \overline{B} \cdot C \cdot \ldots$
0 0 1
$S_{n-1}$
NEXT STATE
SET $Q_0$: $S_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$
RESET $Q_1$: $S_1 = 0$
$R_1 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
HOLD $Q_2$: $S_2 = 0$
$R_2 = 0$
TB00900S

## VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

6. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power–up procedure.
7. All transition terms are disabled (0).
8. All S/R flip–flop inputs are disabled (0).
9. The device can be clocked via a Test Array pre–programmed with a standard test pattern.

   NOTE: The Test Array pattern must be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

## TRUTH TABLE[1, 2, 3, 4, 5, 6]

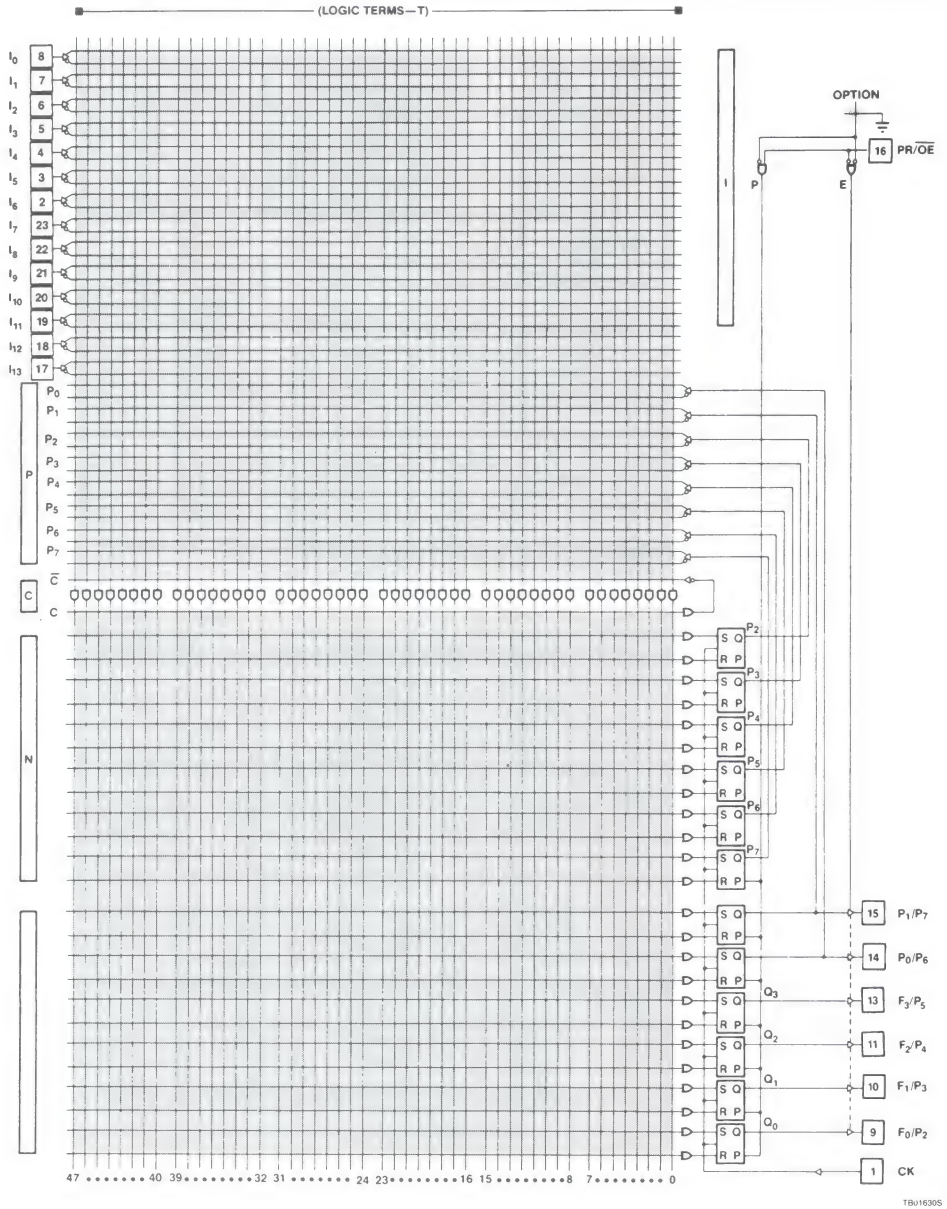
| $V_{CC}$ | OPTION PR | OPTION $\overline{OE}$ | $I_0$ | CK | S | R | $Q_{P/F}$ | F |
|---|---|---|---|---|---|---|---|---|
| +5V | H | | • | X | X | X | H | H |
| | L | | +10V | X | X | X | $Q_n$ | $(Q_P)_n$ |
| | L | | X | X | X | X | $Q_n$ | $(Q_F)_n$ |
| | | H | • | X | X | X | $Q_n$ | Hi–Z |
| | | L | +10V | X | X | X | $Q_n$ | $(Q_P)_n$ |
| | | L | X | X | X | X | $Q_n$ | $(Q_F)_n$ |
| | | L | X | ↑ | L | L | $Q_n$ | $(Q_F)_n$ |
| | | L | X | ↑ | L | H | L | L |
| | | L | X | ↑ | H | L | H | H |
| | | L | X | ↑ | H | H | IND. | IND. |
| ↑ | X | X | X | X | X | X | H | |

**NOTES:**

1. Positive Logic
   $S/\overline{R} = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C(I_0\, I_1\, I_2 \ldots)\,(P_0\, P_1 \ldots P_7)$
2. Either Preset (Active–High) or Output Enable (Active–Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. • = H/L/+10V.
6. X = Don't Care (≤ 5.5V).

# Field-Programmable Logic Sequencer (14×48×6) PLS167

## FPLS LOGIC DIAGRAM




**NOTES:**
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ○ Programmable connection.

# Field-Programmable Logic Sequencer (14×48×6) PLS167

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +7 | $V_{DC}$ |
| $V_I$ | Input voltage | +10.0 | $V_{DC}$ |
| $V_O$ | Output voltage | +5.5 | $V_{DC}$ |
| $I_I$ | Input currents | –30 to +30 | mA |
| $I_O$ | Output currents | +100 | mA |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMIT | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage range | 4.5 | 5.0 | 5.5 | V |
| $V_{IN}$[13] | High level Input voltage | 2.0 | | | V |
| $V_{IL}$[13] | Low level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High level output current | | | –2 | mA |
| $I_{OL}$ | Low level output current | | | 9.6 | mA |
| $T_A$ | Operating free–air temperature range | –55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS[1, 2] | LIMITS[3] | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| $V_{IK}$ | Input clamp voltage[4] | $V_{CC}$ = 4.5V, $I_I = I_{IK}$ | | –0.8 | –1.2 | V |
| | | $V_{CC}$ = Min | | | | |
| $V_{OL}$ | Low level Output Voltage[6] | $I_{OL}$ = Max | | 0.35 | 0.5 | V |
| $V_{OH}$ | High level Output Voltage[5] | $I_{OH}$ = Max | 2.4 | | | V |
| $I_{IL}$ | Low Level Input current | $V_{CC}$ = Min, $V_I$ = 0.45V | | –10 | –150 | µA |
| $I_{IL}$ | Low (CK input) Level Input current | $V_I$ = 0.45V, $V_{CC}$ = Min | | –50 | –350 | µA |
| $I_{IH}$ | High level Input current | $V_I$ = 5.5V, $V_{CC}$ = Min | | –1 | 50 | µA |
| | | $V_{CC}$ = Max | | | | |
| $I_{OHZ}$ | OFF–State output[7] Current High | $V_O$ = 5.5V | | 1 | 60 | µA |
| $I_{OLZ}$ | OFF–State output[7] Current Low | $V_O$ = 0.45V, $V_{CC}$ = Max | | –1 | –60 | µA |
| $I_{OS}$ | Short circuit output current[4,8] | $V_O$ = 0V, $V_{CC}$ = Max | –15 | | –85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[9] | $V_{CC}$ = Max | | 120 | 185 | mA |
| | | $V_{CC}$ = Nom | | | | |
| $C_{IN}$ | Input Capacitance[10] | $V_I$ = 2.0V | | 8 | 13 | pF |
| $C_{OUT}$ | Output Capacitance[10] | $V_O$ = 2.0V | | 10 | 15 | pF |

# Field-Programmable Logic Sequencer (14×48×6) PLS167

## AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$. $4.5V \le V_{CC} \le 5.5V$

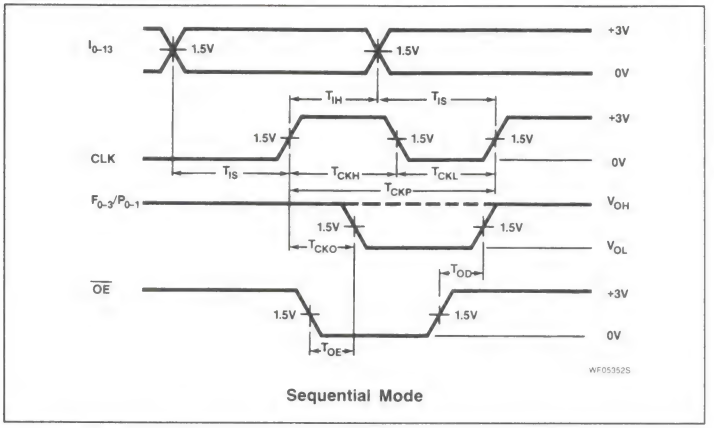
| SYMBOL | PARAMETER | TO | FROM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | |
| **Pulse Width** | | | | | | | |
| $t_{CKH}$ | Clock high[11] | CK– | CK+ | 40 | 15 | | ns |
| $t_{CKL}$ | Clock low | CK+ | CK– | 40 | 15 | | ns |
| $t_{CKP1}$ | Period (w/o C–array) | CK+ | CK+ | 95 | 40 | | ns |
| $t_{CKP2}$ | Period (w/C–array)[10] | CK+ | CK+ | 135 | 60 | | ns |
| $t_{PRH}$ | Preset pulse | PR+ | PR– | 40 | 15 | | ns |
| **Setup Time** | | | | | | | |
| $t_{IS1}$ | Input | CK+ | Input± | 60 | | | ns |
| $t_{IS2}$ | Input (through Complement array)[12] | CK+ | Input± | 100 | | | ns |
| $t_{VS}$ | Power–on preset[10] | CK– | $V_{CC}$+ | 5 | –10 | | ns |
| $t_{PRS}$ | Preset[10] | CK– | PR– | 5 | –10 | | ns |
| **Hold Time** | | | | | | | |
| $t_{IH}$ | Input[10] | Input± | CK+ | 10 | –10 | | ns |
| **Propagation Delay** | | | | | | | |
| $t_{CKO}$ | Clock | Output± | CK+ | | 15 | 35 | ns |
| $t_{OE}$ | Output Enable[12] | Output– | $\overline{OE}$– | | 20 | 40 | ns |
| $t_{OD}$ | Output Disable[12] | Output+ | $\overline{OE}$+ | | 20 | 40 | ns |
| $t_{PR}$ | Preset | Output+ | PR+ | | 18 | 45 | ns |
| $t_{PPR}$ | Power–on preset[10] | Output+ | $V_{CC}$+ | | 0 | 20 | ns |
| **Frequency of Operation** | | | | | | | |
| $f_{MAX}$ | W/O C–array | | | | | 10.5 | MHz |
| $f_{MAX}^{C}$ | W/C–array[10] | | | | | 7.4 | MHz |

**NOTES:**

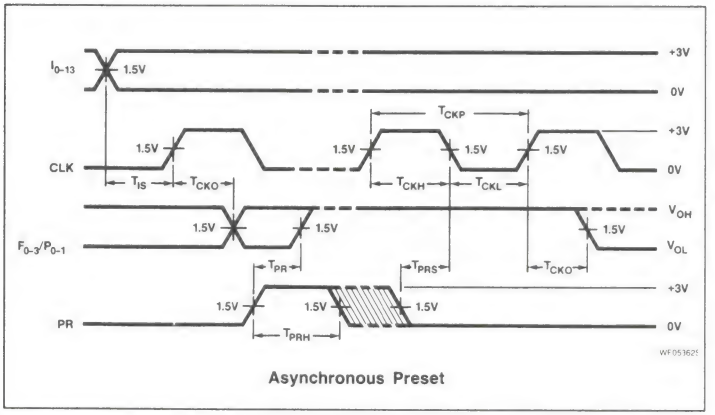
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with $V_{IL}$ applied to $\overline{OE}$ and a logic high stored, or with $V_{IH}$ applied to PR.
6. Measured with a programmed logic condition for which the output is at a low logic level, and $V_{IL}$ applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to $V_{CC}$.
7. Measured with $V_{IH}$ applied to PR/$\overline{OE}$.
8. Duration of short circuit should not exceed 1 second.
9. $I_{CC}$ is measured with the PR/$\overline{OE}$ input grounded, the outputs open.
10. Guaranteed, but not tested.
11. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 30ns.
12. Not testable on unprogrammed devices.
13. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.

# Field-Programmable Logic Sequencer (14×48×6) PLS167

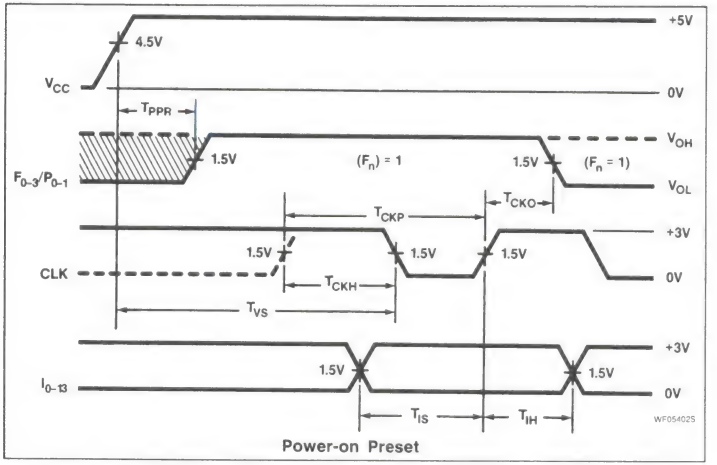
## TIMING DIAGRAMS




Sequential Mode




Asynchronous Preset



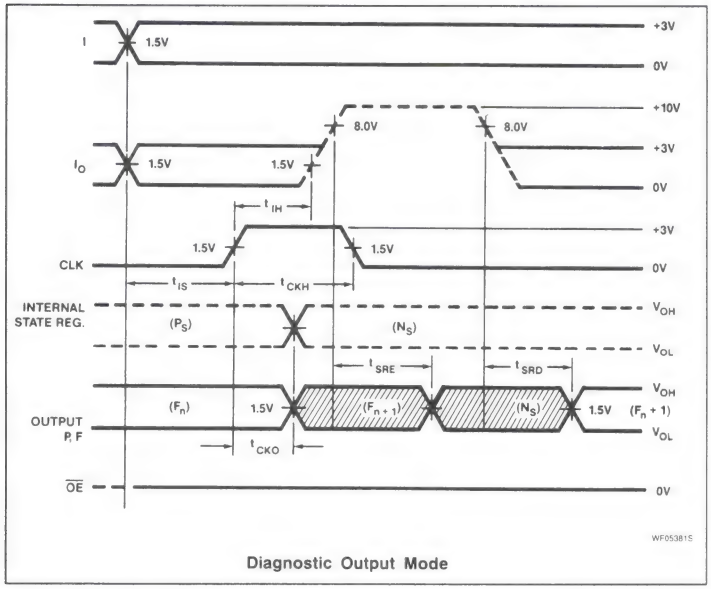

Power-on Preset

## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{CKH}$ | Width of input clock pulse. |
| $t_{CKL}$ | Interval between clock pulses. |
| $t_{CKP1}$ | Clock period – when not using Complement Array. |
| $t_{IS1}$ | Required delay between beginning of valid input and positive transition of clock. |
| $t_{CKP2}$ | Clock period – when using Complement Array. |
| $t_{IS2}$ | Required delay between beginning of valid input and positive transition of clock, when using optional Complement array (two passes necessary through the AND array). |
| $t_{VS}$ | Required delay between $V_{CC}$ (after power-on) and negative transition of clock preceding first reliable clock pulse. |
| $t_{PRS}$ | Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse. |
| $t_{IH}$ | Required delay between positive transition of clock and end of valid input data. |
| $t_{CKO}$ | Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{OE}$ Low). |
| $t_{OE}$ | Delay between beginning of Output Enable Low and when Outputs become valid. |
| $t_{OD}$ | Delay between beginning of Output Enable High and when Outputs are in the OFF-State. |
| $t_{PR}$ | Delay between positive transition of Preset and when Outputs become valid at "1". |
| $t_{PPR}$ | Delay between $V_{CC}$ (after power-on) and when Outputs become preset at "1". |
| $t_{PRH}$ | Width of preset input pulse. |
| $f_{MAX}$ | Maximum clock frequency. |

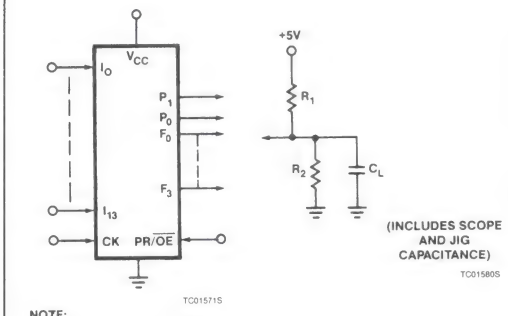
# Field-Programmable Logic Sequencer (14×48×6) PLS167

## TIMING DIAGRAMS (Continued)



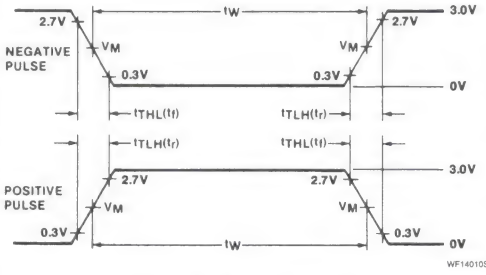

Diagnostic Output Mode

## TEST LOAD CIRCUIT




**NOTE:**
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 50pF$.

## VOLTAGE WAVEFORMS




### INPUT PULSE DEFINITIONS

| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| $V_M$ | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ⩽5ns | ⩽5ns |

# Field-Programmable Logic Sequencer (14×48×6) — PLS167

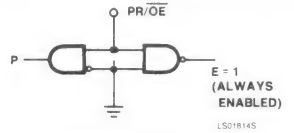
## LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

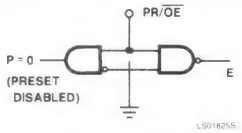
With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using a Program Table.

In this table, the logic state or action of control variables C, I, P, N and F, associated with each Transition Term $T_n$, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

### PRESET/$\overline{OE}$ OPTION – (P/E)




| OPTION | CODE |
|---|---|
| PRESET [14] | H |

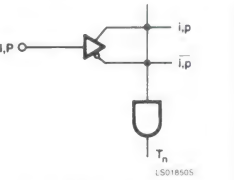



| OPTION | CODE |
|---|---|
| $\overline{OE}$ | L |

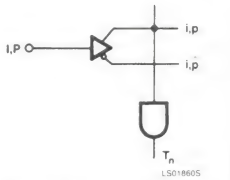
**PROGRAMMING:**

The PLS167 has a power-up feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at a logic high (H). When programming the device, it is important to realize this is the initial state of the device. You must provide a next state jump if you do not wish to use all highs (H) as the present state.

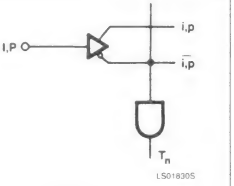
### "AND" ARRAY – (I), (P)



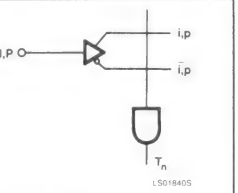

| STATE | CODE |
|---|---|
| INACTIVE [14,15] | O |




| STATE | CODE |
|---|---|
| I, P | H |

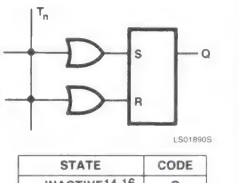



| STATE | CODE |
|---|---|
| $\overline{I}$, $\overline{P}$ | L |

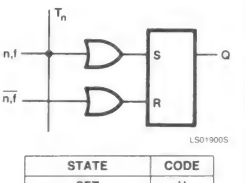



| STATE | CODE |
|---|---|
| DON'T CARE | - |

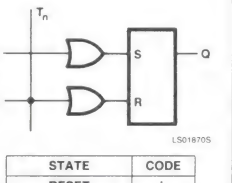
### "OR" ARRAY – (F), (N)



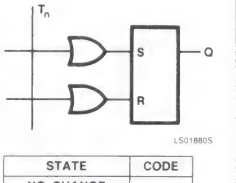

| STATE | CODE |
|---|---|
| INACTIVE [14,16] | O |




| STATE | CODE |
|---|---|
| SET | H |



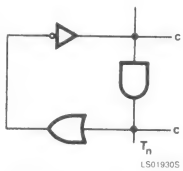

| STATE | CODE |
|---|---|
| RESET | L |



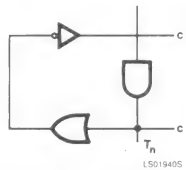

| STATE | CODE |
|---|---|
| NO CHANGE | - |

# Field-Programmable Logic Sequencer (14×48×6) PLS167

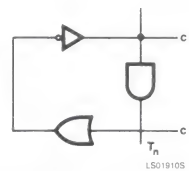
## "COMPLEMENT" ARRAY – (C)



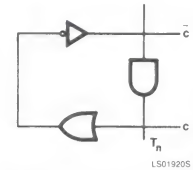

| ACTION | CODE |
|---|---|
| INACTIVE [14,17] | O |




| ACTION | CODE |
|---|---|
| GENERATE | A |




| ACTION | CODE |
|---|---|
| PROPAGATE | • |




| ACTION | CODE |
|---|---|
| TRANSPARENT | – |

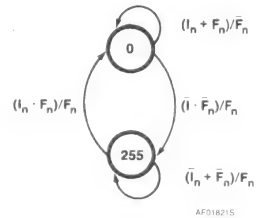
**NOTES:**
14. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates $T_n$.
15. Any gate $T_n$ will be unconditionally inhibited if any one of ites I or P link pairs are left intact.
16. To prevent simultaneous Set and Reset flip–flop commands, this state is not allowed for N and F link pairs coupled to active gates $T_n$ (see flip–flop truth tables).
17. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates $T_n$.

## TEST ARRAY

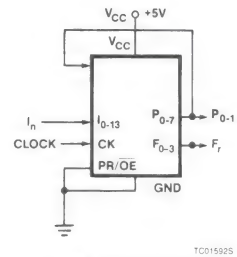
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to $I_{0\text{-}13}$ as shown in the test circuit timing diagram.




State Diagram




FPLS Under Test

| TERM | C | AND: INPUT (Im) 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PRESENT STATE (Ps) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 | A | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| 49 | • | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L |

Test Array Program

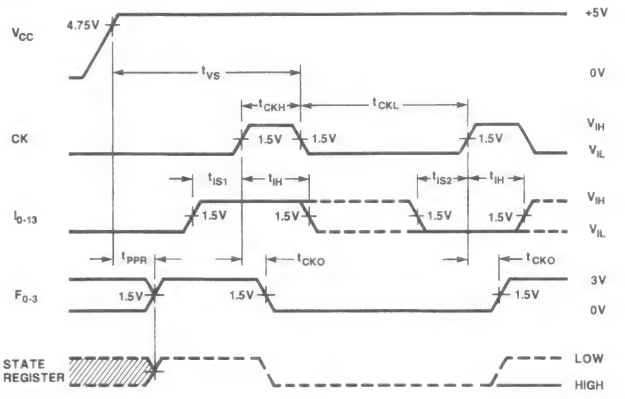
| OPTION (P/E) | | | | | | | | | | | H |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OR | | | | | | | | | | | |
| NEXT STATE (Ns) | | | | | | | | OUTPUT (Fr) | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 |
| L | L | L | L | L | L | L | L | L | L | L | L |
| H | H | H | H | H | H | H | H | H | H | H | H |

TB01600S

# Field-Programmable Logic Sequencer (14×48×6) PLS167

## TEST ARRAY (Continued)

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any of Signetics' qualified programming equipment.




Test Circuit Timing Diagram

| TERM | C | AND: INPUT (Im) 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PRESENT STATE (Ps) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 | – | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| 49 | ● | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L |

| OPTION (P/E) | | | | | | | | | | | H |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OR | | | | | | | | | | | |
| NEXT STATE (Ns) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OUTPUT (Fr) 3 | 2 | 1 | 0 |
| – | – | – | – | – | – | – | – | – | – | – | – |
| – | – | – | – | – | – | – | – | – | – | – | – |

TB01610S

Test Array Deleted

Signetics

# PLS168
## Field Programmable Logic Sequencer (12×48×8)

**Signetics Programmable Logic**
***Product Specification***

**Military**
**Customer Specific Products**

### DESCRIPTION

The PLS168 is a bipolar, programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 10 $Q_p$, and 4 $Q_f$ edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 12 external inputs, $I_{0-11}$, with 10 internal inputs, $P_{0-9}$, fed back from the State register to form up to 48 transition terms (AND terms). In addition, $P_0$–$P_3$ of the internal state register are brought off-chip to allow extending the output register to 8 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the log to high transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the complement array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes for this device are listed in the Ordering Information table.

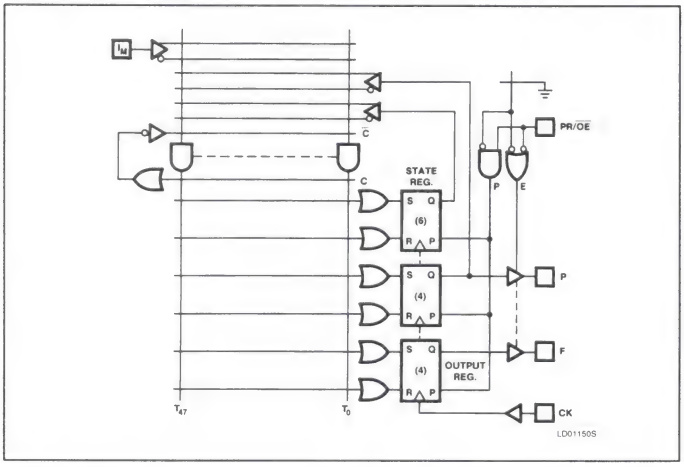
### FEATURES

- **Field-programmable (Ni-Cr link)**
- **12 True/Complement buffered inputs**
- **48 programmable AND gates**
- **29 programmable OR gates**
- **10-bit state register**
- **4-bit shared state/output register**
- **4-bit output register**
- **Transition complement array**
- **Programmable asynchronous preset/output enable**
- **Positive edge-trigger clock**
- **Power-on preset to logic "1" of all registers**
- **Automatic logic "HOLD" state via S/R flip-flops**
- **On-chip test array**
- **Power: 600mW**
- **TTL compatible**
- **3-State outputs**
- **Single +5V supply**
- **300mil-wide 24-pin DIP**

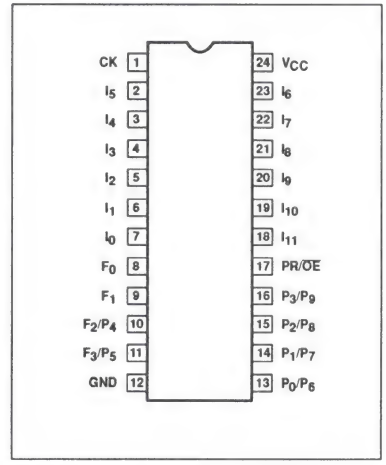
### APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

### FUNCTIONAL DIAGRAM

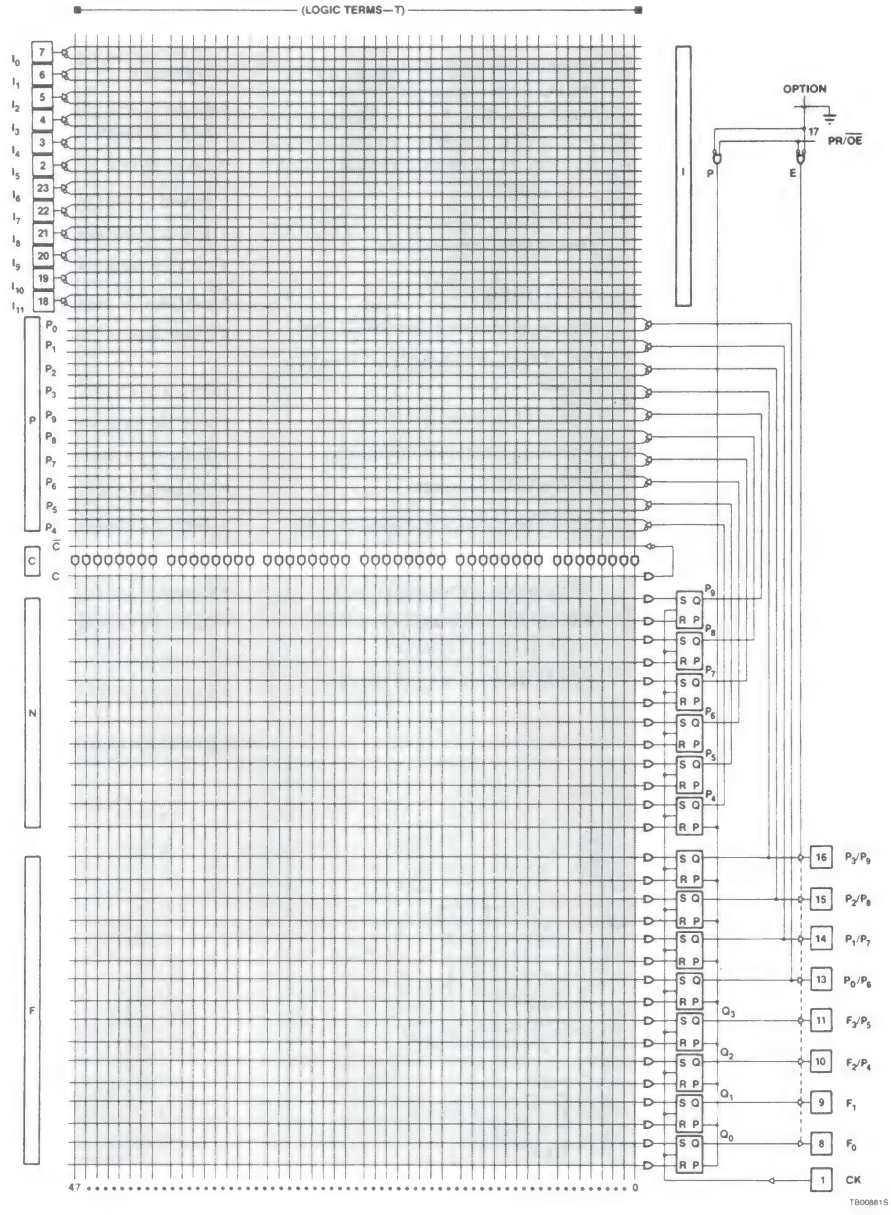



### PIN CONFIGURATION



# Field-Programmable Logic Sequencer (12×48×8) PLS168

## FPLS LOGIC DIAGRAM




**NOTES:**
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. Programmable connection.

# Field-Programmable Logic Sequencer (12×48×8) PLS168

## ORDERING INFORMATION

| PACKAGE | ORDER CODE |
|---|---|
| 24–Pin Ceramic DIP 300mil–wide | PLS168/BLA |

## PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION | POLARITY |
|---|---|---|---|
| 1 | CK | **Clock:** The Clock input to the state and output registers. A Low–to–High transition on this line is necessary to update the contents of both registers. | Active–High |
| 2 – 7<br>18 – 23 | $I_{1-11}$ | **Logic Inputs:** The 11 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. | Active–High/Low |
| 7 | $I_0$ | **Logic/Diagnostic Input:** A 12th external logic input to the AND array, as above, when exercised with standard TTL levels. When $I_0$ is held at +10V, device outputs $F_{2-3}$ and $P_{0-3}$ reflect the contents of state register bits $P_{4-9}$ (see Diagnostic Output Mode diagram on page 7). The contents of flip–flops $P_{0-1}$ and $F_{0-3}$ remain unaltered. | Active–High/Low |
| 13 – 16 | $P_{0-3}$ | **Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of state register bits $P_{0-3}$. When $I_0$ is held at +10V these pins reflect ($P_6 - P_9$). | Active–High |
| 10 – 11 | $F_2 - F_3$ | **Logic/Diagnostic Outputs:** Two register bits ($F_2 - F_3$) which normally reflect output register bits ($Q_2 - Q_3$). When $I_0$ is held at +10V these pins reflect ($P_4 - P_5$). | Active–High |
| 17 | PR/$\overline{OE}$ | **Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function:<br>• **Preset:** Provides an asynchronous preset to logic "1" of all state and output register bits. Preset overrides Clock, and when held High, clocking is inhibited and $P_{0-9}$ and $F_{0-3}$ are High. Normal clocking resumes with the first full clock pulse following a High–to–Low clock transition, after Preset goes Low.<br>• **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers. | Active–High (H)<br>Active–Low (L) |
| 8, 9 | $F_0 - F_1$ | **Logic Output:** Two device outputs which reflect output registers $Q_0 - Q_1$. When $I_0$ is held at +10V $F_0 - F_1$ = Logic "1". | |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | | +7 | $V_{DC}$ |
| $V_I$ | Input voltage | | +10.0 | $V_{DC}$ |
| $V_O$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_I$ | Input currents | –30 | +30 | mA |
| $I_O$ | Output currents | | +100 | mA |
| $T_A$ | Operating Temperature range | –55 | +125 | °C |
| $T_{STG}$ | Storage Temperature range | –65 | +150 | °C |

# Field-Programmable Logic Sequencer (12×48×8) PLS168

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER[3] | TEST CONDITIONS[3] | LIMITS[3] | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| **Input Voltage** | | | | | | |
| $V_{IH}$ | High | $V_{CC}$ = 5.5V | 2 | | | V |
| $V_{IL}$ | Low | $V_{CC}$ = 4.5V | | | 0.8 | V |
| $V_{IK}$ | Clamp[4] | $V_{CC}$ = 4.5V, $I_I$ = –18mA | | –0.8 | –1.2 | V |
| **Output Voltage** | | | | | | |
| | | $V_{CC}$ = 4.5V | | | | |
| $V_{OH}$ | High[5] | $I_{OH}$ = –2mA | 2.4 | | | V |
| $V_{OL}$ | Low[6] | $I_{OL}$ = 9.6mA | | 0.35 | 0.5 | V |
| **Input Current** | | | | | | |
| | | $V_{CC}$ = 5.5V | | | | |
| $I_{IH}$ | High | $V_I$ = 5.5V | | <1 | 50 | µA |
| $I_{IL}$ | Low | $V_I$ = 0.45V | | –10 | –150 | µA |
| $I_{IL}$ | Low (CK input) | $V_I$ = 0.45V | | –50 | –350 | µA |
| **Output Current** | | | | | | |
| | | $V_{CC}$ = 5.5V | | | | |
| $I_{O(OFF)}$ | Hi–Z state[7] | $V_{CC}$ = 5.5V | | 1 | 60 | µA |
| | | $V_O$ = 0.45V | | –1 | –60 | µA |
| $I_{OS}$ | Short circuit[4,8] | $V_O$ = 0V | –15 | | –85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[9] | $V_{CC}$ = 5.5V | | 120 | 185 | mA |
| **Capacitance[7, 10]** | | | | | | |
| | | $V_{CC}$ = 5.0V | | | | |
| $C_{IN}$ | Input | $V_I$ = 2.0V | | 8 | 10 | pF |
| $C_{OUT}$ | Output | $V_O$ = 2.0V | | 10 | 13 | pF |

# Field-Programmable Logic Sequencer (12×48×8) PLS168

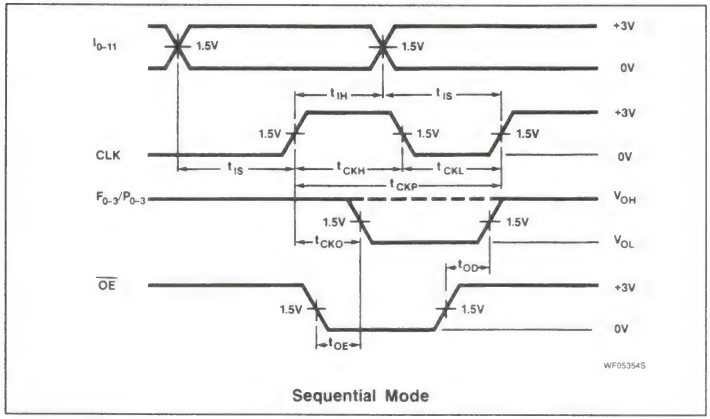
## AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TO | FROM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | |
| **Pulse Width** | | | | | | | |
| $t_{CKH}$ | Clock[11] High | CK– | CK+ | 40 | 15 | | ns |
| $t_{CKL}$ | Clock Low | CK+ | CK– | 40 | 15 | | ns |
| $t_{CKP1}$ | Period (w/o C–array) | CK+ | CK+ | 95 | 40 | | ns |
| $t_{CKP2}$ | Period (w/C–array)[10] | CK+ | CK+ | 135 | 60 | | ns |
| $t_{PRH}$ | Preset pulse | PR+ | PR– | 40 | 15 | | ns |
| **Setup Time** | | | | | | | |
| $t_{IS1}$ | Input | CK+ | Input± | 60 | | | ns |
| $t_{IS2}$ | Input (through Complement array)[12] | CK+ | Input± | 100 | | | ns |
| $t_{VS}$ | Power–on preset[10] | CK– | $V_{CC}$+ | 5 | –10 | | ns |
| $t_{PRS}$ | Preset[10] | CK– | PR– | 5 | –10 | | ns |
| **Hold Time** | | | | | | | |
| $t_{IH}$ | Input[10] | Input± | CK+ | 10 | –10 | | ns |
| **Propagation Delay** | | | | | | | |
| $t_{CKO}$ | Clock | Output± | CK+ | | 15 | 35 | ns |
| $t_{OE}$ | Output Enable | Output– | OE– | | 20 | 40 | ns |
| $t_{OD}$ | Output Disable | Output+ | OE+ | | 20 | 40 | ns |
| $t_{PR}$ | Preset | Output+ | PR+ | | 18 | 45 | ns |
| $t_{PPR}$ | Power–on preset | Output+ | $V_{CC}$+ | | 0 | 20 | ns |
| **Frequency of Operation** | | | | | | | |
| $f_{MAX}$ | w/o C–array | | | | | 10.5 | MHz |
| $f_{MAX}{}^{C}$ | w/C–array[10] | | | | | 7.4 | MHz |

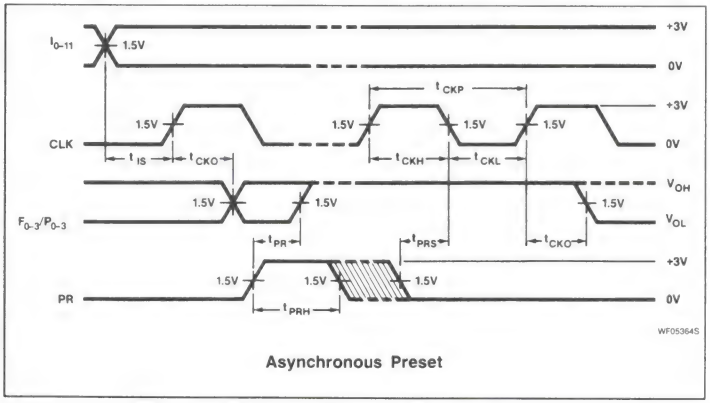
**NOTES:**
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with $V_{IL}$ applied to $\overline{OE}$ and a logic High stored, or with $V_{IH}$ applied to PR.
6. Measured with a programmed logic condition for which the output is at a Low logic level, and $V_{IL}$ applied to PR/$\overline{OE}$ Output sink current is applied through a resistor to $V_{CC}$.
7. Measured with $V_{IH}$ applied to PR/$\overline{OE}$.
8. Duration of short circuit should not exceed 1 second.
9. $I_{CC}$ is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V, ant the outputs open.
10. Guaranteed, but not tested.
11. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 30ns.
12. Not testable on unprogrammed devices.

# Field-Programmable Logic Sequencer (12×48×8) PLS168

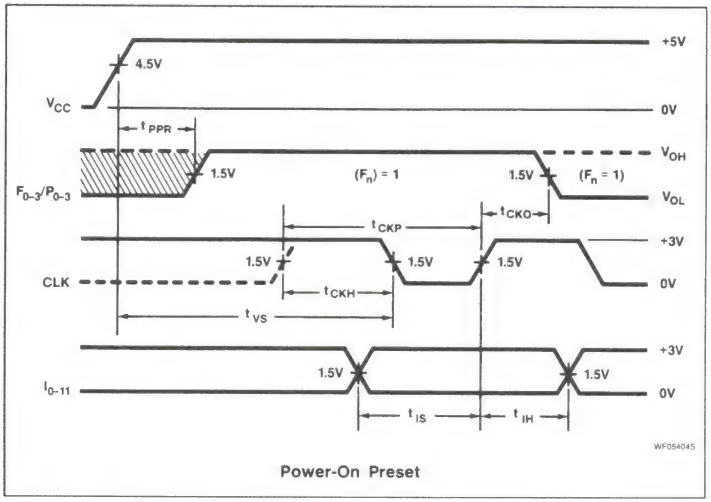
## TIMING DIAGRAMS




Sequential Mode




Asynchronous Preset



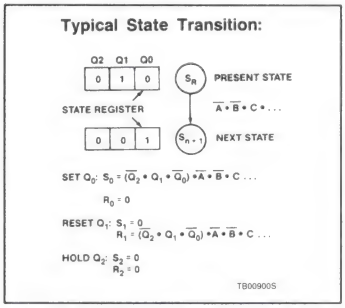

Power-On Preset

## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{CKH}$ | Width of input clock pulse. |
| $t_{CKL}$ | Interval between clock pulses. |
| $t_{CKP1}$ | Clock period – when not using Complement Array. |
| $t_{IS1}$ | Required delay between beginning of valid input and positive transition of clock. |
| $t_{CKP2}$ | Clock period – when using Complement Array. |
| $t_{IS2}$ | Required delay between beginning of valid input and positive transition of clock, when using optional Complement array (two passes necessary through the AND array). |
| $t_{VS}$ | Required delay between $V_{CC}$ (after power-on) and negative transition of clock preceding first reliable clock pulse. |
| $t_{PRS}$ | Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse. |
| $t_{IH}$ | Required delay between positive transition of clock and end of valid input data. |
| $t_{CKO}$ | Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{OE}$ Low). |
| $t_{OE}$ | Delay between beginning of Output Enable Low and when Outputs become valid. |
| $t_{OD}$ | Delay between beginning of Output Enable High and when Outputs are in the OFF-State. |
| $t_{PR}$ | Delay between positive transition of Preset and when Outputs become valid at "1". |
| $t_{PPR}$ | Delay between $V_{CC}$ (after power-on) and when Outputs become preset at "1". |
| $t_{PRH}$ | Width of preset input pulse. |
| $f_{MAX}$ | Maximum clock frequency. |

# Field-Programmable Logic Sequencer (12×48×8) — PLS168

## LOGIC FUNCTION


Typical State Transition:
Q2 Q1 Q0
0 1 0
PRESENT STATE
STATE REGISTER
0 0 1
NEXT STATE
SET Q0: S0 = (Q2 • Q1 • Q0) • A • B • C . . .
R0 = 0
RESET Q1: S1 = 0
R1 = (Q2 • Q1 • Q0) • A • B • C . . .
HOLD Q2: S2 = 0
R2 = 0
TB00900S

## VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power–up procedure.
2. All transition terms are disabled (0).
3. All S/R flip–flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre–programmed with a standard test pattern.

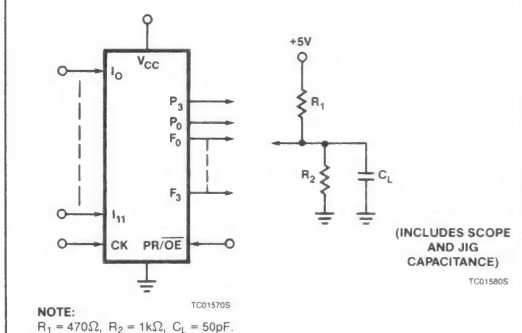
   NOTE: The Test Array pattern must be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

## TRUTH TABLE[1, 2, 3, 4, 5, 6]

| $V_{CC}$ | OPTION PR | OPTION $\overline{OE}$ | $I_0$ | CK | S | R | $Q_{P/F}$ | F |
|---|---|---|---|---|---|---|---|---|
| +5V | H | | • | X | X | X | H | H |
| | L | | +10V | X | X | X | $Q_n$ | $(Q_P)_n$ |
| | L | | X | X | X | X | $Q_n$ | $(Q_F)_n$ |
| | | H | • | X | X | X | $Q_n$ | Hi–Z |
| | | L | +10V | X | X | X | $Q_n$ | $(Q_P)_n$ |
| | | L | X | X | X | X | $Q_n$ | $(Q_F)_n$ |
| | | L | X | ↑ | L | L | $Q_n$ | $(Q_F)_n$ |
| | | L | X | ↑ | L | H | L | L |
| | | L | X | ↑ | H | L | H | H |
| | | L | X | ↑ | H | H | IND. | IND. |
| ↑ | X | X | X | X | X | X | H | |

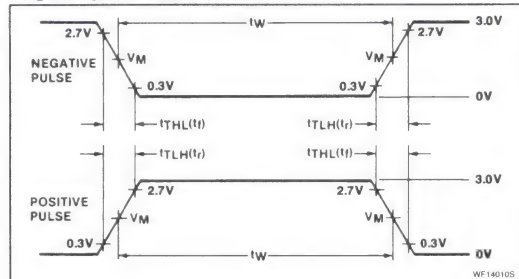
NOTES:
1. Positive Logic $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$; $T_n = C(I_0\, I_1\, I_2 \ldots)(P_0\, P_1 \ldots P_8)$
2. Either Preset (Active–High) or Output Enable (active–Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an Illegal input condition.
5. • = H/L/+10V.
6. X = Don't Care (≤ 5.5V).

## TEST LOAD CIRCUIT




NOTE:
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 50pF$.

## VOLTAGE WAVEFORMS




### INPUT PULSE DEFINITIONS

| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| $V_M$ | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ⩽5ns | ⩽5ns |

# Field-Programmable Logic Sequencer (12×48×8) — PLS168

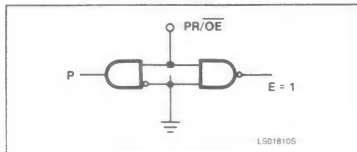
## LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Table on the following page.

In this table, the logic state or action of control variables C, I, P, N and F, associated with each Transition Term $T_n$, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

## PRESET/$\overline{OE}$ OPTION – (P/E)

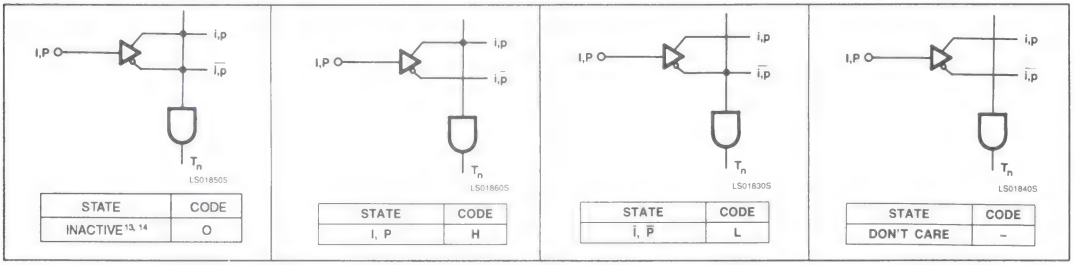



| OPTION | CODE |
|---|---|
| PRESET | H |

| OPTION | CODE |
|---|---|
| $\overline{O.E.}$ | L |

**PROGRAMMING:**
The PLS168 has a power–up pre–set feature. This feature insures that the device will power–up in a known state with all register elements (state and output register) at a logic High (H). When programming the device, it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

## "AND" ARRAY – (I), (P)



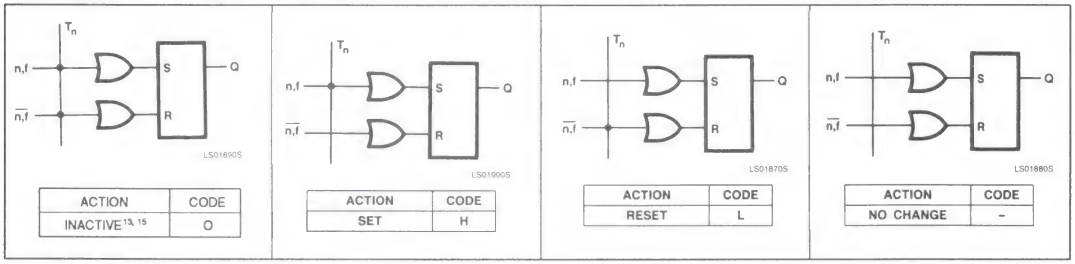

| STATE | CODE |
|---|---|
| INACTIVE[13, 14] | O |

| STATE | CODE |
|---|---|
| I, P | H |

| STATE | CODE |
|---|---|
| $\overline{I}$, $\overline{P}$ | L |

| STATE | CODE |
|---|---|
| DON'T CARE | – |

## "OR" ARRAY – (N), (F)



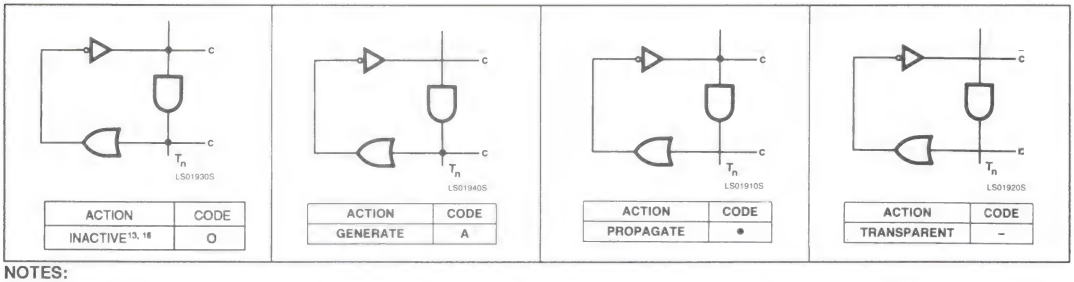

| ACTION | CODE |
|---|---|
| INACTIVE[13, 15] | O |

| ACTION | CODE |
|---|---|
| SET | H |

| ACTION | CODE |
|---|---|
| RESET | L |

| ACTION | CODE |
|---|---|
| NO CHANGE | – |

## "COMPLEMENT" ARRAY – (C)




| ACTION | CODE |
|---|---|
| INACTIVE[13, 16] | O |

| ACTION | CODE |
|---|---|
| GENERATE | A |

| ACTION | CODE |
|---|---|
| PROPAGATE | • |

| ACTION | CODE |
|---|---|
| TRANSPARENT | – |

**NOTES:**
13. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates $T_n$.
14. Any gate $T_n$ will be unconditionally inhibited if any one of its I or P link pairs are left intact.
15. To prevent simultaneous Set and Reset flip–flop commands, this state is not allowed for N and F link pairs coupled to active gates $T_n$ (see flip–flop truth tables).
16. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates $T_n$.

# Field-Programmable Logic Sequencer (12×48×8) PLS168

## FPLS PROGRAM TABLE PLS168

CUSTOMER NAME _____

SIGNETICS DEVICE # _____

PROGRAM TABLE # _____

REV _____

DATE _____

AND

| | |
|---|---|
| INACTIVE | O |
| GENERATE | A |
| PROPAGATE | * |
| TRANSPARENT | – |

$C_n$

| | |
|---|---|
| INACTIVE | O |
| L.P | H |
| L.P | L |
| DON'T CARE | – |

$I_m$ $P_s$

OR

| | |
|---|---|
| INACTIVE | O |
| SET | H |
| RESET | L |
| NO CHANGE | – |

$N_s$ . $F_r$

OPTION

| | |
|---|---|
| PRESET | H |
| OE | L |

P/E

| TERM | $C_n$ | INPUT(Im) 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PRESENT STATE (Ps) (Px) 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | REMARKS | NEXT STATE (Ns) (Px) 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | OUTPUT (Fr) 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 33 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 34 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 35 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 37 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 38 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 39 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 40 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 41 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 42 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 43 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 44 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 45 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 46 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 47 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| PIN NO. | 18 | 19 | 20 | 21 | 22 | 23 | 2 | 3 | 4 | 5 | 6 | 7 | | 16 | 15 | 14 | 13 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VARIABLE NAME | | | | | | | | | | | | | | | | | | | | | |

TB00891S

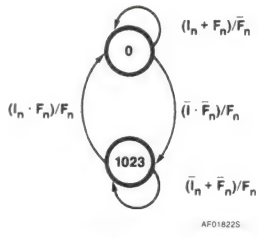
# Field-Programmable Logic Sequencer (12×48×8) PLS168

## TEST ARRAY

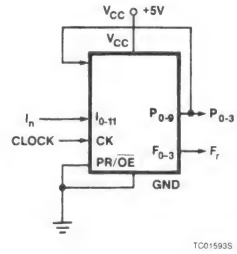
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to $I_{0\text{-}11}$ as shown in the test circuit timing diagram.




State Diagram

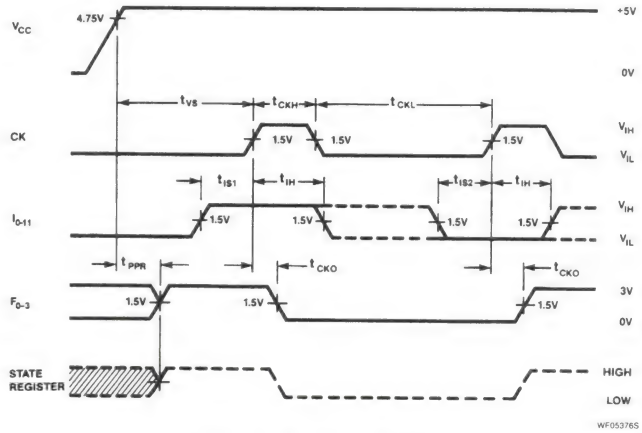



FPLS Under Test

| TERM | $C_n$ | INPUT(Im) 11 10 9 8 7 6 5 4 3 2 1 0 | PRESENT STATE (Ps) (Px) 9 8 7 6 5 4 3 2 1 0 | REMARKS | OPTION (P E) H; OR; NEXT STATE (Ns) (Px) 9 8 7 6 5 4 3 2 1 0 | OUTPUT (Fr) 3 2 1 0 |
|---|---|---|---|---|---|---|
| 48 | A | H H H H H H H H H H H H | H H H H H H H H H H | | L L L L L L L L L L | L L L L |
| 49 | • | L L L L L L L L L L L L | L L L L L L L L L L | | H H H H H H H H H H | H H H H |

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any of Signetics' qualified programming equipment.




Test Circuit Timing Diagram

| TERM | $C_n$ | INPUT(Im) 11 10 9 8 7 6 5 4 3 2 1 0 | PRESENT STATE (Ps) (Px) 9 8 7 6 5 4 3 2 1 0 | REMARKS | OPTION (P E) H; OR; NEXT STATE (Ns) (Px) 9 8 7 6 5 4 3 2 1 0 | OUTPUT (Fr) 3 2 1 0 |
|---|---|---|---|---|---|---|
| 48 | – | H H H H H H H H H H H H | H H H H H H H H H H | | – – – – – – – – – – | – – – – |
| 49 | • | L L L L L L L L L L L L | L L L L L L L L L L | | – – – – – – – – – – | – – – – |

Test Array Deleted

Signetics

# PLS173
## Field-Programmable Logic Array (22×42×10)

**Signetics Programmable Logic**
***Product Specification***

**Military**
**Application Specific Products**

### DESCRIPTION

The PLS173 is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS173 is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

### FEATURES

- **Field-Programmable (NI-Cr links)**
- **12 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
  - **32 Logic Terms**
  - **10 Control Terms**
- **Power dissipation: 750mW (typ)**
- **Output: 3-State**
- **TTL compatible**

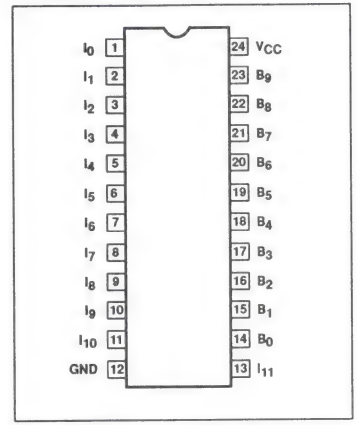
### APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 24-pin Ceramic DIP 300mil-wide | PLS173/BLA |

### PIN CONFIGURATION




### LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L

$Z = \overline{P0 + P1 + P2 + \ldots}$

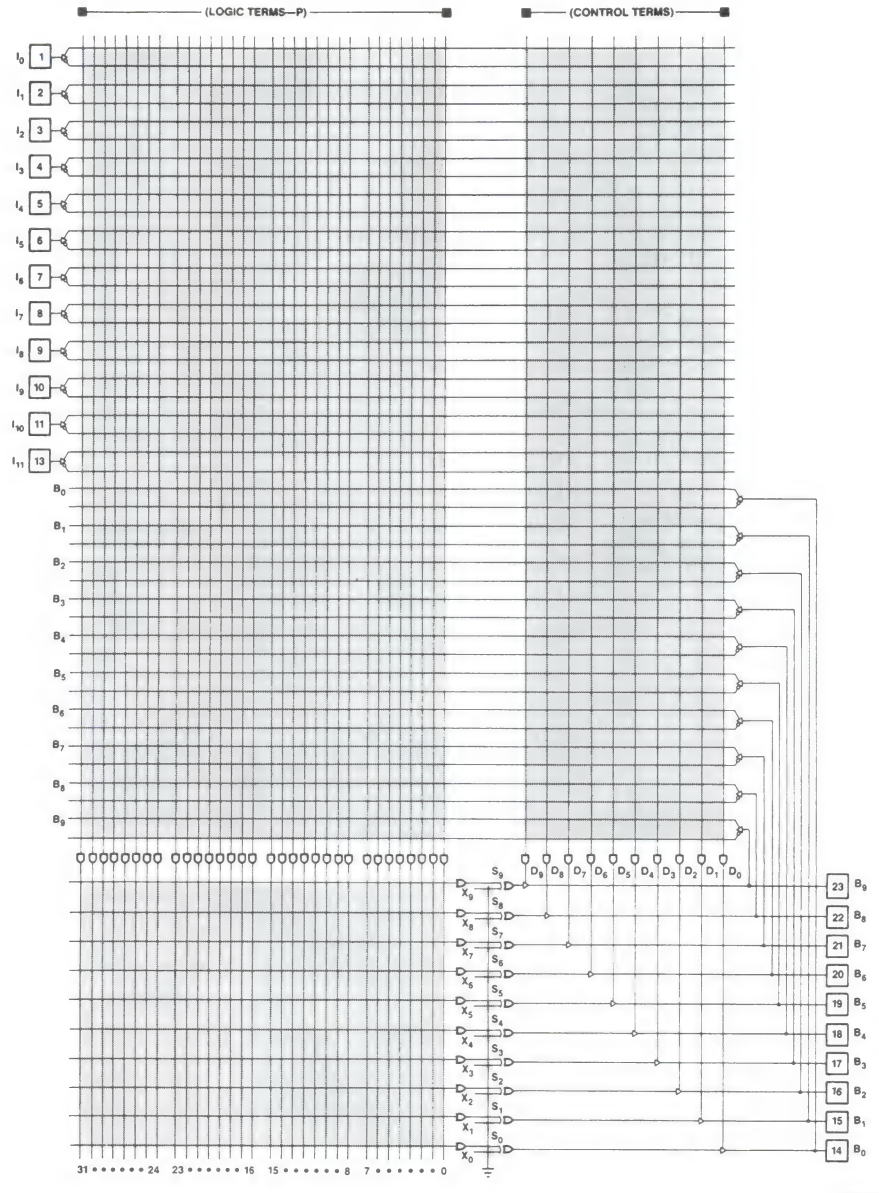
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:

1. For each of the 10 outputs, either function Z (active-high) or Z (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc., are user defined connections to fixed inputs (I) and bidirectional pins (B).

# Field–Programmable Logic Array (22×42×10) PLS173

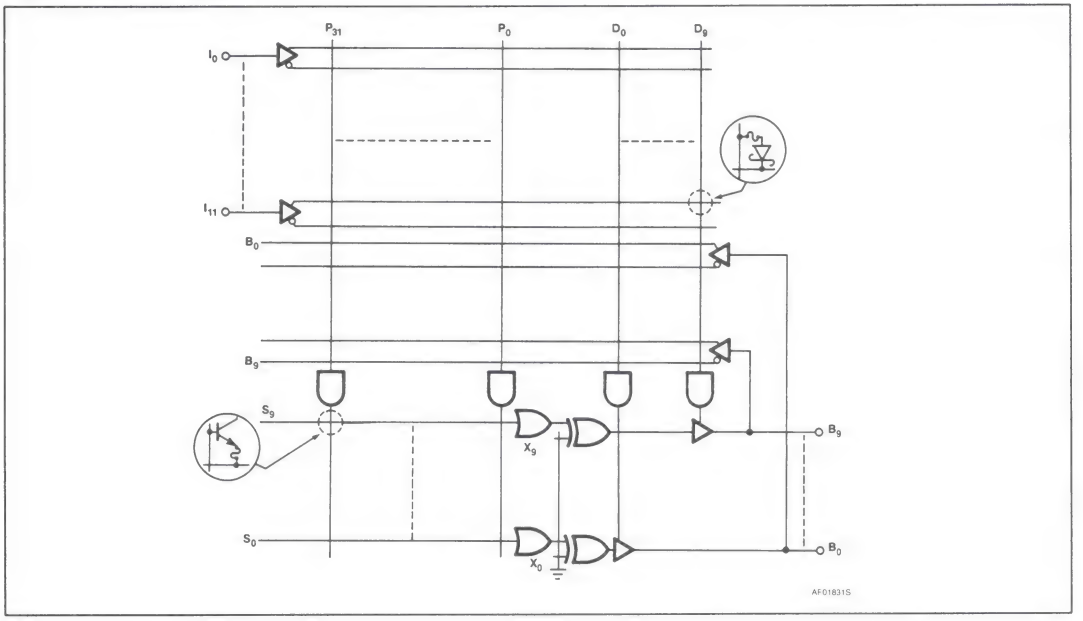
## FPLA LOGIC DIAGRAM




**NOTES:**
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ● Programmable connection.

# Field-Programmable Logic Array (22×42×10) PLS173

## FUNCTIONAL DIAGRAM




## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | | +7 | $V_{DC}$ |
| $V_I$ | Input voltage | | +10.0 | $V_{DC}$ |
| $V_O$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_I$ | Input currents | –30 | +30 | mA |
| $I_O$ | Output currents | | +100 | mA |
| $T_A$ | Operating temperature range | –55 | +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 | +150 | °C |

# Field-Programmable Logic Array (22×42×10) PLS173

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER[3] | TEST CONDITIONS[3] | LIMITS[3] | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| **Input voltage** | | | | | | |
| $V_{IL}$ | Low | $V_{CC}$ = 4.5V | | | .80 | V |
| $V_{IH}$ | HIgh | $V_{CC}$ = 5.5V | 2.0 | | | V |
| $V_{IK}$ | Clamp[4] | $V_{CC}$ = 4.5V, $I_I$ = −18mA | | −0.8 | −1.2 | V |
| **Output voltage** | | | | | | |
| | | $V_{CC}$ = 4.5V | | | | |
| $V_{OL}$ | Low[5] | $I_{OL}$ = 12mA | | | 0.5 | V |
| $V_{OH}$ | High[6] | $I_{OH}$ = −2mA | 2.4 | | | V |
| **Input current** | | | | | | |
| | | $V_{CC}$ = 5.5V | | | | |
| $I_{IL}$ | Low | $V_I$ = 0.45V | | | −150 | µA |
| $I_{IH}$ | High | $V_I$ = 5.5V | | | 50 | µA |
| **Output current** | | | | | | |
| | | $V_{CC}$ = 5.5V | | | | |
| $I_{O(OFF)}$ | Hi–Z state[10] | $V_O$ = 5.5V | | | 110 | µA |
| | | $V_O$ = 0.45V | | | −210 | µA |
| $I_{OS}$ | Output short circuit[4,6,7] | $V_O$ = 0V | −15 | | −85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[8] | $V_{CC}$ = 5.5V | | 150 | 170 | mA |
| **Capacitance[11]** | | | | | | |
| | | $V_{CC}$ = 5.0V | | | | |
| $C_I$ | Input | $V_I$ = 2.0V | | 8 | 12 | pF |
| $C_B$ | I/O | $V_B$ = 2.0V | | 15 | 19 | pF |

## AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

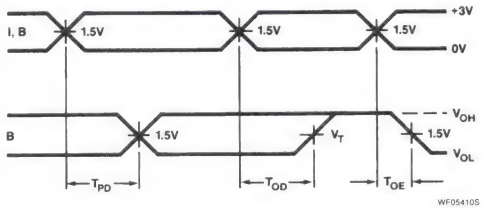
| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $t_{PD}$ | Propagation Delay | Output± | Input± | $C_L$ = 50pF | | 20 | 40 | ns |
| $t_{OE}$ | Output Enable[12] | Output– | Input± | $C_L$ = 50pF | | 20 | 35 | ns |
| $t_{OD}$ | Output Disable[9,12] | Output+ | Input± | $C_L$ = 50pF | | 20 | 35 | ns |

**NOTES:**

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with Pins 1 – 5 = 0V, Pins 6 – 10 = 4.5V, Pin 11 = 0V and Pin 13 = 10V.
6. Same conditions as Note 5, except Pin 11 = +10V.
7. Duration of short circuit should not exceed 1 second.
8. $I_{CC}$ is measured with $I_0$ and $I_1$ = 0V and $I_2 - I_{11}$ and $B_0 - B_9$ = 4.5V. Part in Virgin State.
9. Measured at $V_T = V_{OL} + 0.5V$.
10. Leakage values are a combination of input and output leakage.
11. Guaranteed, but not tested.
12. Guaranteed but not tested in unprogrammed devices.

# Field-Programmable Logic Array (22×42×10) PLS173

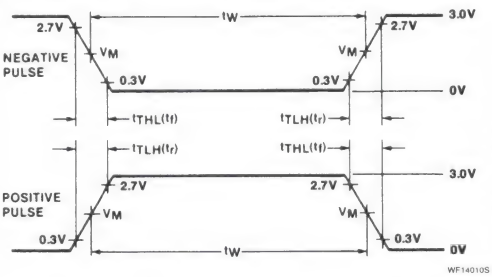
## TIMING DIAGRAMS




## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{PD}$ | Propagation delay between input and output. |
| $t_{OD}$ | Delay between input change and when output is off (Hi–Z or High). |
| $t_{OE}$ | Delay between input change and when output reflects specified output level. |

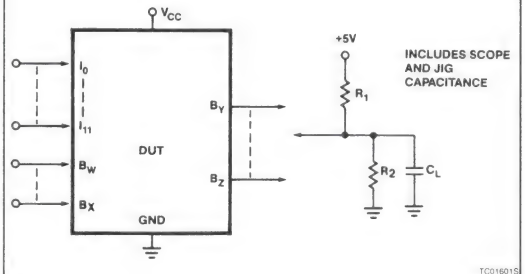
## VOLTAGE WAVEFORM




### INPUT PULSE DEFINITIONS

| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| $V_M$ | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ⩽5ns | ⩽5ns |

## TEST LOAD CIRCUIT




NOTE:
$R_1 = 470\Omega$, $R_2 = 1K\Omega$, $C_L = 50pF$

# Field-Programmable Logic Array (22×42×10) — PLS173

## LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

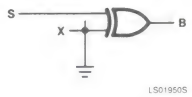
With Logic programming, the AND/OR/EX–OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this table, the logic state of variables I, P and B, associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

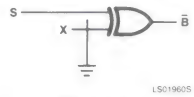
## CAUTION: PLS173 TEST COLUMNS

The PLS173 incorporates two columns not shown in the logic block diagram. These columns are used for in–house testing of the device in the unprogrammed state. These columns must be disabled prior to using the PLS173 in your application. If you are using a Signetics approved programmer, the disabling is accomplished during the device programming sequence. If these columns are not disabled, abnormal operation is possible.

## OUTPUT POLARITY – (O, B)

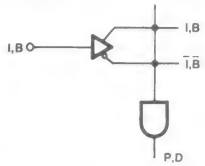



| ACTIVE LEVEL | CODE |
|---|---|
| HIGH | H |

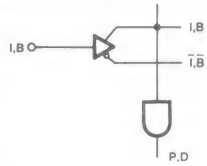



| ACTIVE LEVEL | CODE |
|---|---|
| LOW | L |

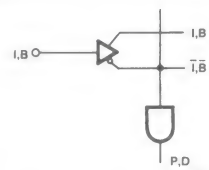
## "AND" ARRAY – (I, B)



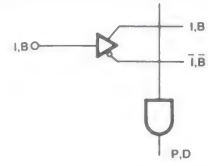

| ACTION | CODE |
|---|---|
| INACTIVE[13,14] | O |




| STATE | CODE |
|---|---|
| I, B | H |

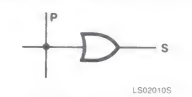



| STATE | CODE |
|---|---|
| $\overline{I}$, $\overline{B}$ | L |

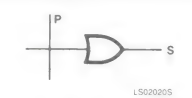



| STATE | CODE |
|---|---|
| DON'T CARE | – |

## "OR" ARRAY – (B)




| $P_n$ STATUS | CODE |
|---|---|
| ACTIVE | A |




| $P_n$ STATUS | CODE |
|---|---|
| INACTIVE | • |

## VIRGIN STATE

A factory shipped virgin device contains all fusible links open, such that:

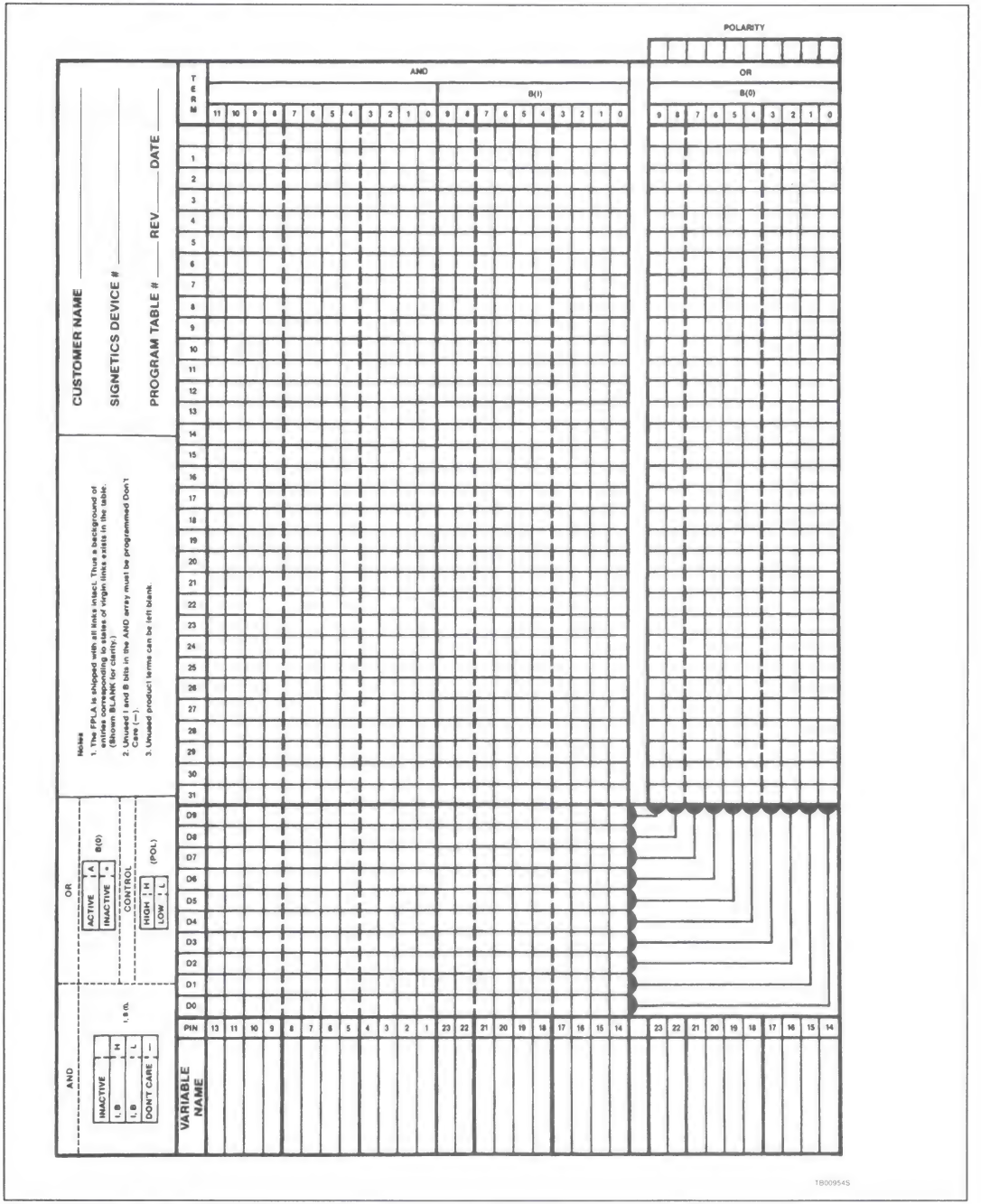
1. All outputs at "H" polarity.
2. All $P_n$ terms are disabled.
3. All $P_n$ terms are active on all outputs.

**NOTES:**

13. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates $P_n$, $D_n$.
14. Any gate $P_n$, $D_n$ will unconditionally inhibited if any one its (I, B) link pairs is left intact.

# Field-Programmable Logic Array (22×42×10) PLS173

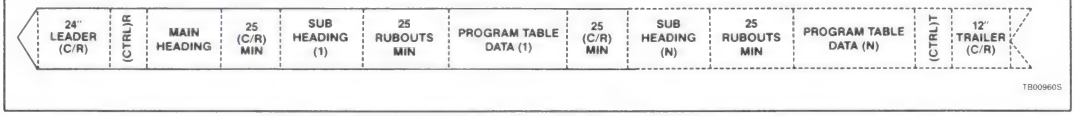
## FPLA PROGRAM TABLE



## TWX TAPE CODING (LOGIC FORMAT)

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8–level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339–9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however, limit tape length to a roll of 1.75 inch inside diameter and 4.25 inch outside diameter.



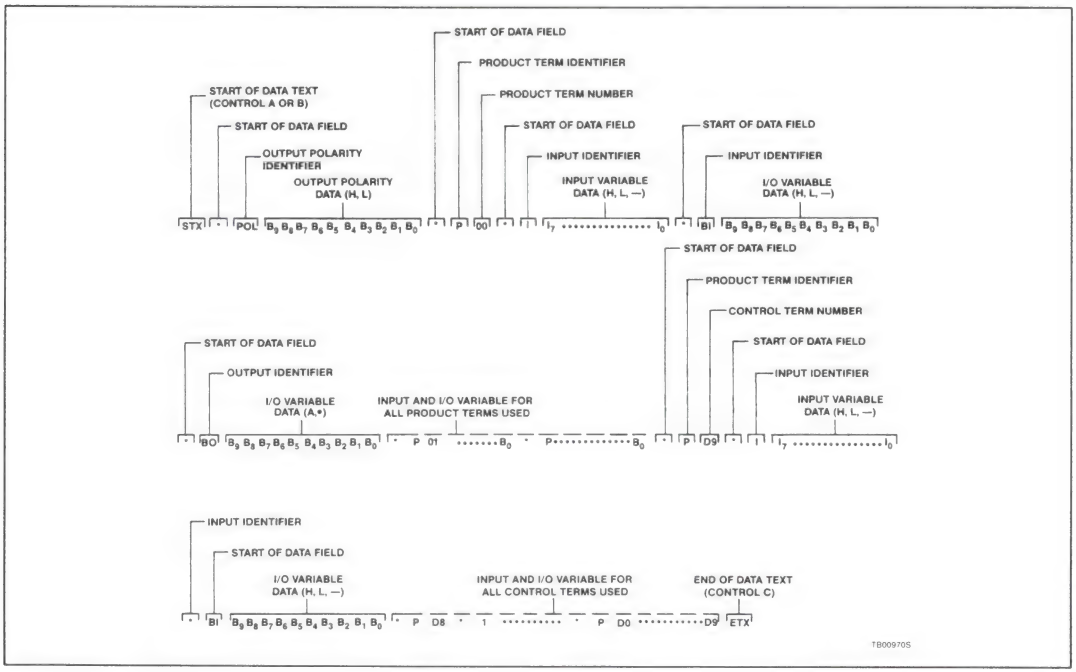

A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a (S) character, whether used or not:

—1. Customer Name
—2. Customer TWX No
—3. Data
—4. Purchase Order No
—5. Number of Program Tables
—6. Total Number of Parts

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a (S) character, whether used or not:

—1. Signetics Device No.
—2. Program Table No.
—3. Revision
—4. Date
—5. Customer Symbolized Part No.
—6. Number of Parts

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character, The body of the data consists of output polarity, product term, and output information separated by appropriate identifiers in accordance with the following format. Entries form the data fields correspond to those defined in the Logic PROGRAM TABLE.



Signetics

# PLS179

## Field Programmable Logic Sequencer (20×45×12)

*Product Specification*

**Military Standard Products**

### DESCRIPTION

The PLS179 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "foldback" inverting buffer and control gate $F_C$. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). There are 8 dedicated inputs. These yield variable I/O gate and register configurations via control gates (D, L) ranging from 20 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 8 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complementary Array output ($\overline{C}$). The Complementary Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

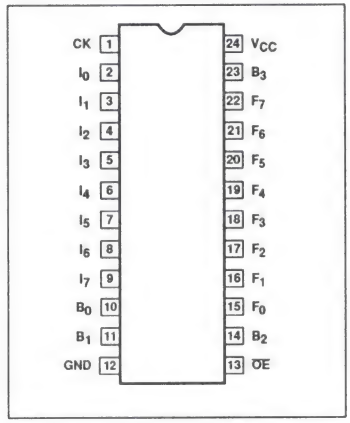
### APPLICATIONS

- Random sequential logic
- Synchronous Up/Down counters
- Shift Registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

### FEATURES

- Field-programmable (Ni-Cr link)
- 8 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J/K, T, or D-type flip-flops
- Asynchronous Preset/Reset
- Complement Array
- Active high or low outputs
- Programmable $\overline{OE}$ control
- Positive edge triggered clock
- Power-on reset on flip-flop (Fn = "1")
- Power dissipation: 725mW (typ)
- TTL Compatible

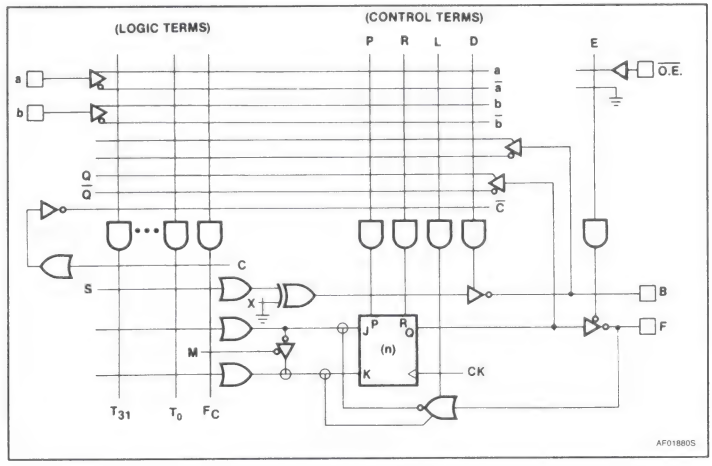
### PIN CONFIGURATION




### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 24-Pin Ceramic DIP 300-mil Wide | PLS179/BLA |

### FUNCTIONAL DIAGRAM



# Field Programmable Logic Sequencer (20×45×12) — PLS179

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. One group of AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops, as well as asynchronous Preset and Reset lines (P, R).

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (Q) and programmable output select lines (E).

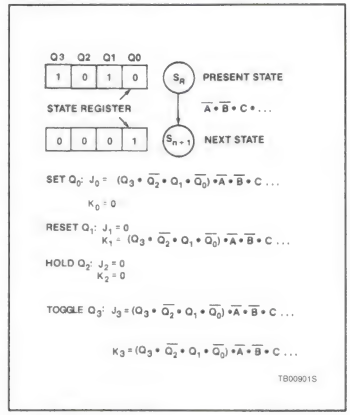
The PLS179 is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

## VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode.
5. All B pins are inputs and all F pins are outputs.

## LOGIC FUNCTION


Q3 Q2 Q1 Q0
1 0 1 0
PRESENT STATE
STATE REGISTER
0 0 0 1
NEXT STATE
SET Q0: J0 = (Q3 • Q̄2 • Q1 • Q̄0) • Ā • B̄ • C ...
K0 = 0
RESET Q1: J1 = 0
K1 = (Q3 • Q̄2 • Q1 • Q̄0) • Ā • B̄ • C ...
HOLD Q2: J2 = 0
K2 = 0
TOGGLE Q3: J3 = (Q3 • Q̄2 • Q1 • Q̄0) • Ā • B̄ • C ...
K3 = (Q3 • Q̄2 • Q1 • Q̄0) • Ā • B̄ • C ...
TB00901S

**NOTE:**
Similar logic functions are applicable for D and T mode flip-flops.

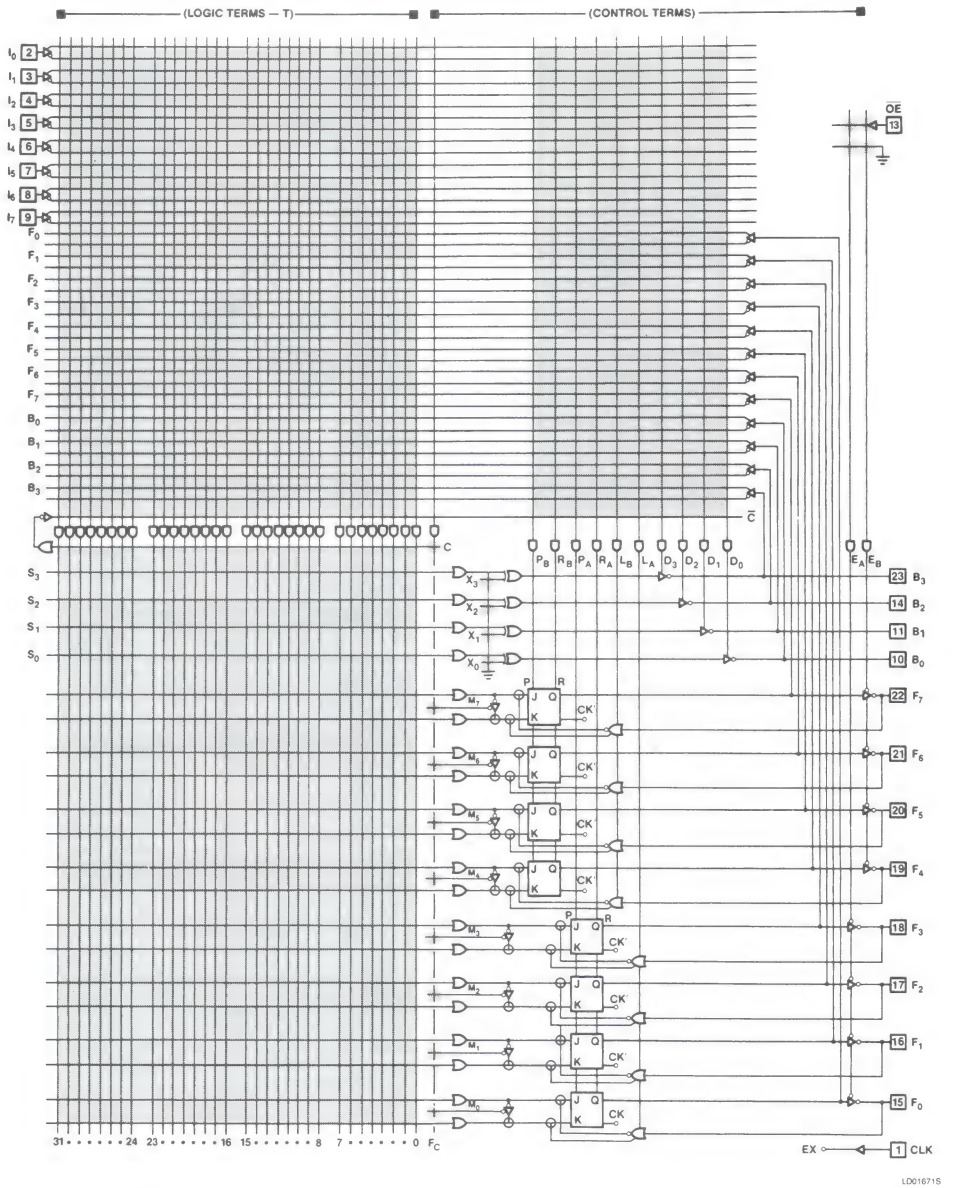
## FLIP-FLOP TRUTH TABLE

| $\overline{OE}$ | L | CK | P | R | J | K | Q | F |
|---|---|---|---|---|---|---|---|---|
| H | | | | | | | | H/Hi-Z |
| L | X | X | L | X | X | X | L | H |
| L | X | X | H | L | X | X | H | L |
| L | X | X | L | H | X | X | L | H |
| L | L | ↑ | L | L | L | L | Q | $\overline{Q}$ |
| L | L | ↑ | L | L | L | H | L | H |
| L | L | ↑ | L | L | H | L | H | L |
| L | L | ↑ | L | L | H | H | $\overline{Q}$ | Q |
| H | H | ↑ | L | L | L | H | L | H* |
| H | H | ↑ | L | L | H | L | H | L* |
| +10V | X | ↑ | X | X | L | H | L | H** |
| | X | ↑ | X | X | H | L | H | L** |

**NOTES:**

1. Positive Logic:
   $J/K = T_0 + \overline{T}_1 + T_2 + ... + T_{31}$
   $T_n = \overline{C} \bullet (I_0 \bullet I_1 \bullet I_2 ...) \bullet (Q_0 \bullet Q_1 ...) \bullet (B_0 \bullet B_1 ...)$
2. ↑ denotes transition for Low to High level.
3. X = Don't care
4. * = Forced at $F_n$ pin for loading J/K flip-flop in I/O mode. L must be enabled, and other active $T_R$ disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at $F_n$ pin to load J/K flip-flop independent of program code (Diagnostic mode).

## FPLS LOGIC DIAGRAM




1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ⊗ Programmable connection.

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | +7.0 | $V_{DC}$ |
| $V_I$ | Input voltage | +10.0 | $V_{DC}$ |
| $V_O$ | Output voltage | +5.5 | $V_{DC}$ |
| $I_I$ | Input currents | –30 to +30 | mA |
| $I_O$ | Output currents | +100 | mA |
| $t_{STG}$ | Storage temperature range | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$[15] | High-level input voltage | 2.2 | | | V |
| $V_{IL}$[15] | Low-level input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High-level output current | | | –2 | mA |
| $I_{OL}$ | Low-level output current | | | 10.0 | mA |
| $T_A$ | Operating free-air temperature range | –55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER[3] | TEST CONDITIONS[3] | LIMITS[3] | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| $V_{IK}$ | Clamp Voltage | $V_{CC}$ = MIN, $I_I = I_{IK}$ | | –0.8 | –1.2 | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $I_{OL}$ = MAX | | 0.35 | 0.5 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = MAX | 2.4 | | | V |
| | | $V_{CC}$ = MAX | | | | |
| $I_{IL}$ | Low-level output current | $V_I$ = 0.45V | | <1.0 | –100 | µA |
| $I_{IL}$ | Low-level output current (CK input) | $V_I$ = 0.45V | | –10 | –250 | µA |
| $I_{IH}$ | High-level output current | $V_I$ = 5.5V | | –50 | 40 | µA |
| | | $V_{CC}$ = MAX | | | | |
| $I_{O(OFF)}$ | Hi-Z State output current[5, 8] | $V_O$ = 5.5V | | 1 | 80 | µA |
| | | $V_O$ = 0.45V[14] | | | –140 | µA |
| $I_{OS}$ | Short circuit output current[4, 6] | $V_O$ = 0V | –15 | | –85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[7] | $V_{CC}$ = MAX | | 145 | 210 | mA |
| | | $V_{CC}$ = NOM | | | | |
| $C_{IN}$ | Input capacitance[9] | $V_I$ = 2.0V | | 8 | 12 | pF |
| $C_{OUT}$ | Output capacitance[9] | $V_O$ = 2.0V | | 15 | 19 | pF |

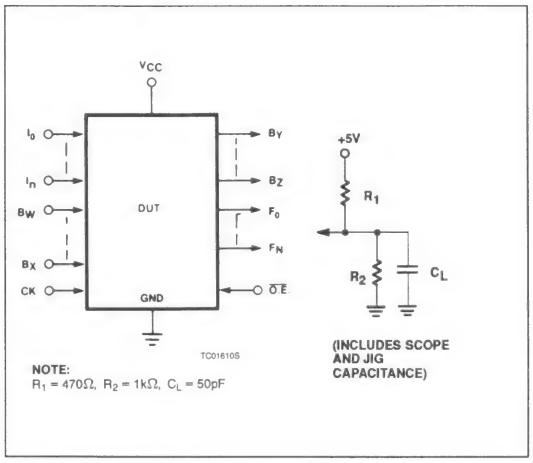
## AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min[13] | Typ[2] | Max | |
| **Pulse Width** | | | | | | | | |
| $t_{CKH}$ | Clock high[10] | CK– | CK+ | | 25 | 15 | | ns |
| $t_{CKL}$ | Clock low | CK+ | CK– | $C_L$ = 50pF | 25 | 15 | | ns |
| $t_{CKP}$ | Period[12] | CK+ | CK+ | | 65 | 45 | | ns |
| $t_{PRH}$[14] | Preset/Reset pulse | (I,B)+ | (I,B)– | | 45 | 30 | | ns |
| **Setup Time** | | | | | | | | |
| $t_{IS1}$ | Input | CK+ | (I,B)± | | 40 | 30 | | ns |
| $t_{IS2}$ | Input (through $F_n$) | CK+ | F± | $C_L$ = 50pF | 25 | 10 | | ns |
| $t_{IS3}$[14] | Input (through Complement array)[12] | CK+ | (I,B)± | | 65 | 45 | | ns |
| **Hold Time** | | | | | | | | |
| $t_{IH1}$ | Input | CK+ | (I,B)± | $C_L$ = 50pF | 0 | –5 | | ns |
| $T_{IH2}$[14] | Input (through $F_n$) | CK+ | F± | | 15 | 10 | | ns |
| **Propagation Delay** | | | | | | | | |
| $t_{CKO}$ | Clock | F± | CK+ | | | 15 | 25 | ns |
| $t_{OE1}$[14] | Output enable | F– | $\overline{OE}$– | | | 20 | 35 | ns |
| $t_{OD1}$[14] | Output disable[11] | F+ | $\overline{OE}$+ | | | 20 | 35 | ns |
| $t_{PD}$ | Output | B± | (I,B)± | | | 25 | 40 | ns |
| $t_{OE2}$[14] | Output enable | B± | (I,B)+ | $C_L$ = 50pF | | 20 | 40 | ns |
| $t_{OD2}$[14] | Output disable[11] | B+ | (I,B)– | | | 20 | 40 | ns |
| $t_{PRO}$[14] | Preset/Reset | F± | (I,B)+ | | | 35 | 50 | ns |
| $t_{PPR}$ | Power-on preset | F– | $V_{CC}$+ | | | 0 | 20 | ns |

**NOTES:**

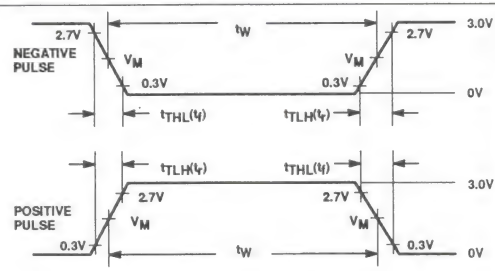
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured at $V_{IH}$ applied to $\overline{OE}$.
6. Duration of short circuit should not exceed 1 second.
7. $I_{CC}$ is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V, and the outputs open.
8. Leakage values are a combination of input and output leakage.
9. Guaranteed, but not tested.
10. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 10ns.
11. Measured at $V_T = V_{OL} + 0.5V$.
12. When using the Complement Array $T_{CKP}$ = 85ns (min.).
13. Limits are guaranteed with 12 product terms maximum connected to each sumterm line.
14. Not tested on an unprogrammed device.
15. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.

## TEST LOAD CIRCUIT




NOTE:
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 50pF$

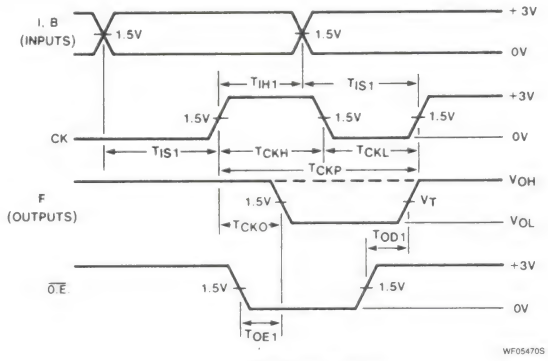
## VOLTAGE WAVEFORM



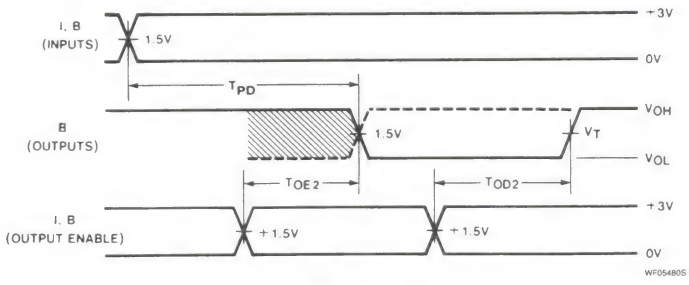

Input Pulse Definitions

| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| $V_M$ | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ≤5ns | ≤5ns |

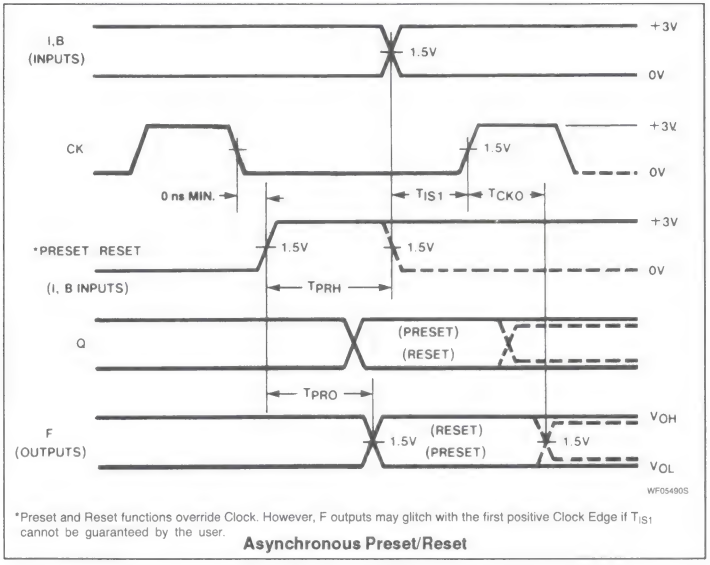
## TIMING DIAGRAMS




Flip-Flop Outputs

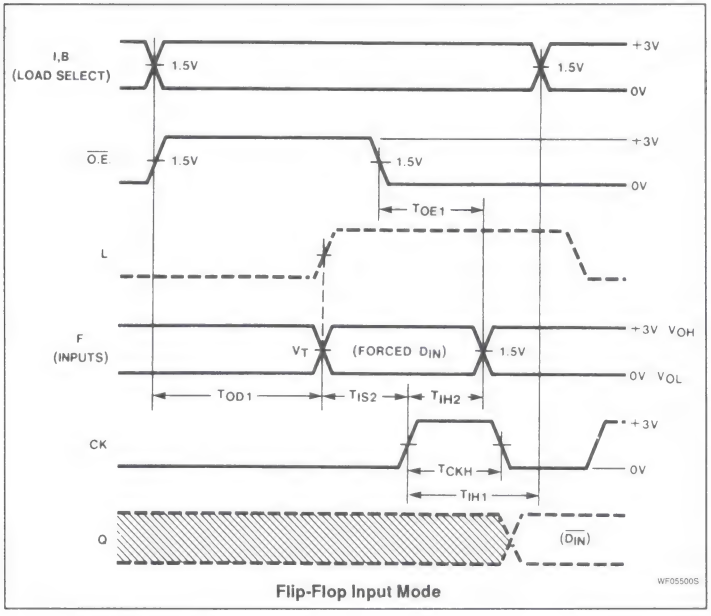



Gate Outputs




*Preset and Reset functions override Clock. However, F outputs may glitch with the first positive Clock Edge if $T_{IS1}$ cannot be guaranteed by the user.

**Asynchronous Preset/Reset**




**Flip-Flop Input Mode**

## MEMORY TIMING DEFINITIONS

| | |
|---|---|
| $t_{CKH}$ | Width of input clock pulse. |
| $t_{CKL}$ | Interval between clock pulses. |
| $t_{CKP}$ | Clock period. |
| $t_{PRH}$ | Width of preset input pulse. |
| $t_{IS1}$ | Required delay between beginning of valid input and positive transition of clock. |
| $t_{IS2}$ | Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock. |
| $t_{IH1}$ | Required delay between positive transition of clock and end of valid input data. |
| $t_{IH2}$ | Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins. |
| $t_{CKO}$ | Delay between positive transition of clock and when Outputs become valid (w/$\overline{OE}$ low). |
| $t_{OE1}$ | Delay between beginning of Output Enable Low and when Outputs become valid. |
| $t_{OD1}$ | Delay between beginning of Output Enable High and when Outputs are in the off state. |
| $t_{PD}$ | Propagation delay between combinational inputs and outputs. |
| $t_{OE2}$ | Delay between predefined Output Enable High, and when combinational Outputs become valid. |
| $t_{OD2}$ | Delay between predefined Output Enable Low and when combinational Outputs are in the off state. |
| $t_{PRO}$ | Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid. |

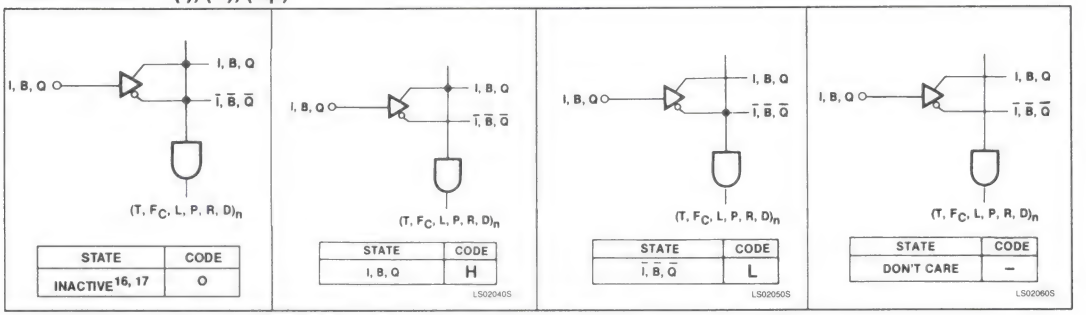
# Field Programmable Logic Sequencer (20×45×12) — PLS179

The FPLS can be programmed by means of Logic Programming equipment.

With Logic Programming, the AND/OR-EX-OR input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Tables on the following pages.

In these Tables, the logic state or action of all I/O, control and state variables are assigned a symbol which results in the proper fusing pattern of corresponding links defined as follows:

## "AND" ARRAY – (I), (B), (Qp)




| STATE | CODE |
|---|---|
| INACTIVE[16, 17] | O |

| STATE | CODE |
|---|---|
| I, B, Q | H |

LS02040S

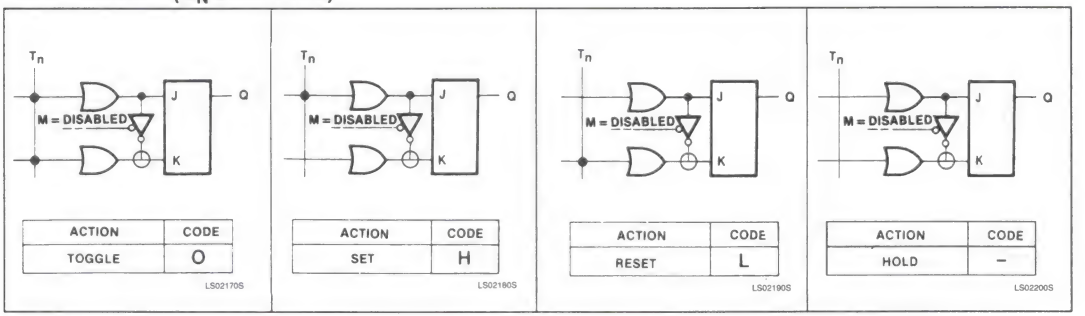
| STATE | CODE |
|---|---|
| $\overline{I}$, $\overline{B}$, $\overline{Q}$ | L |

LS02050S

| STATE | CODE |
|---|---|
| DON'T CARE | – |

LS02060S

## "AND" ARRAY – ($Q_N$ = J-K TYPE)




| ACTION | CODE |
|---|---|
| TOGGLE | O |

LS02170S

| ACTION | CODE |
|---|---|
| SET | H |

LS02180S

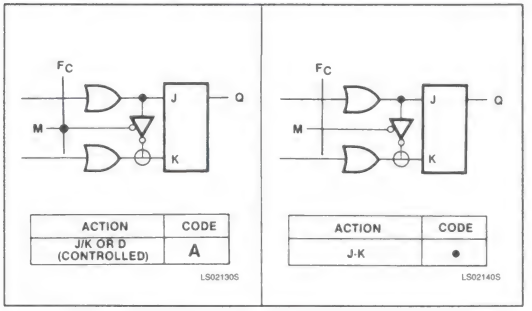
| ACTION | CODE |
|---|---|
| RESET | L |

LS02190S

| ACTION | CODE |
|---|---|
| HOLD | – |

LS02200S

## "OR" ARRAY – (MODE)



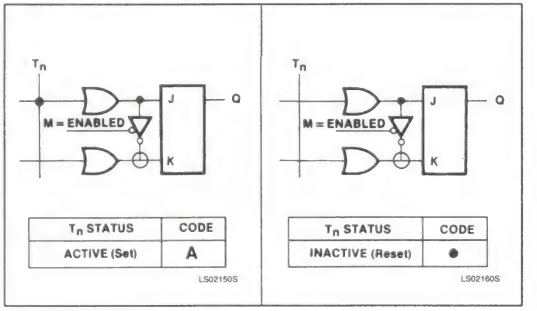

| ACTION | CODE |
|---|---|
| J/K OR D (CONTROLLED) | A |

LS02130S

| ACTION | CODE |
|---|---|
| J-K | ● |

LS02140S

## "OR" ARRAY – ($Q_N$ = D-TYPE)



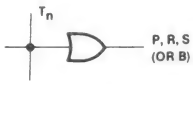

| $T_n$ STATUS | CODE |
|---|---|
| ACTIVE (Set) | A |

LS02150S

| $T_n$ STATUS | CODE |
|---|---|
| INACTIVE (Reset) | ● |

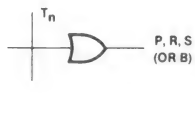
LS02160S

### "OR" ARRAY – (S or B), (P), (R)




| $T_n$ STATUS | CODE |
|---|---|
| ACTIVE | A |

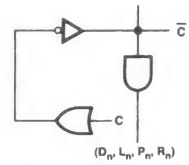
LS02210S




| $T_n$ STATUS | CODE |
|---|---|
| INACTIVE | • |

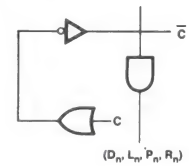
LS02220S

### "COMPLEMENT" ARRAY – MODE




| ACTION | CODE |
|---|---|
| PROPAGATE | • |

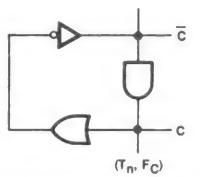
LS02110S



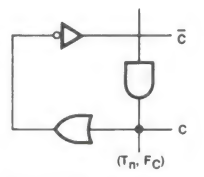

| ACTION | CODE |
|---|---|
| TRANSPARENT | – |

LS02120S

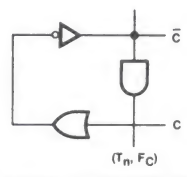
### "COMPLEMENT" ARRAY – (C)




| ACTION | CODE |
|---|---|
| INACTIVE[16, 18, 20] | O |

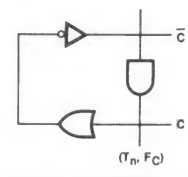



| ACTION | CODE |
|---|---|
| INACTIVE[20] | O |




| ACTION | CODE |
|---|---|
| PROPAGATE | • |

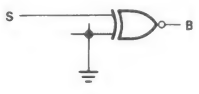
LS02090S




| ACTION | CODE |
|---|---|
| TRANSPARENT | – |

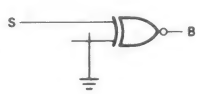
LS02100S

### "EX-OR" ARRAY – (B)




| POLARITY | CODE |
|---|---|
| LOW | L |

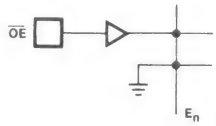
LS02230S



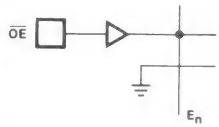

| POLARITY | CODE |
|---|---|
| HIGH | H |

LS02240S

## "OE" ARRAY – (E)

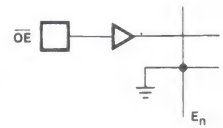



| ACTION | CODE |
|---|---|
| IDLE[16, 19] | O |

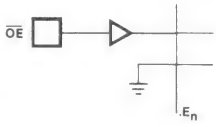



| ACTION | CODE |
|---|---|
| CONTROL | A |

LS02260S




| ACTION | CODE |
|---|---|
| ENABLE[19] | O |




| ACTION | CODE |
|---|---|
| DISABLE | – |

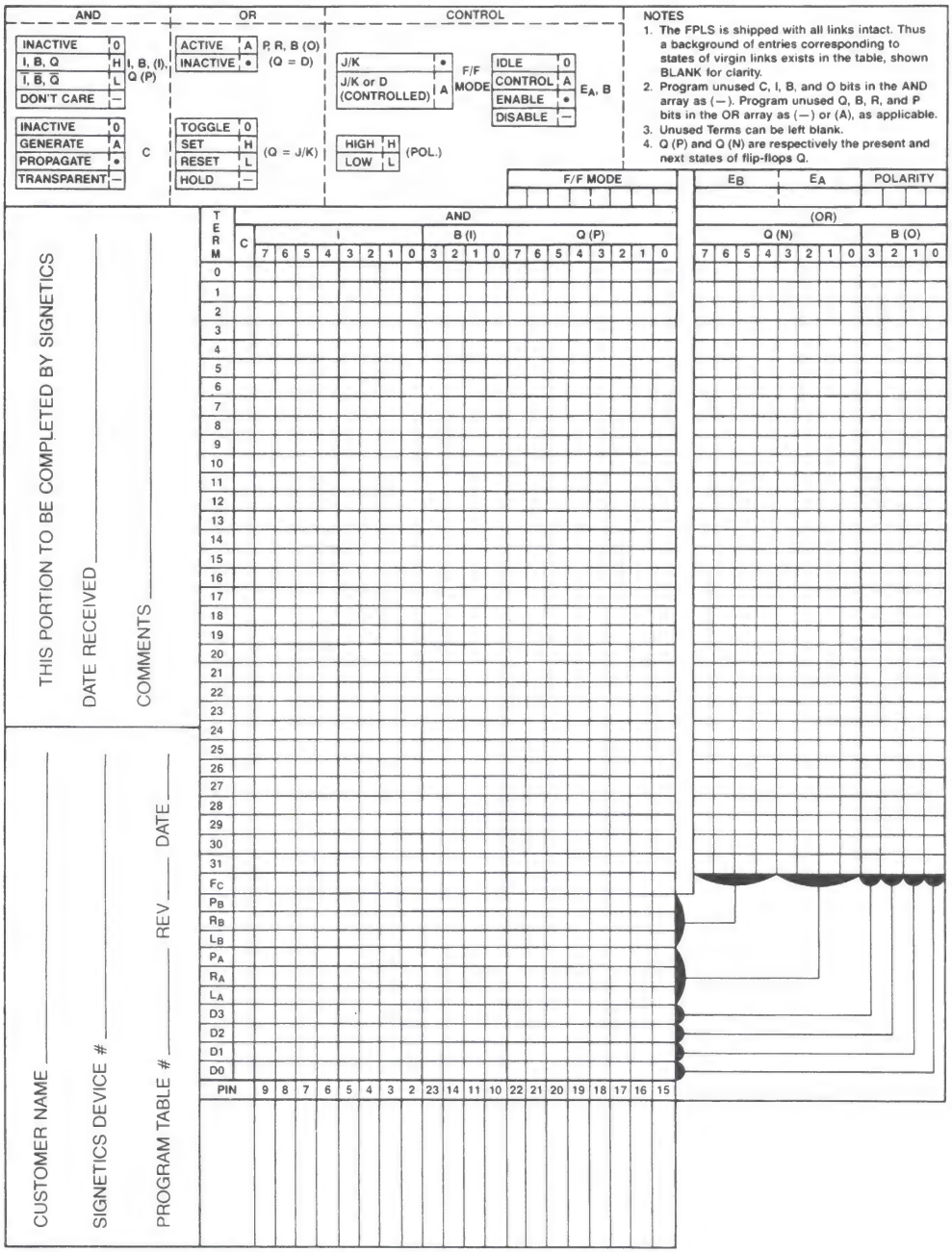
LS02280S

**NOTES:**

16. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
17. Any gate $(T, F_C, L, P, R, D)_n$ will be unconditionally inhibited if any one of the I, B, or Q link pairs are left intact.
18. To prevent oscillations, this state is not allowed for C link, pairs coupled to active gates $T_n$, $F_c$.
19. $E_n$ = O and $E_n$ = • are logically equivalent states, since both cause $F_n$ outputs to be unconditionally enabled.
20. These states are not allowed for control gates $(L, P, R, D)_n$ due to their lack of "OR" array links.

# Field Programmable Logic Sequencer (20×45×12) — PLS179

## FPLS PROGRAM TABLE


AND
OR
CONTROL
INACTIVE 0
I, B, Q H
I, B, Q L
DON'T CARE —
I, B, (I), Q (P)
INACTIVE 0
GENERATE A
PROPAGATE •
TRANSPARENT —
C
ACTIVE A
INACTIVE •
P, R, B (O) (Q = D)
TOGGLE 0
SET H
RESET L
HOLD —
(Q = J/K)
J/K •
J/K or D (CONTROLLED) A
F/F MODE
IDLE 0
CONTROL A
ENABLE •
DISABLE —
EA, B
HIGH H
LOW L
(POL.)
NOTES
1. The FPLS is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Program unused C, I, B, and O bits in the AND array as (—). Program unused Q, B, R, and P bits in the OR array as (—) or (A), as applicable.
3. Unused Terms can be left blank.
4. Q (P) and Q (N) are respectively the present and next states of flip-flops Q.
F/F MODE
EB
EA
POLARITY
THIS PORTION TO BE COMPLETED BY SIGNETICS
DATE RECEIVED
COMMENTS
CUSTOMER NAME
SIGNETICS DEVICE #
PROGRAM TABLE #
REV
DATE
TERM
C
AND
I
B (I)
Q (P)
(OR)
Q (N)
B (O)
7 6 5 4 3 2 1 0 3 2 1 0 7 6 5 4 3 2 1 0
7 6 5 4 3 2 1 0 3 2 1 0
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
FC PB RB LB PA RA LA D3 D2 D1 D0
PIN 9 8 7 6 5 4 3 2 23 14 11 10 22 21 20 19 18 17 16 15

TB01712S

Signetics

# PLUS16L8, PLUS16R8
## PAL®-Type Devices

**Signetics Programmable Logic**
***Product Specification***

**Military Application Specific Products**
- **Series 20**

## FEATURES
- **Ultra high-speed**
  - $t_{PD}$ = 10ns
  - $f_{MAX}$ = 50 MHz
  - $t_{IS}$ = 10ns
  - $t_{CKO}$ = 10ns
- **100% functionally and pin-for-pin compatible with industry standard 20-pin PAL ICs**
- **Power-up reset function to enhance state machine design and testability**
- **Design support provided via AMAZE and other CAD tools for Series 20 PAL devices**
- **Field-programmable on industry standard programmers**
- **Security fuse**
- **Individual 3-State control of all outputs**

## DESCRIPTION

The Signetics PLUS16XX family is an ultra high-speed version of existing Series 20 PAL devices.

The PLUS16XX family is 100% functional and pin-compatible with the 16L8 and 16R8 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 fixed OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8) is also provided. Proprietary designs can be protected by programming the security fuse.

The PLUS16R8 has D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art oxide isolation Bipolar fabrication process is employed to achieve high-performance operation.

The PLUS16XX family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment. See the programmer chart for qualified programmers.

The AMAZE software package from Signetics supports easy design entry for the PLUS16XX series as well as other PLD devices from Signetics. The PLUS16XX series are also supported by other standard CAD tools for PAL-type devices.

| DEVICE NUMBER | DEDICATED INPUTS | COMBINATORIAL OUTPUTS | REGISTERED OUTPUTS |
|---|---|---|---|
| PLUS16L8 | 10 | 8(6 I/O) | 0 |
| PLUS16R8 | 8 | 0 | 8 |

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 20-Pin Ceramic DIP | PLUS16L8/BRA, PLUS16R8/BRA |
| 20-Pin Ceramic Flatpack | PLUS16L8/BSA, PLUS16R8/BSA |
| 20-Pin Ceramic LLCC | PLUS16L8/B2A, PLUS16R8/B2A |

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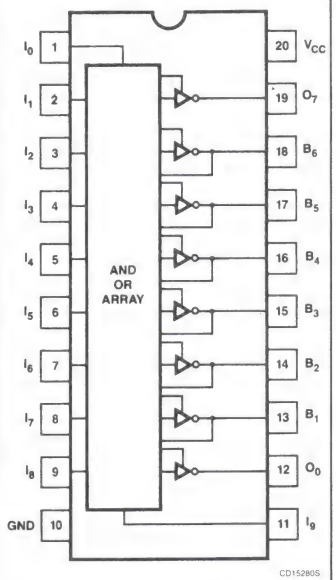
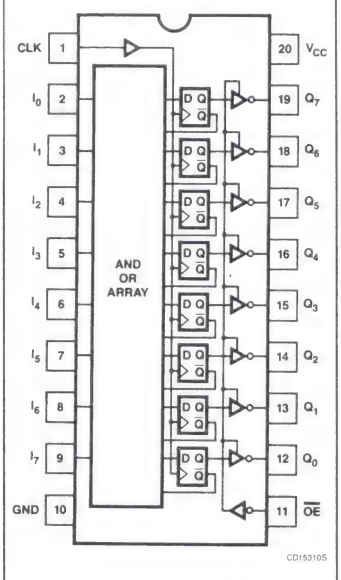
## PIN CONFIGURATIONS

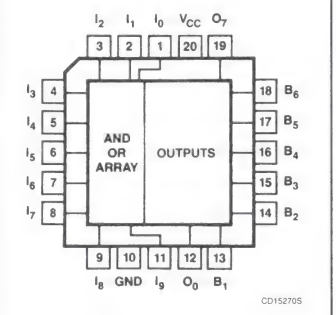
### PLUS16L8




### PLUS16R8

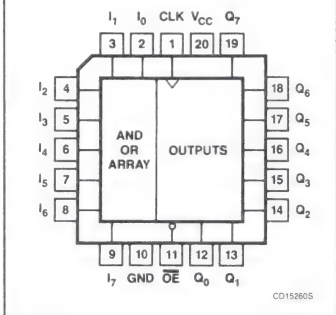



### PLUS16L8 (LLCC)




| SYMBOL | DESCRIPTION |
|---|---|
| I | Dedicated Input |
| O | Dedicated combinatorial Output |
| B | Bidirectional (input/output) |
| CLK | Clock input |
| OE | Output Enable |
| $V_{CC}$ | Supply Voltage |
| GND | Ground |

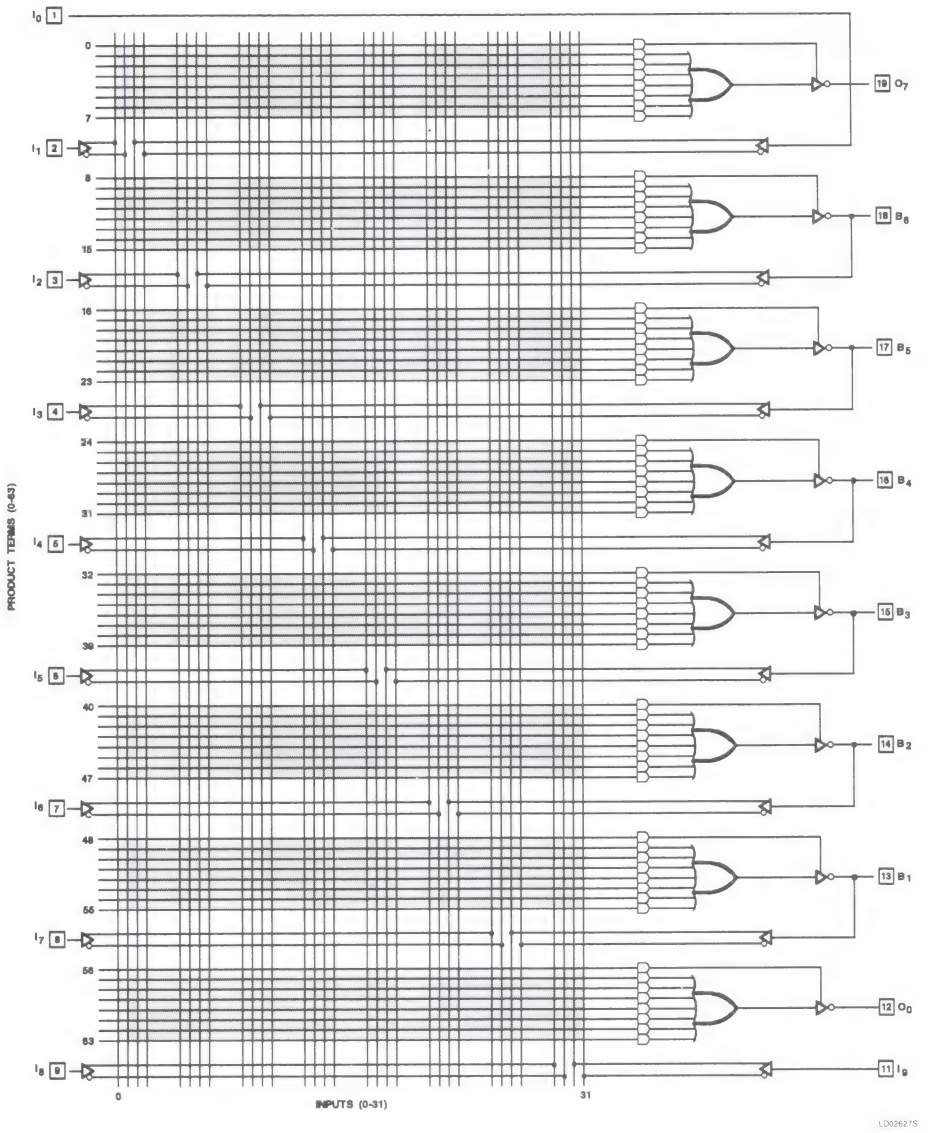
### PLUS16R8 (LLCC)




| SYMBOL | DESCRIPTION |
|---|---|
| I | Dedicated Input |
| Q | Registered output |
| B | Bidirectional (input/output) |
| CLK | Clock input |
| OE | Output Enable |
| $V_{CC}$ | Supply Voltage |
| GND | Ground |

## LOGIC DIAGRAM

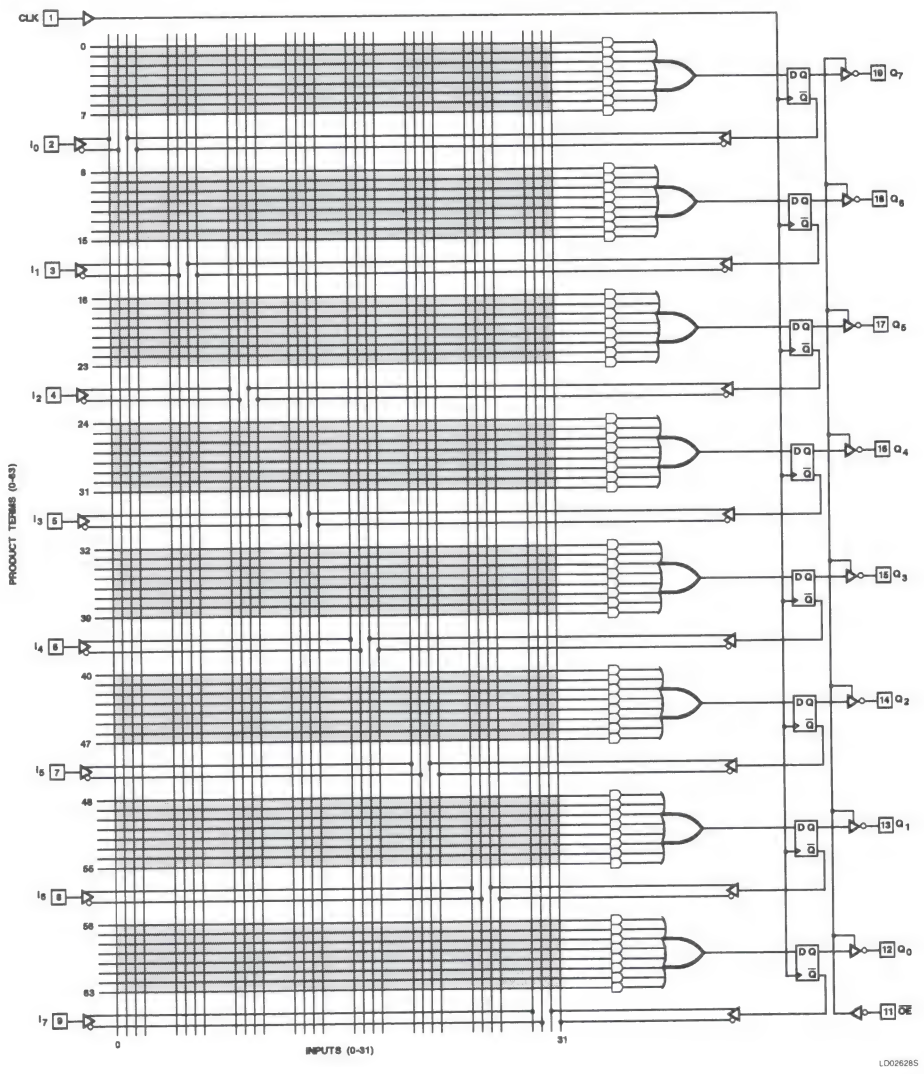
PLUS16L8




**NOTES:**
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0"
2. Programmable connections

## LOGIC DIAGRAM

PLUS16R8




**NOTES:**
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0"
2. ⊠ Programmable connections

# PAL®-Type Devices

# PLUS16L8, PLUS16R8

## FUNCTIONAL DESCRIPTIONS

The PLUS16XX series utilizes the familiar sum–of–products implementation consisting of a programmable AND array and a fixed OR array. These devices are capable of replacing an equivalent of four or more SSI/MSI integrated circuits to reduce package count and board area occupancy, consequently improving reliability and design cycle over Standard Cell or gate array options. By programming the security fuse, proprietary designs can be protected from duplication.

The PLUS16XX series consists of two PAL–type devices. Depending on the particular device type, there are a variable number of combinatorial and registered outputs available to the designer. The PLUS16L8 is a combinatorial part with 8 user configurable Bidirectional outputs, while the other device, PLUS16R8, has 8 output registers.

After programming these devices, all product terms with bits programmed will be set to the logical High state and those with both True and Complement signals unprogrammed will be set to the logical Low state.

### 3–State Outputs

The PLUS16XX series devices also feature 3–State output buffers on each output pin which can be programmed for individual control of all outputs. The registered outputs (Qn) are controlled by an external input (/OE), and the combinatorial outputs (On, Bn) use a product term to control the enable function.

### Programmable Bidirectional Pins

The PLUS16XX products feature variable Input/Output ratios. In addition to 12 dedicated inputs, each combinatorial output pin of the registered device can be individually programmed as an input or output. The PLUS16L8 provides 10 dedicated inputs and 6 Bidirectional I/O lines that can be individually configured as inputs or outputs.

### Output Registers

The PLUS16R8 has 8 output registers. Each output register is a D–type flip–flop which is loaded on the Low–to–High transition of the clock input. These output registers are capable of feeding the outputs of the registers back into the array to facilitate design of synchronous state machines.

### Power–up Reset

By resetting all flip–flops to a logic Low, as the power is turned on, the PLUS16R8 enhances state machine design and initialization capability.

### Software Support

Like other Programmable Logic Devices from Signetics, the PLUS16XX series is supported by AMAZE, the PC–based software development tool from Signetics. The PLUS16XX family of devices is also supported by standard CAD tools for PAL devices, including ABEL and CUPL.

AMAZE is available free of charge to qualified users.

### Logic Programming

Logic designs for PLUS16XX series can be generated using any commercially available JEDEC standard design software that supports the 20–pin PAL devices. No JEDEC fuse map conversion or translation is necessary when transferring designs from slower 20–pin PAL devices.

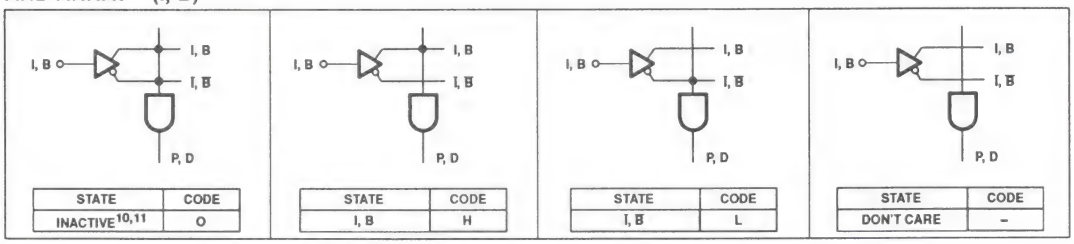
To implement the desired logic functions, each logic variable from the logic equations is assigned a symbol. True (High), Complement (Low), Don't Care and Inactive symbols are defined below.

## VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All $P_n$ terms are disabled.
3. All $P_n$ terms are active on all outputs.

## AND ARRAY – (I, B)




| STATE | CODE |
|---|---|
| INACTIVE[10,11] | O |

| STATE | CODE |
|---|---|
| I, B | H |

| STATE | CODE |
|---|---|
| I, $\overline{B}$ | L |

| STATE | CODE |
|---|---|
| DON'T CARE | – |

# PAL®-Type Devices PLUS16L8, PLUS16R8

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATINGS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | –0.5 | +7 | $V_{DC}$ |
| $V_{IN}$ | Input voltage | –0.5 | +10.0 | $V_{DC}$ |
| $V_{OUT}$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_{IN}$ | Input currents | –30 | +30 | mA |
| $I_{OUT}$ | Output currents | | +100 | mA |
| $T_{STG}$ | Storage temperature range | –65 | +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$[7] | High level Input Voltage | 2.0 | | | V |
| $V_{IL}$[7] | Low level Input Voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High level Output current | | | –2.0 | mA |
| $I_{OL}$ | Low level Output current | | | 16.0 | mA |
| $T_A$ | Operating Free–Air Temperature Range | –55 | | +125 | C° |

## DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS[3] | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_{IK}$ = Max | | –0.8 | –1.5 | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max | | | 0.5 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max | 2.4 | | | V |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_{IN}$ = 0.4V | | | –250 | µA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_{IN}$ = 2.4V | | | 25 | µA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max, $V_{IN}$ = 5.5V | | | 100 | µA |
| $I_{OLZ}$ | Off State Output Current, Low Level | $V_{CC}$ = Max, $V_{OUT}$ = 0.4V | | | –100 | µA |
| $I_{OHZ}$ | Off State Output Current, High Level | $V_{CC}$ = Max, $V_{OUT}$ = 2.4V | | | 100 | µA |
| $I_{OS}$[4,5] | Short circuit Output Current | $V_{CC}$ = Max, $V_{OUT}$ = 0.5V | –30 | | –90 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = Max | | | 210 | mA |
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 5.0V, $V_{OUT}$ = 2.0V | | 8 | | pF |
| $C_{OUT}$ | I/O | f = 1MHz, $V_{OUT}$ = 0.45V | | 8 | | pF |

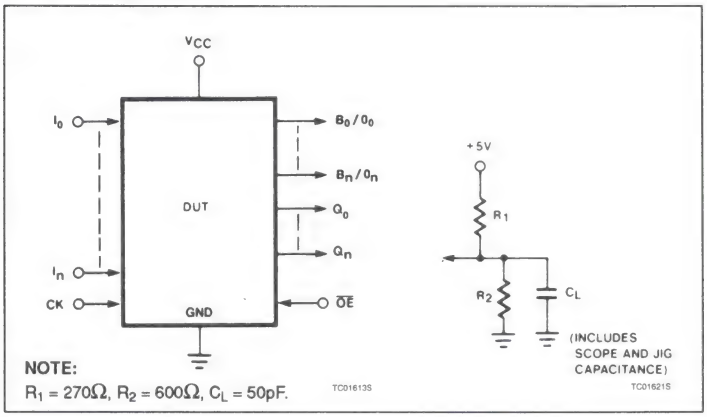
## AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TO | FROM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | |
| **PLUS16L8** | | | | | | | |
| $t_{PD}$ | Output | Q± | I, B | | | 12 | ns |
| $t_{OE2}$[8] | Output Enable | Output | I | | | 12 | ns |
| $t_{OD2}$[8] | Output Disable | Output | I | | | 12 | ns |
| **PLUS16R8** | | | | | | | |
| $t_{CKH}$ | Clock High | CK– | CK+ | 9 | | | ns |
| $t_{CKL}$ | Clock Low | CK+ | CK– | 9 | | | ns |
| $t_{CKP}$[9] | Period | Q± | I | 20 | | | ns |
| $t_{IS}$ | Input | CK+ | Input or Feedback | 10 | | | ns |
| $t_{IH}$ | Input | Input or Feedback | CK+ | 0 | | | ns |
| $t_{CKO}$ | Clock | Q± | CK+ | | | 10 | ns |
| $t_{OE1}$ | Output Enable | Q± | $\overline{OE}$ | | | 12 | ns |
| $t_{OD1}$ | Output Disable | Q± | $\overline{OE}$ | | | 12 | ns |
| $t_{PPR}$[6] | Power–up Reset | $V_{CC}$+ | Q+ | | | 12 | ns |
| $f_{MAX}$[8] | Feedback $1/(t_{IS} + t_{CKO})$<br>No Feedback $1/(t_{CKL} + t_{CKH})$ | | | 50 | | | MHz |

**NOTES:**

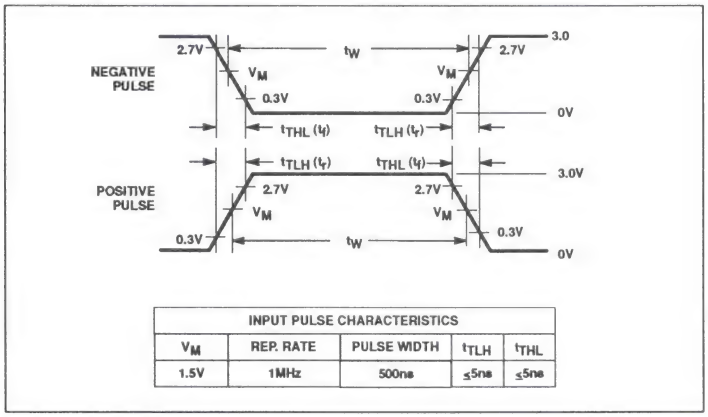
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Duration of short circuit should not exceed 1 second.
5. Tested at an address cycle time of 1µs.
6. Guaranteed but not tested.
7. These are absolute voltages with respect to device group pin and include all overshoots due to system and/or tester noise. Testing of these values require special equipment.
8. Not testable on an unprogrammed device.
9. Test guaranteed due to the testing of $t_{IS}$ and $t_{CKO}$.
10. This is the initial unprogrammed state of all links.
11. Any gate P or $D_n$ will be unconditionally inhibited if both the True and Complement fuses of any input (I or B) are left intact.

## TEST LOAD CIRCUIT



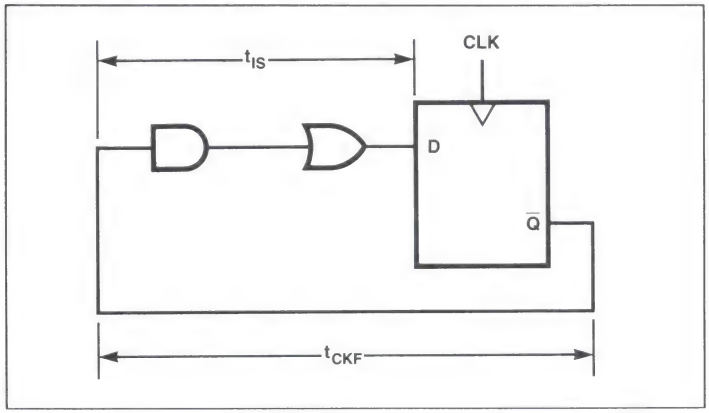

NOTE:
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

## VOLTAGE WAVEFORMS

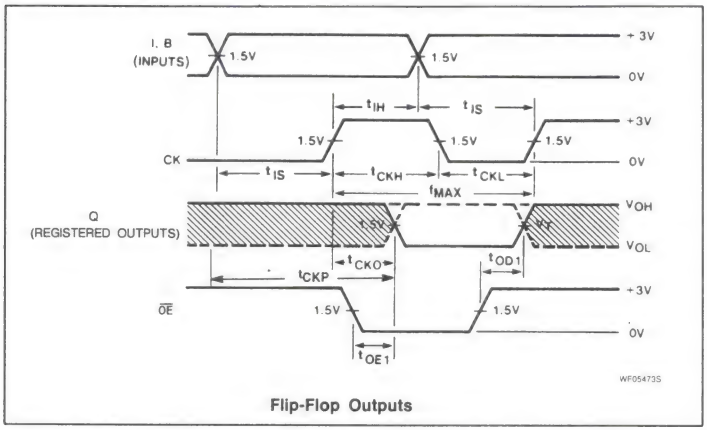



| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| $V_M$ | REP. RATE | PULSE WIDTH | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ≤5ns | ≤5ns |

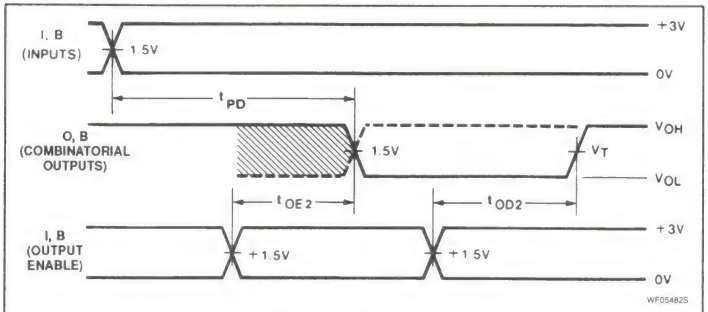
## CLOCK TO FEEDBACK PATH



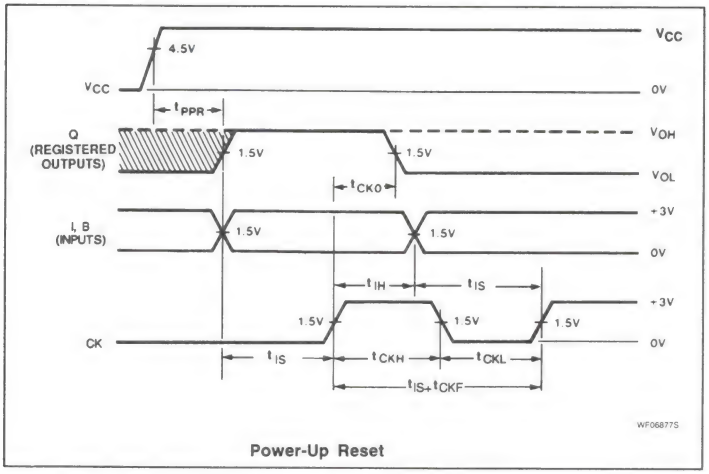
## TIMING DIAGRAMS[12,13]




Flip-Flop Outputs




Gate Outputs




Power-Up Reset

## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{CKH}$ | Width of input clock pulse. |
| $t_{CKL}$ | Interval between clock pulses. |
| $t_{CKP}$ | Clock period. |
| $t_{IS}$ | Required delay between beginning of valid input and positive transition of clock. |
| $t_{IH}$ | Required delay between positive transition of clock and end of valid input data. |
| $t_{CKF}$ | Delay between positive transition of clock and when internal $\overline{Q}$ output of flip–flop becomes valid. |
| $t_{CKO}$ | Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low). |
| $t_{OE1}$ | Delay between beginning of Output Enable Low and when outputs become valid. |
| $t_{OD1}$ | Delay between beginning of Output Enable High and when outputs are in the Off–State. |
| $t_{OE2}$ | Delay between predefined Output Enable High, and when combinational outputs become valid. |
| $t_{OD2}$ | Delay between predefined Output Enable Low and when combinational outputs are in the Off–State. |
| $t_{PPR}$ | Delay between $V_{CC}$ (after power–on) and when flip–flop outputs become preset at "1" (internal Q outputs at "0"). |
| $t_{PD}$ | Propagation delay between combinational inputs and outputs. |

## FREQUENCY DEFINITIONS

| | |
|---|---|
| $f_{MAX}$ | **No feedback:** Determined by the minimum clock period, $1/(t_{CKL} + t_{CKH})$.<br>**Internal feedback:** Determined by the internal de3lay from flip–flop outputs through the internal feedback and array to the flip–flop inputs, $1/(t_{IS} + t_{CKF})$.<br>**External feedback:** Determined by clock–to–output delay and input setup time, $1/(t_{IS} + t_{CKO})$. |

**NOTES:**
12. Input pulse amplitude is 0V to 3V.
13. Input rise and fall times are 2.5ns.

## PROGRAMMING

The PLUS16XX Series are programmable on conventional programmers for 20–pin PAL® devices. Refer to the following charts for qualified manufacturers of programmers and software tools:

| PROGRAMMER MANUFACTURER | PROGRAMMER MODEL | FAMILY/PINOUT CODES |
|---|---|---|
| DATA I/O CORPORATION<br>10525 WILLOWS ROAD, N.E.<br>P.O. BOX 97046<br>REDMOND, WASHINGTON 98073–9746<br><br>(800)247–5700 | SYSTEM 29B, LogicPak™ 303A–V04<br><br>ADAPTER 303A–011A–V08<br><br>UNISITE 40/48, V2.4<br><br>MODEL 60, 60A/H, V.13 | 16L8/16L8D : 1B/17<br>16R8/16R8D : 1B/24 |
| STAG MICROSYSTEMS, INC.<br>1600 WYATT DRIVE<br>SUITE 3<br>SANTA CLARA, CALIFORNIA 95054<br><br>(408)988–1118 | ZL30/30A PROGRAMMER<br>REV. 30A31<br><br>PPZ PROGRAMMER<br>TBA | 16L8/16L8D : 11/29<br>16R8/16R8D : 11/30 |

| SOFTWARE MANUFACTURER | DEVELOPMENT SYSTEM |
|---|---|
| SIGNETICS COMPANY<br>811 EAST ARQUES AVENUE<br>P.O. BOX 3409<br>SUNNYVALE, CALIFORNIA 94088–3409<br><br>(408)991–2000 | AMAZE SOFTWARE<br>REV. 1.7 |
| DATA I/O<br>10525 WILLOWS ROAD, N.E.<br>P.O. BOX 97046<br>REDMOND, WASHINGTON 98073–9746<br><br>(800)247–5700 | ABEL™ SOFTWARE<br>REV. 1.0 AND LATER |
| LOGICAL DEVICES, INC.<br>1201 NORTHWEST 65TH PLACE<br>FORT LAUDERDALE, FLORIDA 33309<br><br>(800)331–7766 | CUPL™ SOFTWARE<br>REV. 1.01 AND LATER |

Signetics

# PLUS20L8, PLUS20R8

## PAL®-Type Devices

**Signetics Programmable Logic**
***Product Specification***

**Military Application Specific Products**
- **Series 24**

### FEATURES

- **Ultra high-speed**
  - $t_{PD}$ = 10ns
  - $f_{MAX}$ = 50 MHz
  - $t_{IS}$ = 10ns
  - $t_{CKO}$ = 10ns
- **100% functionally and pin-for-pin compatible with industry standard 24-pin PAL ICs**
- **Power-up reset function to enhance state machine design and testability**
- **Design support provided via AMAZE and other CAD tools for Series 24 PAL devices**
- **Field-programmable on industry standard programmers**
- **Security fuse**
- **Individual 3-State control of all outputs**

### DESCRIPTION

The Signetics PLUS20XX family is an ultra high-speed version of existing Series 24 PAL devices.

The PLUS20XX family is 100% functional and pin-compatible with the 20L8 and 20R8 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 fixed OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8) is also provided. Proprietary designs can be protected by programming the security fuse.

The PLUS20R8 has D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art oxide isolation Bipolar fabrication process is employed to achieve high-performance operation.

The PLUS20XX family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment. See the programmer chart for qualified programmers.

The AMAZE software package from Signetics supports easy design entry for the PLUS20XX series as well as other PLD devices from Signetics. The PLUS20XX series are also supported by other standard CAD tools for PAL-type devices.

| DEVICE NUMBER | DEDICATED INPUTS | COMBINATORIAL OUTPUTS | REGISTERED OUTPUTS |
|---|---|---|---|
| PLUS20L8 | 14 | 8(6 I/O) | 0 |
| PLUS20R8 | 12 | 0 | 8 |

### ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 24-Pin Ceramic DIP | PLUS20L8/BLA, PLUS20R8/BLA |
| 24-Pin Ceramic Flatpack | PLUS20L8/BKA, PLUS20R8/BKA |
| 22-Pin Ceramic LLCC | PLUS20L8/B3A, PLUS20R8/B3A |

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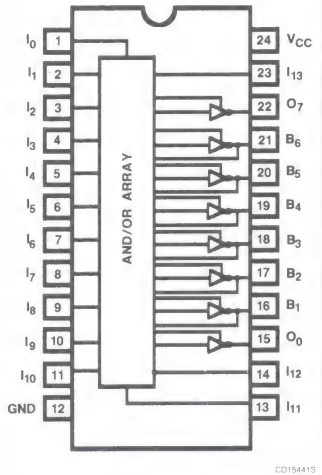
# PAL®-Type Devices

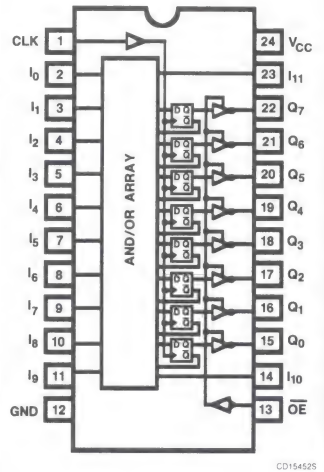
# PLUS20L8, PLUS20R8

## PIN CONFIGURATIONS

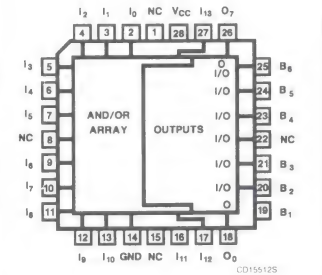
### PLUS20L8




### PLUS20R8

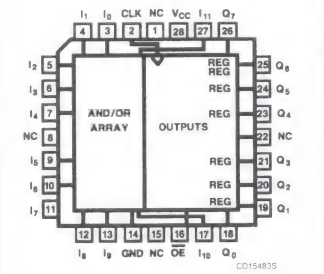



### PLUS20L8 (LLCC)




| SYMBOL | DESCRIPTION |
|---|---|
| I | Dedicated Input |
| O | Dedicated combinatorial Output |
| B | Bidirectional (input/output) |
| CLK | Clock input |
| OE | Output Enable |
| VCC | Supply Voltage |
| GND | Ground |
| NC | No Connection |

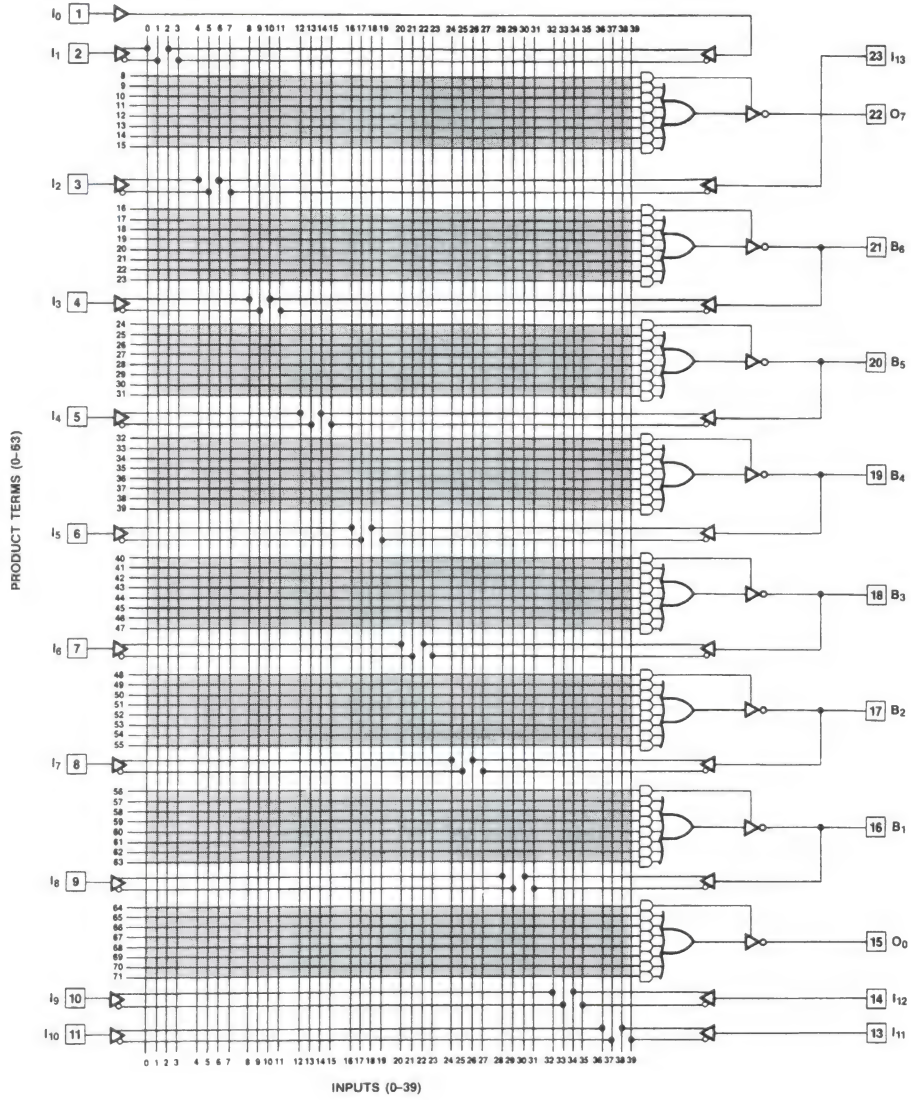
### PLUS20R8 (LLCC)




| SYMBOL | DESCRIPTION |
|---|---|
| I | Dedicated Input |
| Q | Registered output |
| B | Bidirectional (input/output) |
| CLK | Clock input |
| OE | Output Enable |
| VCC | Supply Voltage |
| GND | Ground |
| NC | No Connection |

# PAL®–Type Devices PLUS20L8, PLUS20R8

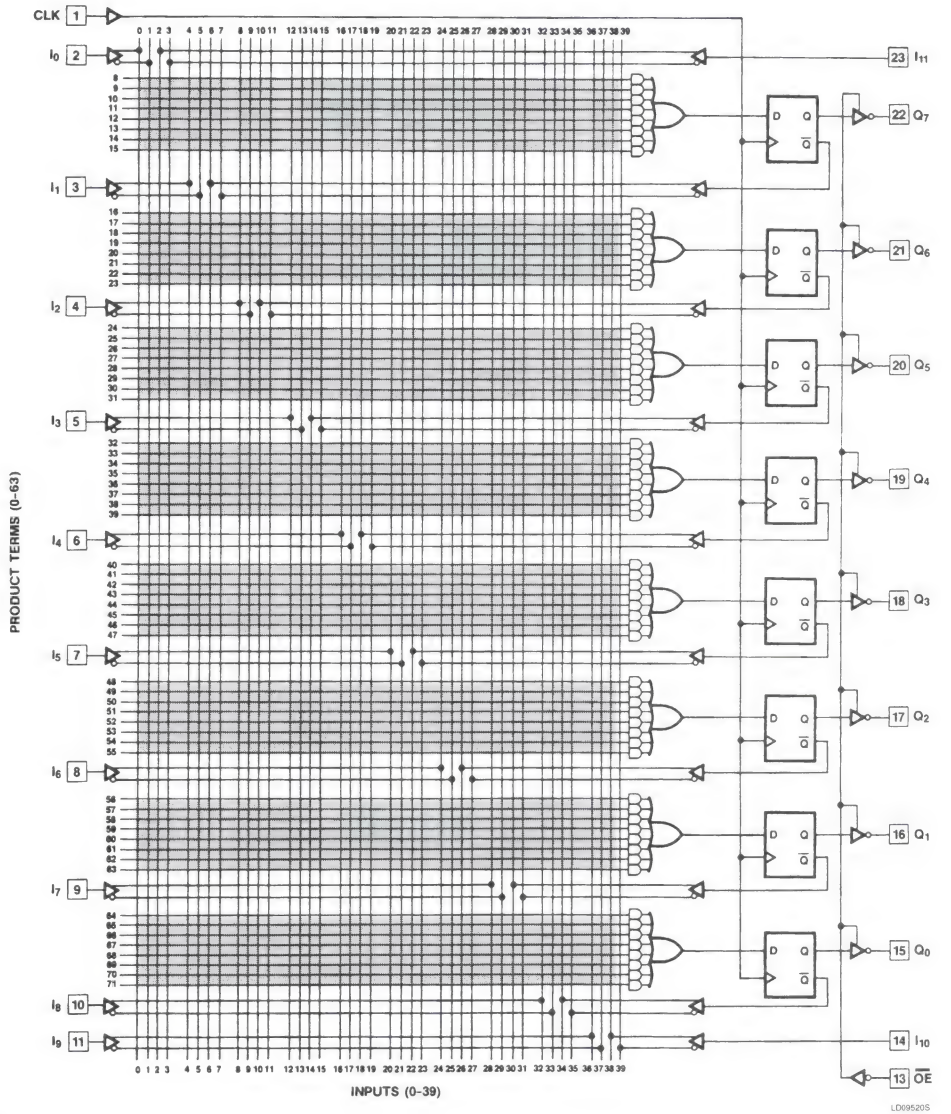
## LOGIC DIAGRAM PLUS20L8




NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0"
2. ⊠ Programmable connections

# PAL®–Type Devices PLUS20L8, PLUS20R8

## LOGIC DIAGRAM PLUS20R8




**NOTES:**
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0"
2. ▒ Programmable connections

# PAL®-Type Devices

# PLUS20L8, PLUS20R8

## FUNCTIONAL DESCRIPTIONS

The PLUS20XX series utilizes the familiar sum–of–products implementation consisting of a programmable AND array and a fixed OR array. These devices are capable of replacing an equivalent of four or more SSI/MSI integrated circuits to reduce package count and board area occupancy, consequently improving reliability and design cycle over Standard Cell or gate array options. By programming the security fuse, proprietary designs can be protected from duplication.

The PLUS20XX series consists of two PAL–type devices. Depending on the particular device type, there are a variable number of combinatorial and registered outputs available to the designer. The PLUS20L8 is a combinatorial part with 8 user configurable Bidirectional outputs, while the other device, PLUS20R8, has 8 output registers.

After programming these devices, all product terms with bits programmed will be set to the logical High state and those with both True and Complement signals unprogrammed will be set to the logical Low state.

### 3–State Outputs

The PLUS20XX series devices also feature 3–State output buffers on each output pin which can be programmed for individual control of all outputs. The registered outputs (Qn) are controlled by an external input (/OE), and the combinatorial outputs (On, Bn) use a product term to control the enable function.

### Programmable Bidirectional Pins

The PLUS20XX products feature variable Input/Output ratios. In addition to 12 dedicated inputs, each combinatorial output pin of the registered device can be individually programmed as an input or output. The PLUS20L8 provides 14 dedicated inputs and 6 Bidirectional I/O lines that can be individually configured as inputs or outputs.

### Output Registers

The PLUS20R8 has 8 output registers. Each output register is a D–type flip–flop which is loaded on the Low–to–High transition of the clock input. These output registers are capable of feeding the outputs of the registers back into the array to facilitate design of synchronous state machines.

### Power–up Reset

By resetting all flip–flops to a logic Low, as the power is turned on, the PLUS20R8 enhances state machine design and initialization capability.

### Software Support

Like other Programmable Logic Devices from Signetics, the PLUS20XX series are supported by AMAZE, the PC–based software development tool from Signetics. The PLUS20XX family of devices are also supported by standard CAD tools for PAL devices, including ABEL and CUPL.

AMAZE is available free of charge to qualified users.

### Logic Programming

Logic designs for PLUS20XX series can be generated using any commercially available JEDEC standard design software that supports the 24–pin PAL devices. No JEDEC fuse map conversion or translation is necessary when transferring designs from slower 24–pin PAL devices.

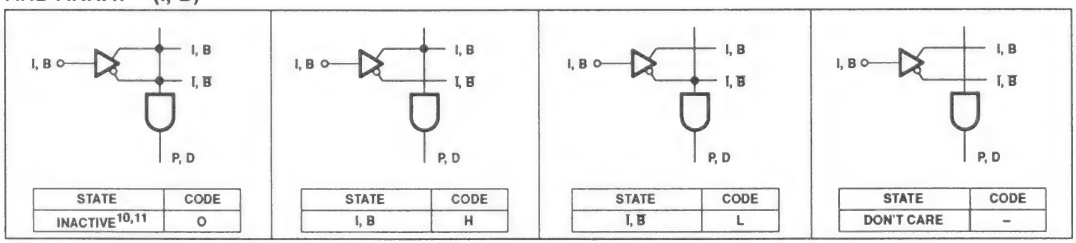
To implement the desired logic functions, each logic variable from the logic equations is assigned a symbol. True (High), Complement (Low), Don't Care and Inactive symbols are defined below.

## VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All $P_n$ terms are disabled.
3. All $P_n$ terms are active on all outputs.

### AND ARRAY – (I, B)




| STATE | CODE |
|---|---|
| INACTIVE[10,11] | O |

| STATE | CODE |
|---|---|
| I, B | H |

| STATE | CODE |
|---|---|
| $\overline{I, B}$ | L |

| STATE | CODE |
|---|---|
| DON'T CARE | – |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATINGS | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | –0.5 | +7 | $V_{DC}$ |
| $V_{IN}$ | Input voltage | –0.5 | +5.5 | $V_{DC}$ |
| $V_{OUT}$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_{IN}$ | Input currents | –30 | +30 | mA |
| $I_{OUT}$ | Output currents | | +100 | mA |
| $T_{STG}$ | Storage temperature range | –65 | +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$[7] | High level Input Voltage | 2.0 | | | V |
| $V_{IL}$[7] | Low level Input Voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High level Output current | | | –2.0 | mA |
| $I_{OL}$ | Low level Output current | | | 16.0 | mA |
| $T_A$ | Operating Free–Air Temperature Range | –55 | | +125 | C° |

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5 \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS[3] | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_{IK}$ = Max | | –0.8 | –1.5 | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max | | | 0.5 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max | 2.4 | | | V |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_{IN}$ = 0.4V | | | –250 | µA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_{IN}$ = 2.4V | | | 25 | µA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max, $V_{IN}$ = 5.5V | | | 100 | µA |
| $I_{OLZ}$ | Off State Output Current, Low Level | $V_{CC}$ = Max, $V_{OUT}$ = 0.4V | | | –100 | µA |
| $I_{OHZ}$ | Off State Output Current, High Level | $V_{CC}$ = Max, $V_{OUT}$ = 2.4V | | | 100 | µA |
| $I_{OS}$[4,5] | Short circuit Output Current | $V_{CC}$ = Max, $V_{OUT}$ = 0.5V | –30 | | –90 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = Max | | | 210 | mA |
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 5.0V, $V_{OUT}$ = 2.0V | | 8 | | pF |
| $C_{OUT}$ | I/O | f = 1MHz, $V_{OUT}$ = 0.45V | | 8 | | pF |

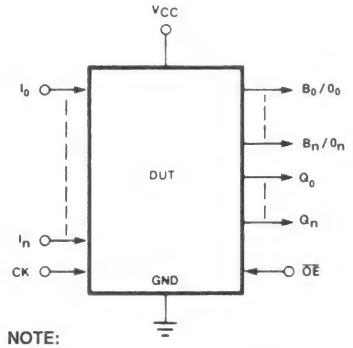
## AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5 \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TO | FROM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | |
| **PLUS20L8** | | | | | | | |
| $t_{PD}$ | Output | Q± | I, B | | | 10 | ns |
| $t_{OE2}$[8] | Output Enable | Output | I | | | 12 | ns |
| $t_{OD2}$[8] | Output Disable | Output | I | | | 12 | ns |
| **PLUS20R8** | | | | | | | |
| $t_{CKH}$ | Clock High | CK– | CK+ | 10 | | | ns |
| $t_{CKL}$ | Clock Low | CK+ | CK– | 10 | | | ns |
| $t_{CKP}$[9] | Period | Q± | I | 20 | | | ns |
| $t_{IS}$ | Input | CK+ | Input or Feedback | 10 | | | ns |
| $t_{IH}$ | Input | Input or Feedback | CK+ | 0 | | | ns |
| $t_{CKO}$ | Clock | Q± | CK+ | | | 10 | ns |
| $t_{OE1}$ | Output Enable | Q± | $\overline{OE}$ | | | 12 | ns |
| $t_{OD1}$ | Output Disable | Q± | $\overline{OE}$ | | | 12 | ns |
| $t_{PPR}$[6] | Power–up Reset | $V_{CC}$+ | Q+ | | | 12 | ns |
| $f_{MAX}$[8] | Feedback $1/(t_{IS} + t_{CKO})$<br>No Feedback $1/(t_{CKL} + t_{CKH})$ | | | 50 | | | MHz |

**NOTES:**

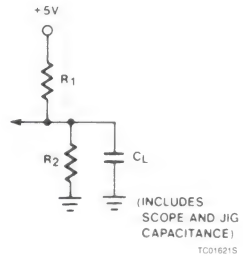
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Duration of short circuit should not exceed 1 second.
5. Tested at an address cycle time of 1µs.
6. Guaranteed but not tested.
7. These are absolute voltages with respect to device group pin and include all overshoots due to system and/or tester noise. Testing of these values require special equipment.
8. Not testable on an unprogrammed device.
9. Test guaranteed due to the testing of $t_{IS}$ and $t_{CKO}$.
10. This is the initial unprogrammed state of all links.
11. Any gate P or $D_n$ will be unconditionally inhibited if both the True and Complement fuses of any input (I or B) are left intact.

## TEST LOAD CIRCUIT



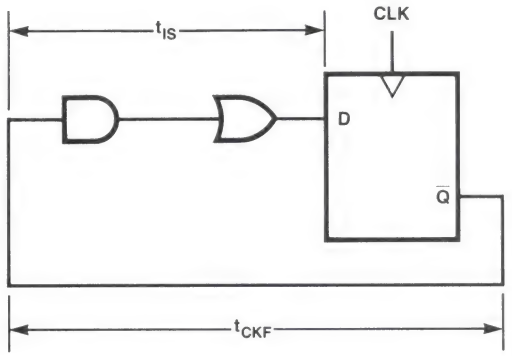

NOTE:
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

TC01613S

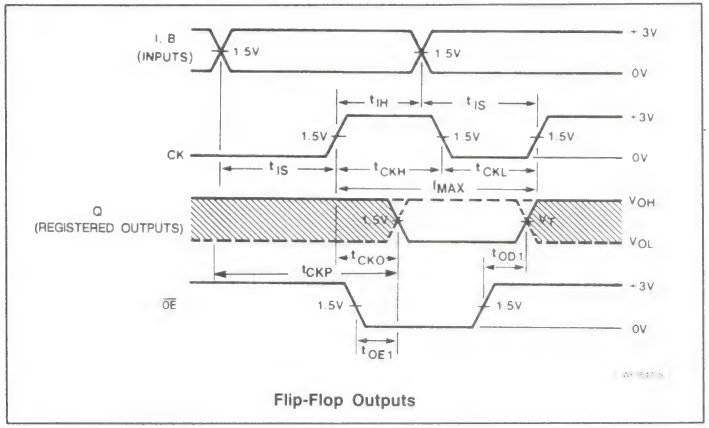



TC01621S

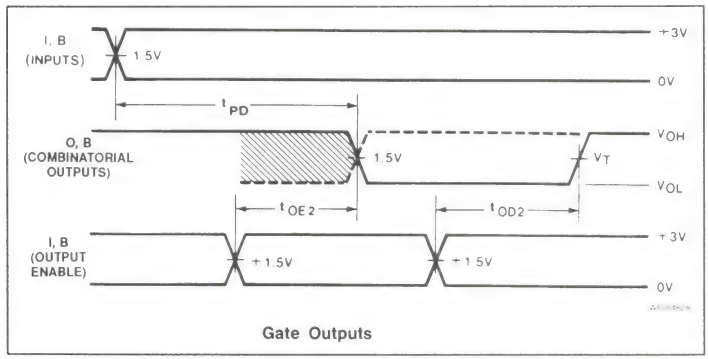
## CLOCK TO FEEDBACK PATH



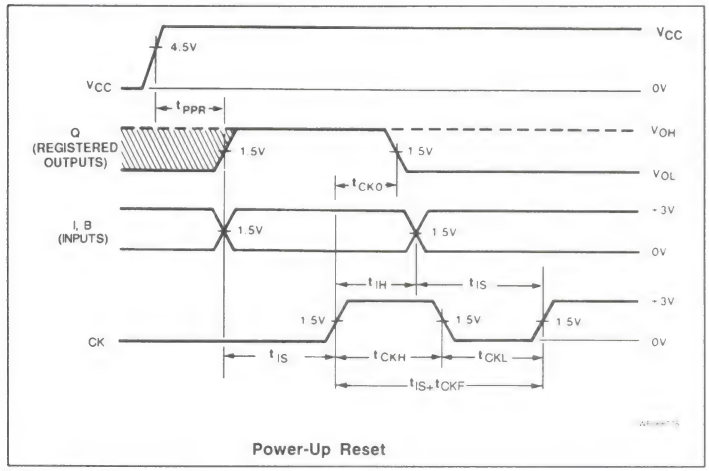
## TIMING DIAGRAMS[12,13]




Flip-Flop Outputs




Gate Outputs




Power-Up Reset

**NOTES:**
12. Input pulse amplitude is 0V to 3V.
13. Input rise and fall times are 2.5ns.

## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{CKH}$ | Width of input clock pulse. |
| $t_{CKL}$ | Interval between clock pulses. |
| $t_{CKP}$ | Clock period. |
| $t_{IS}$ | Required delay between beginning of valid input and positive transition of clock. |
| $t_{IH}$ | Required delay between positive transition of clock and end of valid input data. |
| $t_{CKF}$ | Delay between positive transition of clock and when internal $\overline{Q}$ output of flip–flop becomes valid. |
| $t_{CKO}$ | Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low). |
| $t_{OE1}$ | Delay between beginning of Output Enable Low and when outputs become valid. |
| $t_{OD1}$ | Delay between beginning of Output Enable High and when outputs are in the Off–State. |
| $t_{OE2}$ | Delay between predefined Output Enable High, and when combinational outputs become valid. |
| $t_{OD2}$ | Delay between predefined Output Enable Low and when combinational outputs are in the Off–State. |
| $t_{PPR}$ | Delay between $V_{CC}$ (after power–on) and when flip–flop outputs become preset at "1" (internal Q outputs at "0"). |
| $t_{PD}$ | Propagation delay between combinational inputs and outputs. |

## FREQUENCY DEFINITIONS

| | |
|---|---|
| $f_{MAX}$ | **No feedback:** Determined by the minimum clock period, $1/(t_{CKL} + t_{CKH})$. **External feedback:** Determined by clock–to–output delay and input setup time, $1/(t_{IS} + t_{CKO})$. |

## PROGRAMMING

The PLUS20XX Series are programmable on conventional programmers for 24–pin PAL® devices. Refer to the following charts for qualified manufacturers of programmers and software tools:

| PROGRAMMER MANUFACTURER | PROGRAMMER MODEL | FAMILY/PINOUT CODES |
|---|---|---|
| DATA I/O CORPORATION<br>10525 WILLOWS ROAD, N.E.<br>P.O. BOX 97046<br>REDMOND, WASHINGTON 98073–9746<br><br>(800)247–5700 | SYSTEM 29B, LogicPak™ 303A–V04 .<br><br>ADAPTER 303A–011A–V08<br><br>UNISITE 40/48, V2.4<br><br>MODEL 60, 60A/H, V.13 | 20L8/20L8D : 1B/26<br>20R8/20R8D : 1B/27 |
| STAG MICROSYSTEMS, INC.<br>1600 WYATT DRIVE<br>SUITE 3<br>SANTA CLARA, CALIFORNIA 95054<br><br>(408)988–1118 | ZL30/30A PROGRAMMER<br>REV. 30A31<br><br>PPZ PROGRAMMER<br>TBA | 20L8/20L8D : 11/56<br>20R8/20R8D : 11/57 |

| SOFTWARE MANUFACTURER | DEVELOPMENT SYSTEM |
|---|---|
| SIGNETICS COMPANY<br>811 EAST ARQUES AVENUE<br>P.O. BOX 3409<br>SUNNYVALE, CALIFORNIA 94088–3409<br><br>(408)991–2000 | AMAZE SOFTWARE<br>REV. 1.7 |
| DATA I/O<br>10525 WILLOWS ROAD, N.E.<br>P.O. BOX 97046<br>REDMOND, WASHINGTON 98073–9746<br><br>(800)247–5700 | ABEL™ SOFTWARE<br>REV. 1.0 AND LATER |
| LOGICAL DEVICES, INC.<br>1201 NORTHWEST 65TH PLACE<br>FORT LAUDERDALE, FLORIDA 33309<br><br>(800)331–7766 | CUPL™ SOFTWARE<br>REV. 1.01 AND LATER |

Signetics

# PLUS405
## Field-Programmable Logic Sequencer (16×64×8)

**Signetics Programmable Logic**
***Product Specification***

**Military**
**Application Specific Products**

- **Series 28**

## DESCRIPTION

The PLUS405 device is a bipolar programmable state machine of the Mealy type. Both the AND and the OR arrays are user-programmable. All 64 AND gates are connected to the 16 external dedicated inputs ($I_0$ - $I_{15}$) and to the feedback paths of the 8 on-chip State Registers ($Q_{P0}$ - $Q_{P7}$). Two complement arrays support complex IF-THEN-ELSE state transitions with a single product term (input variables $C_0$, $C_1$).

All state transition terms can include True, False, or Don't Care states of the controlling state variables. All AND gates are merged into the programmable OR array to issue the next-state and next-output commands to their respective register. Because the OR array is programmable, any one or all of the 64 transition terms can be connected to any or all of the State and Output Registers.

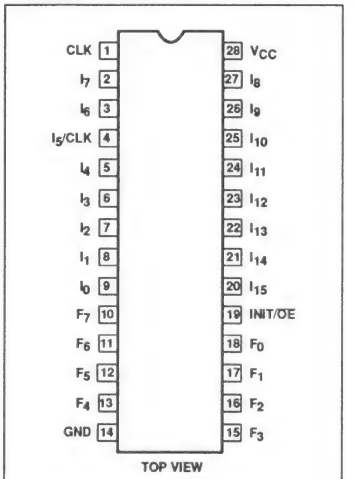
All state ($Q_{P0}$ - $Q_{P7}$) and output ($Q_{F0}$ - $Q_{F7}$) registers are edge-triggered, clocked J-K flip-flops, with Asynchronous Preset and Reset options. The PLUS405 architecture provides the added flexibility of the J-K toggle function which is indeterminate on S-R flip-flops. Each register may be individually programmed such that a specific Preset-Reset pattern is initialized when the initialization pin is raised to a logic level "1". This feature allows the state machine to be asynchronously initialized to known internal state and output conditions prior to proceeding through a sequence of state transitions. Upon power-up, all registers are unconditionally preset to "1". If desired, the initialization input pin (INIT) can be converted to an $\overline{\text{Output Enable}}$ ($\overline{OE}$) function as an additional user-programmable feature.

Availability of two user-programmable clocks allows the user to design two independently clocked state machine functions consisting of four state and four output bits each.

## FEATURES

- **50 and 58.8MHz clock rates $T_{CKM}$**
- **$f_{MAX}$ = 30MHz ($1/(t_{IS1} + t_{CKO1})$)**
- **Functional superset of PLS105/105A**
- **Field-programmable (TI-W fusible link)**
- **16 input variables**
- **8 output functions**
- **64 transition terms**
- **8-bit State Register**
- **8-bit Output Register**
- **2 transition Complement Array terms**
- **Multiple clocks***
- **Programmable Asynchronous Initialization or $\overline{\text{Output Enable}}$**
- **Power-on preset of all registers to "1"**
- **"On-chip" diagnostic test mode features for access to state and output registers**
- **950mW power dissipation (typical)**
- **TTL compatible**
- **J-K or S-R flip-flop functions**
- **Automatic "Hold" states**
- **3-State outputs**

## PIN CONFIGURATION




TOP VIEW

For LLCC pin assignments see JEDEC Standard 21.

## APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 28–Pin Ceramic DIP 600mil–wide | PLUS405/BXA |
| 28–Pin Ceramic Leadless Chip Carrier | PLUS405/B3A |
| 28–Pin Ceramic Flat Pack | PLUS405/BYA |

* Refer to AC Specifications for clock and operating frequencies when using multiple clocks.

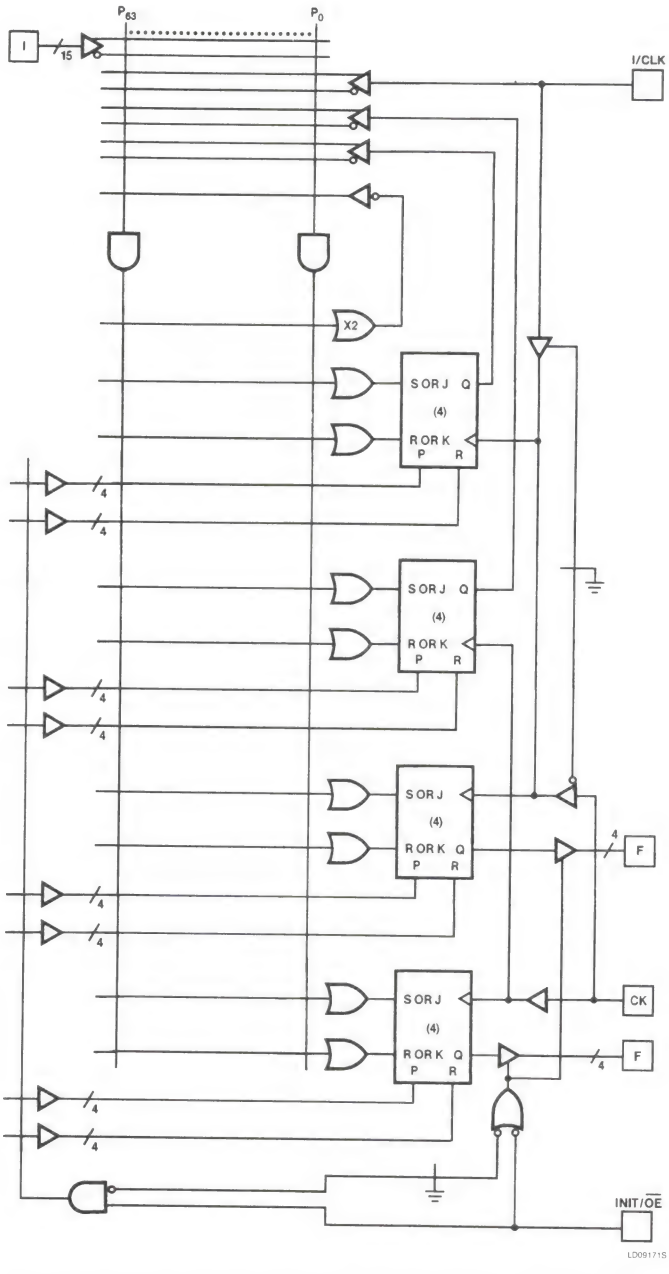
# Field-Programmable Logic Sequencer (16×64×8) PLUS405

## PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION | POLARITY |
|---|---|---|---|
| 1 | CLK1 | **Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers. Pin 1 only clocks $P_{0-3}$ and $F_{0-3}$ if Pin 4 is also being used as a clock. | Active-High (H) |
| 2, 3, 5 - 9, 26 - 27 20 - 22 | $I_0$ - $I_4$, $I_7$, $I_6$, $I_8$ - $I_9$ $I_{13}$ - $I_{15}$ | **Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L". | Active-High/Low (H/L) |
| 4 | $I_5$/CLK2 | **Logic Input/Clock:** A user programmable function: | |
| | | • **Logic Input**: A 13th external logic input to the AND array, as above. | Active-High/Low (H/L) |
| | | • **Clock**: A 2nd clock for the State Registers $P_{4-7}$ and Output Registers $F_{4-7}$, as above. Note that input buffer $I_5$ must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using Pin 4 as a Clock. | Active-High (H) |
| 23 | $I_{12}$ | **Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL levels. When $I_{12}$ is held at +10V, device outputs $F_0$ - $F_7$ reflect the contents of State Register bits $P_0$ - $P_7$. The contents of each Output Register remains unaltered. | Active-High/Low (H/L) |
| 24 | $I_{11}$ | **Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When $I_{11}$ is held at +10V, device outputs $F_0$ - $F_7$ become direct inputs for State Register bits $P_0$ - $P_7$; a Low-to-High transition on the appropriate clock line loads the values on pins $F_0$ - $F_7$ into the State Register bits $P_0$ - $P_7$. The contents of each Output Register remains unaltered. | Active-High/Low (H/L) |
| 25 | $I_{10}$ | **Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When $I_{10}$ is held at +10V, device outputs $F_0$ - $F_7$ become direct inputs for Output Register bits $Q_0$ - $Q_7$; a Low-to-High transition on the appropriate clock line loads the values on pins $F_0$ - $F_7$ into the Output Register bits $Q_0$ - $Q_7$. The contents of each State Register remains unaltered. | Active-High/Low (H/L) |
| 10 - 13 15 - 18 | $F_0$ - $F_7$ | **Logic Outputs/Diagnostic Outputs/Diagnostic Inputs**: Eight device outputs which normally reflect the contents of Output Register Bits $Q_0$ - $Q_7$, when enabled. When $I_{12}$ is held at +10V, $F_0$ - $F_7$ = ($P_0$ - $P_7$). When $I_{11}$ is held at +10V, $F_0$ - $F_7$ become inputs to State Register bits $P_0$ - $P_7$. When $I_{10}$ is held at +10V, $F_0$ - $F_7$ become inputs to Output Register bits $Q_0$ - $Q_7$. | Active-High (H) |
| 19 | INIT/$\overline{OE}$ | **Initialization or $\overline{\text{Output Enable}}$ Input:** **A user-programmable function:** | |
| | | • **Initialization**: Provides an asynchronous preset to logic "1" or reset to logic "0" of all State and Output Register bits, determined individually for each register bit through user programming. INIT overrides Clock, and when held High, clocking is inhibited and $F_0$ - $F_7$ are in their initialization state. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after INIT goes Low. See timing definition for $t_{VCK}$ and $t_{NVCK}$. | Active-High (H) |
| | | • **$\overline{\text{Output Enable}}$**: Provides an output enable function to buffers $F_0$ - $F_7$ from the Output Registers. | Active-Low (L) |

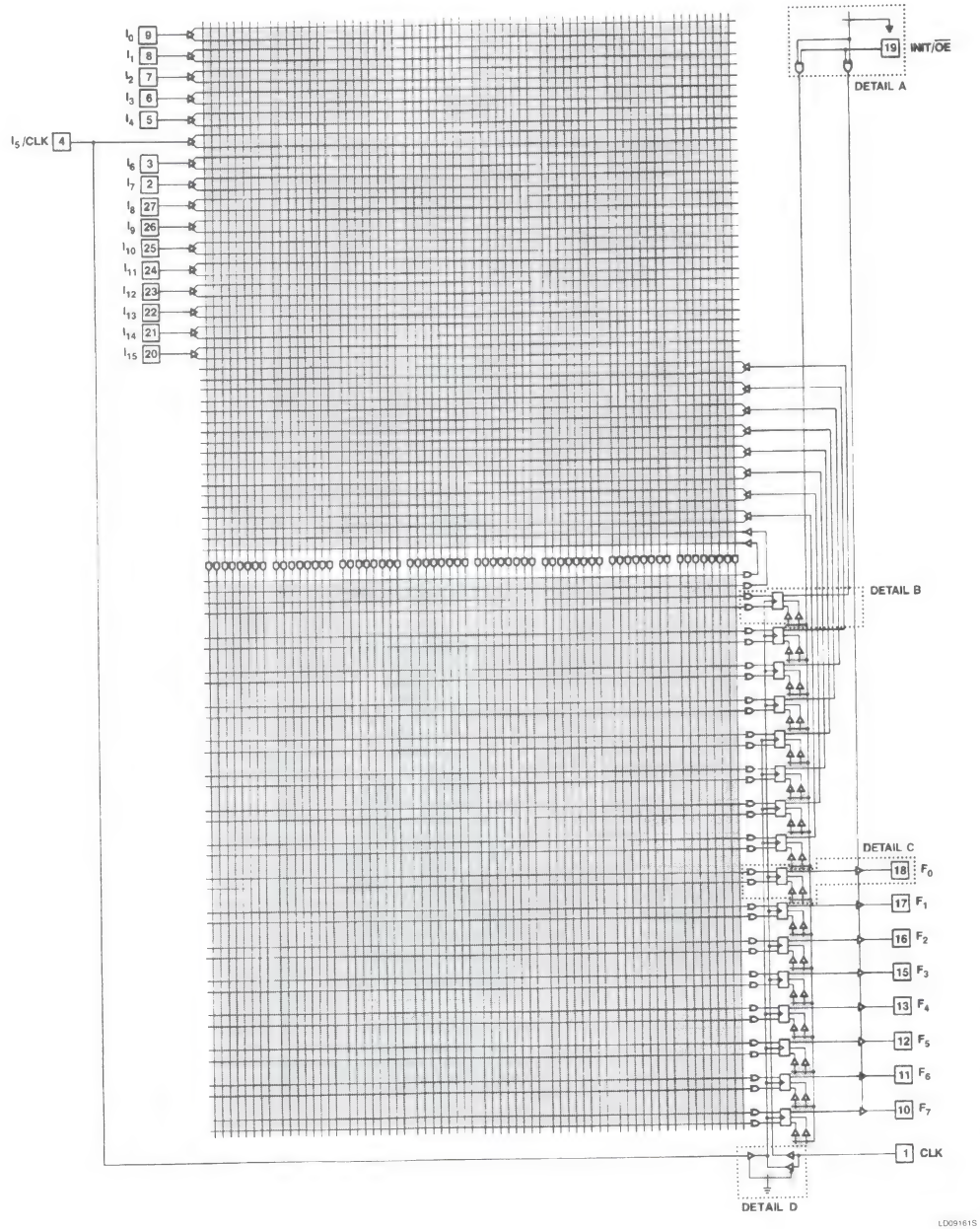
# Field-Programmable Logic Sequencer (16×64×8) PLUS405

## FUNCTIONAL DIAGRAM



# Field–Programmable Logic Sequencer (16×64×8) PLUS405

## FPLS LOGIC DIAGRAM




NOTE:
Denotes a programmable fuse location.

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | | +7 | $V_{DC}$ |
| $V_{IN}$ | Input voltage | | +5.5 | $V_{DC}$ |
| $V_{OUT}$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_{IN}$ | Input currents | -30 | +30 | mA |
| $I_{OUT}$ | Output currents | | +100 | mA |
| $T_{STG}$ | Storage temperature range | -65 | +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMIT | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$[9] | High level Input voltage | 2.0 | | | V |
| $V_{IL}$[9] | Low level Input voltage | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | -18 | mA |
| $I_{OH}$ | High level Output current | | | -2 | mA |
| $I_{OL}$ | Low level Output current | | | 9.6 | mA |
| $T_A$ | Operating free-air temperature range | -55 | | +125 | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER[3] | TEST CONDITIONS[3] | LIMITS[3] | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| $V_{IC}$ | Input Clamp voltage[4] | $V_{CC}$ = Min, $I_{IN}$ = Max | | -0.8 | -1.2 | V |
| $V_{OH}$ | High Level Output voltage | $V_{CC}$ = Min<br>$I_{OH}$ = Max | 2.4 | | | V |
| $V_{OL}$ | Low Level Output voltage | $V_{CC}$ = Min<br>$I_{OL}$ = Max | | 0.35 | 0.5 | V |
| $I_{IH}$ | High Level Input current | $V_{IN}$ = $V_{CC}$ = Max | | <1 | 25 | µA |
| $I_{IH1}$ | High Level Input current (Pin 1 only) | $V_{IN}$ = $V_{CC}$ = MAX | | | 50 | µA |
| $I_{IL}$ | Low Level Input current | $V_{IN}$ = 0.45V, $V_{CC}$ = Max | | -10 | -100 | µA |
| $I_{IL}$ | Low (CK input) Level Input current | $V_{IN}$ = 0.45V, $V_{CC}$ = Max | | -50 | -150 | µA |
| $I_{OHZ}$ | Off-State Output current High level | $V_{CC}$ = Max, $V_{OUT}$ 5.5V | | 1 | 40 | µA |
| $I_{OLZ}$ | Off-State Output current Low level | $V_{CC}$ = Max, $V_{OUT}$ 0.45V | | -1 | -40 | µA |
| $I_{OS}$ | Short circuit[4,5] | $V_{CC}$ = Max, $V_{OUT}$ = 0V | -15 | | -85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[6] | $V_{CC}$ = Max | | 190 | 225 | mA |
| $C_{IN}$ | Input Capacitance[7] | $V_{CC}$ = Nom, $V_{IN}$ = 2.0V | | 8 | 13 | pF |
| $C_{OUT}$ | Output Capacitance[7] | $V_{CC}$ = Nom, $V_{OUT}$ = 2.0V | | 10 | 15 | pF |

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

## AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TO | FROM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[2] | Max | |
| **Pulse Width** | | | | | | | |
| $t_{CKH1}$ | Clock High; CLK1 (Pin 1) | CK- | CK+ | 10 | 8 | | ns |
| $t_{CKL1}$ | Clock Low; CLK1 (Pin 1) | CK+ | CK- | 10 | 8 | | ns |
| $t_{CKP1}$ | CLK1 Period (without Complement Array) | Output± | Input± | 33 | 24 | | ns |
| $t_{CKH2}$ | Clock High: CLK2 (Pin 4) | CK- | CK+ | 10 | 8 | | ns |
| $t_{CKL2}$ | Clock Low; CLK2 (Pin 4) | CK+ | CK- | 10 | 8 | | ns |
| $t_{CKP2}$ | CLK2 Period (without Complement Array) | Output+ | Input± | 30 | 25 | | ns |
| $t_{CKP3}$ | CLK1 Period (with Complement Array) | CK+ | CK+ | 40 | 32 | | ns |
| $t_{CKP4}$ | CLK2 Period (with Complement Array)[11] | Output± | Input± | 40 | 35 | | ns |
| $t_{INITH}$ | Initialization pulse | INIT+ | INIT- | 15 | 10 | | ns |
| **Setup Time[8]** | | | | | | | |
| $t_{IS1}$ | Input | CK+ | Input± | 18 | 12 | | ns |
| $t_{IS2}$ | Input (through Complement Array) | CK+ | Input± | 25 | 20 | | ns |
| $t_{VS}$ | Power-on preset[10] | CK- | $V_{CC}$+ | 0 | -10 | | ns |
| $t_{VCK}$ | Clock resume (after initialization) | CK- | INIT- | 0 | -5 | | ns |
| $t_{NVCK}$ | Clock lockout (before initialization) | INIT- | CK- | 15 | 5 | | ns |
| **Hold Time** | | | | | | | |
| $t_{IH}$ | Input | Input± | CK+ | 0 | -5 | | ns |
| **Propagation Delay** | | | | | | | |
| $t_{CKO1}$ | Clock1 (Pin 1) | Output± | CK1+ | | 10 | 15 | ns |
| $t_{CKO2}$ | Clock2 (Pin 4) | Output± | CK2+ | | 12 | 15 | ns |
| $t_{OE}$ | Output Enable | Output- | OE- | | 12 | 15 | ns |
| $t_{OD}$ | Output Disable[8] | Output+ | OE+ | | 12 | 15 | ns |
| $t_{INIT}$ | Initialization | Output+ | INIT+ | | 15 | 20 | ns |
| $t_{PPR}$ | Power-on preset[10] | Output+ | $V_{CC}$+ | | 0 | 10 | ns |
| **Max. Frequency of Operation** | | | | | | | |
| $f_{MAX1}$ | CLK1; (without Complement Array) | | | | | 30.0 | MHz |
| $f_{MAX3}$ | CLK1; (with Complement Array) | | | | | 25.0 | MHz |

**NOTES:**

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. Measured with the INIT/$\overline{OE}$ input grounded, all other inputs $\ge 4.5V$ and the outputs open.
7. $C_{IN}$ and $C_{OUT}$ is guaranteed but not measured.
8. $C_L = 5pF$; $V_T = V_{OL} + 0.5V$.
9. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.
10. These parameters are guaranteed but not tested.
11. Not tested but guaranteed through the testing of $t_{IS2}$ and $t_{CKO2}$.

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

## TRUTH TABLE

| $V_{CC}$ | OPTION INIT | OPTION $\overline{OE}$ | $I_{10}$ | $I_{11}$ | $I_{12}$ | CK | J | K | $Q_P$ | $Q_F$ | F |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | H | | * | * | * | X | X | X | H/L | H/L | $Q_F$ |
| | L | | +10V | X | X | ↑ | X | X | $Q_P$ | L | L[9] |
| | L | | +10V | X | X | ↑ | X | X | $Q_P$ | H | H[9] |
| | L | | X | +10V | X | ↑ | X | X | L | $Q_F$ | L[9] |
| | L | | X | +10V | X | ↑ | X | X | H | $Q_F$ | H[9] |
| | L | | X | X | +10V | X | X | X | $Q_P$ | $Q_F$ | $Q_P$ |
| | L | | X | X | X | X | X | X | $Q_P$ | $Q_F$ | $Q_F$ |
| | | H | X | X | * | X | X | X | $Q_P$ | $Q_F$ | Hi-Z |
| | | X | +10V | X | X | ↑ | X | X | $Q_P$ | L | L[9] |
| +5V | | X | +10V | X | X | ↑ | X | X | $Q_P$ | H | H[9] |
| | | X | X | +10V | X | ↑ | X | X | L | $Q_F$ | L[9] |
| | | X | X | +10V | X | ↑ | X | X | H | $Q_F$ | H[9] |
| | | L | X | X | +10V | X | X | X | $Q_P$ | $Q_F$ | $Q_P$ |
| | | L | X | X | X | X | X | X | $Q_P$ | $Q_F$ | $Q_F$ |
| | | L | X | X | X | ↑ | L | L | $Q_P$ | $Q_F$ | $Q_F$ |
| | | L | X | X | X | ↑ | L | H | L | L | L |
| | | L | X | X | X | ↑ | H | L | H | H | H |
| | | L | X | X | X | ↑ | H | H | $\overline{Q_P}$ | $\overline{Q_F}$ | $\overline{Q_F}$ |
| ↑ | X | X | X | X | X | X | X | X | X | X | H |

**NOTES:**

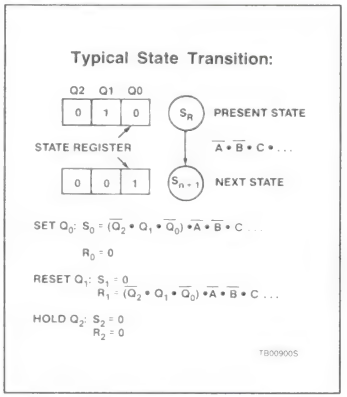
1. Positive Logic:
   S/R (or J/K) = $T_0 + T_1 + T_2 + \ldots T_{63}$
   $T_n = (C_0, C_1)\ (I_0, I_1, I_2, \ldots)\ (P_0, P_1, \ldots P_7)$
2. Either Initialization (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H/L/+10V.
5. X = Don't Care (≤ 5.5V)
6. H/L implies that either a High or a Low can occur, depending upon user-programmed selection (each State and Output Register individually programmable).
7. When using the $F_n$ pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

## VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

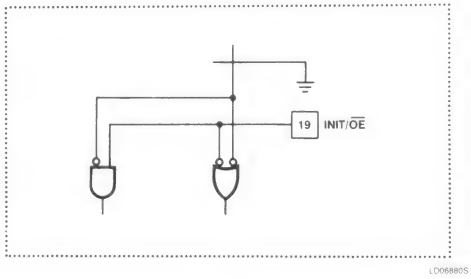
1. INIT/$\overline{OE}$ option is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All S/R (or J/K) flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.

## LOGIC FUNCTION

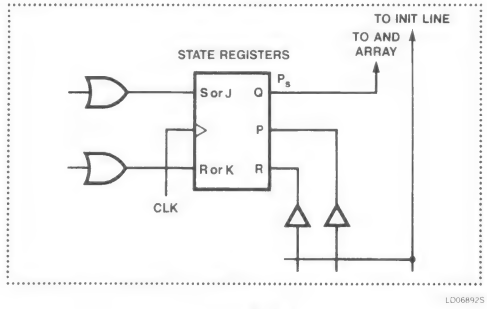

Typical State Transition:
Q2 Q1 Q0
0 1 0
STATE REGISTER
0 0 1
$S_R$
PRESENT STATE
$\overline{A} \bullet \overline{B} \bullet C \bullet \ldots$
$S_{n+1}$
NEXT STATE
SET $Q_0$: $S_0 = (\overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$
$R_0 = 0$
RESET $Q_1$: $S_1 = 0$
$R_1 = (\overline{Q_2} \bullet Q_1 \bullet \overline{Q_0}) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$
HOLD $Q_2$: $S_2 = 0$
$R_2 = 0$
TB00900S

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

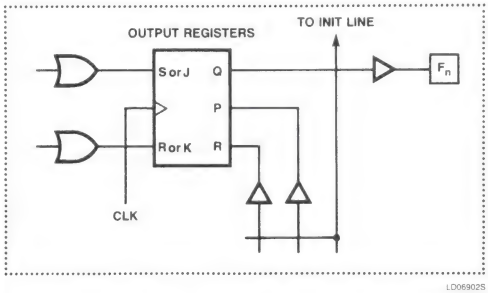
## DETAILS FOR REGISTERS FOR PLUS405



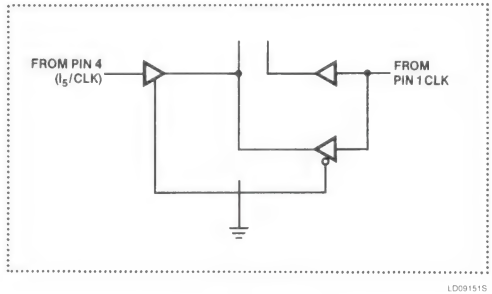

Detail A




Detail B

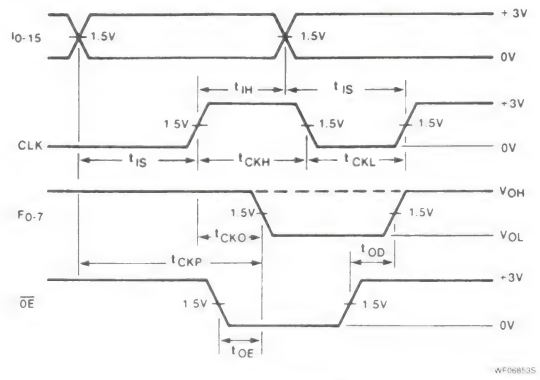



Detail C

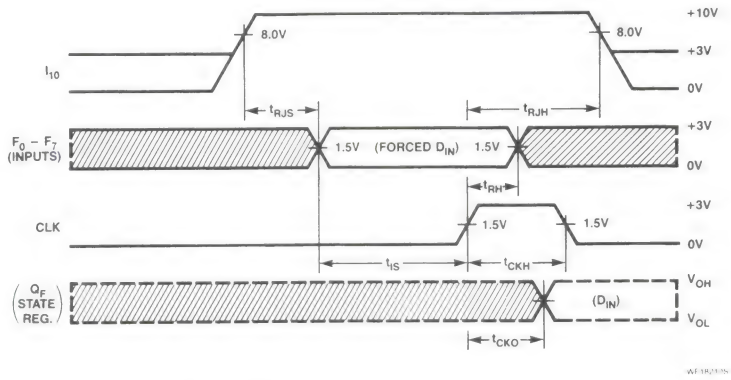



Detail D

## TIMING DIAGRAMS



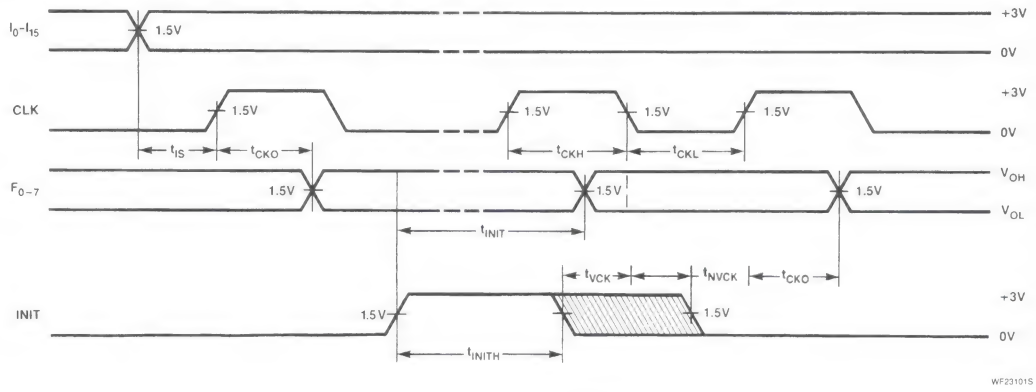

**Sequential Mode**



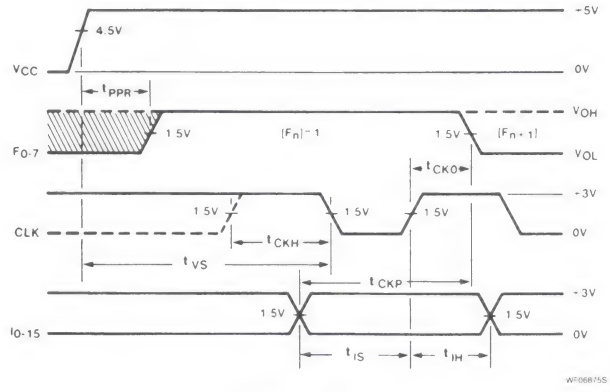

**Diagnostic Mode — Output Register Input Jam**

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

## TIMING DIAGRAMS



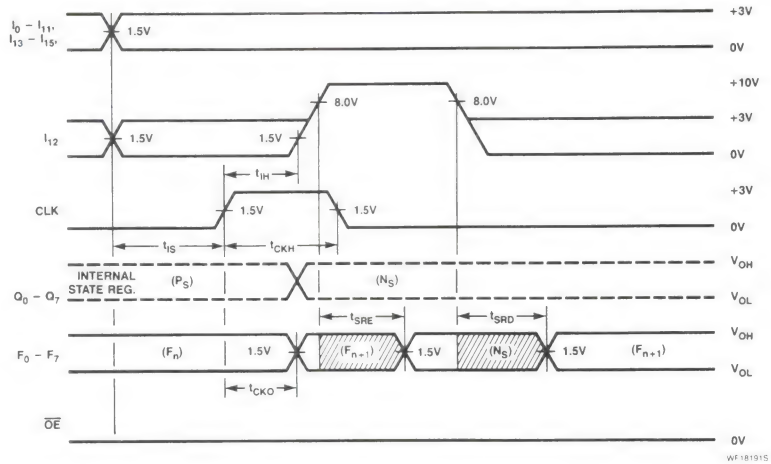

Asynchronous Initialization



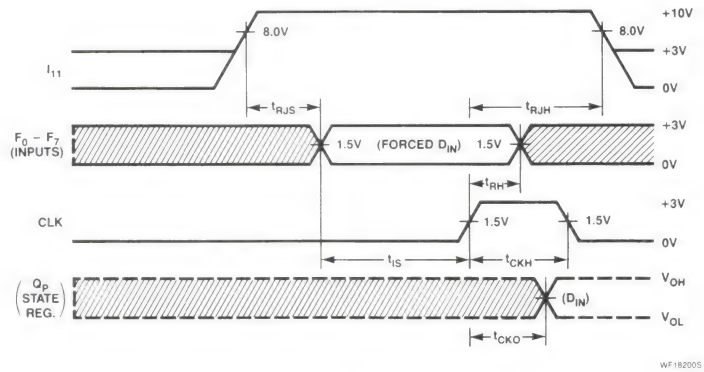

Power-On Preset

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

## TIMING DIAGRAMS




Diagnostic Mode — State Register Outputs




Diagnostic Mode — State Register Input Jam

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

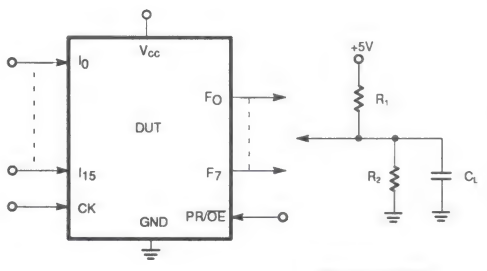
## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{CKH12,13}$ | Width of input clock pulse. |
| $t_{CKP12,13}$ | Clock period – when not using Complement Array. |
| $t_{IS1}$ | Required delay between beginning of valid input and positive transition of Clock. |
| $t_{CKO12,13}$ | Delay between positive transition of Clock and when Outputs become valid (with INIT/$\overline{OE}$ Low). |
| $t_{PPR}$ | Delay between $V_{CC}$ (after power-on) and when Outputs become preset at "1". |
| $t_{IS2}$ | Required delay between beginning of valid input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND array). |
| $t_{RJH}$ | Required delay between positive transition of Clock, and end of inputs $I_{11}$ or $I_{10}$ transition to State and Output Register Input Jam Diagnostic Modes, respectively. |
| $f_{MAX12,13,14,15}$ | Maximum operating frequency. |

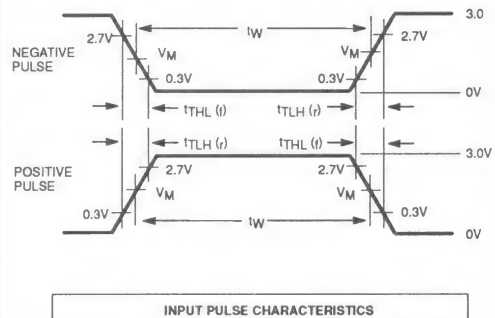
| SYMBOL | PARAMETER |
|---|---|
| $t_{CKL12,13}$ | Interval between clock pulses. |
| $t_{CKP14,15}$ | Clock period – when using Complement Array. |
| $t_{IH}$ | Required delay between positive transition of Clock and end of valid Input data. |
| $t_{OE}$ | Delay between beginning of Output Enable Low and when Outputs become valid. |
| $t_{SRE}$ | Delay between input $I_{12}$ transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register. |
| $t_{RJS}$ | Required delay between inputs $I_{11}$ or $I_{10}$ transition to State and Output Register Input Jam Diagnostic Modes, respectively, and when the output pins become available as inputs. |
| $t_{NVCK}$ | Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization to guarantee that the clock edge is not detected as a valid negative transition. |

| SYMBOL | PARAMETER |
|---|---|
| $t_{INITH}$ | Width of initialization input pulse. |
| $t_{VS}$ | Required delay between $V_{CC}$ (after power-on) and negative transition of Clock preceding first reliable clock pulse. |
| $t_{OD}$ | Delay between beginning of Output Enable High and when Outputs are in the OFF-State. |
| $t_{INIT}$ | Delay between positive transition of Initialization and when Outputs become valid. |
| $t_{SRD}$ | Delay between input $I_{12}$ transition to Logic mode and when the Outputs reflect the contents of the Output Register. |
| $t_{RH}$ | Required delay between positive transition of Clock and end of valid Input data when jaming data into State or Output Registers in diagnostic mode. |
| $t_{VCK}$ | Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding first reliable clock pulse. |

## TEST LOAD CIRCUIT




## VOLTAGE WAVEFORMS




| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| VM | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ≤5ns | ≤5ns |

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

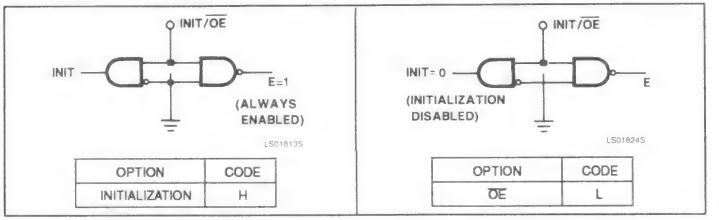
## LOGIC PROGRAMMING

PLUS405 Logic designs can be generated using Signetics AMAZE design software or several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry format is accepted.

PLUS405 logic designs can also ge generated using the program table format detailed on the following page(s). This Program Table Entry Format (PTE) is supported by the Signetics AMAZE PLD design software. AMAZE is available free of charge to qualified users.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations is assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT, ENABLE, INACTIVE, etc., symbols are defined below.

## INITIALIZATION/$\overline{OE}$ OPTION – (INIT/$\overline{OE}$)

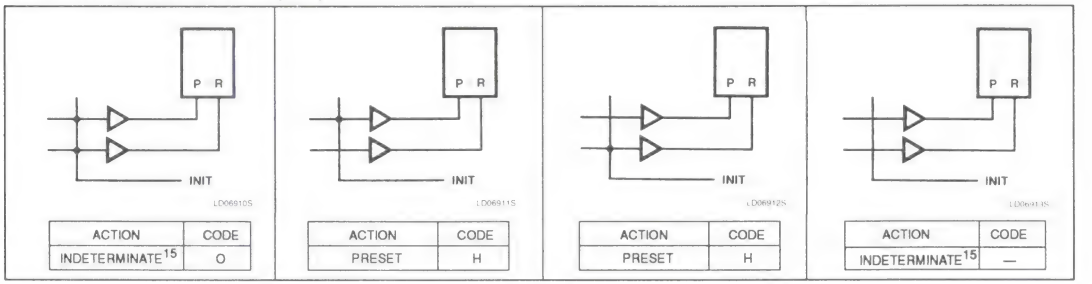



| OPTION | CODE |
|---|---|
| INITIALIZATION | H |

| OPTION | CODE |
|---|---|
| $\overline{OE}$ | L |

**PROGRAMMING THE PLUS405:**
The PLUS405 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at a logic high (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

## PRESET/RESET OPTION – (P/R)



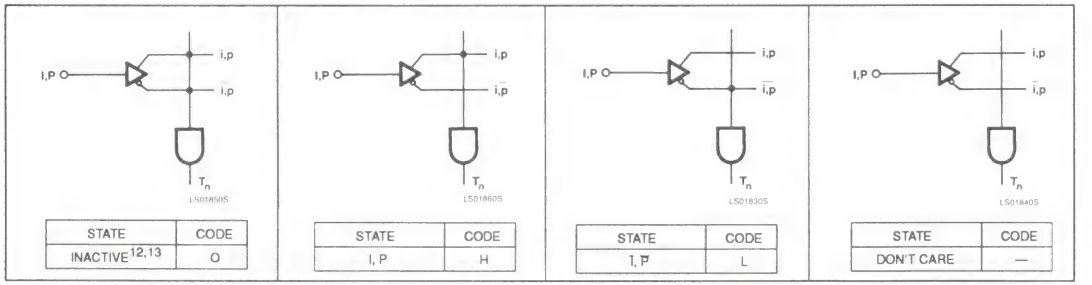

| ACTION | CODE |
|---|---|
| INDETERMINATE[15] | O |

| ACTION | CODE |
|---|---|
| PRESET | H |

| ACTION | CODE |
|---|---|
| PRESET | H |

| ACTION | CODE |
|---|---|
| INDETERMINATE[15] | — |

## "AND" ARRAY – (I), (P)




| STATE | CODE |
|---|---|
| INACTIVE[12,13] | O |

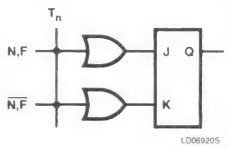
| STATE | CODE |
|---|---|
| I, P | H |

| STATE | CODE |
|---|---|
| $\overline{I}$, $\overline{P}$ | L |

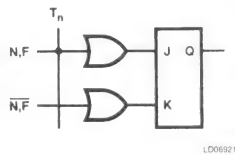
| STATE | CODE |
|---|---|
| DON'T CARE | — |

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

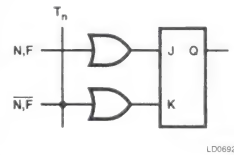
## "OR" ARRAY – J-K FUNCTION – (N), (F)



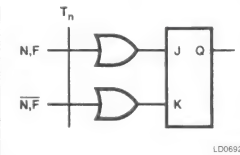

| ACTION | CODE |
|---|---|
| TOGGLE[17] | O |




| ACTION | CODE |
|---|---|
| SET | H |

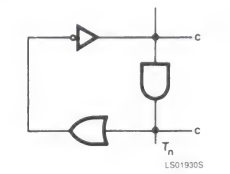



| ACTION | CODE |
|---|---|
| RESET | L |

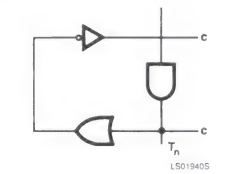



| ACTION | CODE |
|---|---|
| NO CHANGE | — |

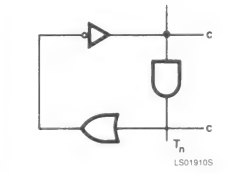
## "COMPLEMENT" ARRAY – (C)



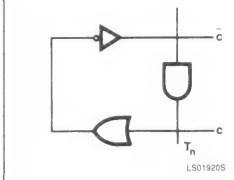

| ACTION | CODE |
|---|---|
| INACTIVE[12,14] | O |




| ACTION | CODE |
|---|---|
| GENERATE | A |

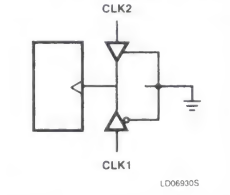



| ACTION | CODE |
|---|---|
| PROPAGATE | • |

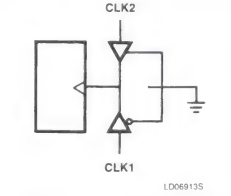



| ACTION | CODE |
|---|---|
| TRANSPARENT | — |

## "CLOCK OPTION — (CLK1/CLK2)




| ACTION | CODE |
|---|---|
| CLK1 ONLY | L |



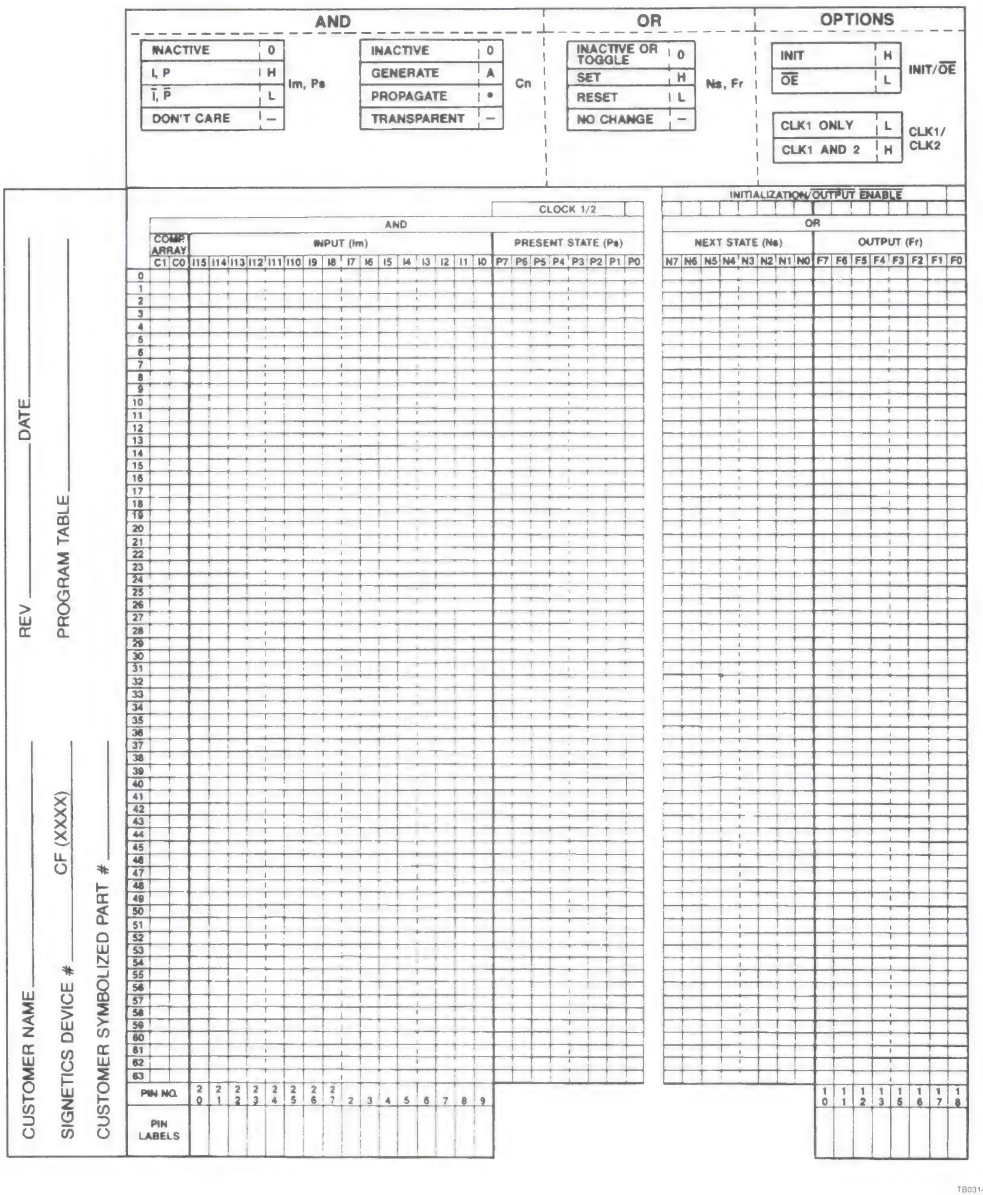

| ACTION | CODE |
|---|---|
| CLK1 and CLK2[16] | L |

**NOTES:**

12. This is the initial unprogrammed state of all links.
13. Any gate $T_n$ will be unconditionally inhibited if any one of its I or P link pairs are left intact.
14. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates $T_n$.
15. These states are not allowed when using PRESET/RESET option.
16. Input buffer $I_5$ must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
17. A single product term cannot drive more than 8 registers by itself when used in TOGGLE mode.

# Field-Programmable Logic Sequencer (16×64×8) PLUS405

## PLUS405 PROGRAM TABLE


AND
INACTIVE 0
I, P H
Ī, P̄ L
DON'T CARE –
Im, Ps
INACTIVE 0
GENERATE A
PROPAGATE •
TRANSPARENT –
Cn
OR
INACTIVE OR TOGGLE 0
SET H
RESET L
NO CHANGE –
Ns, Fr
OPTIONS
INIT H
OE L
INIT/OE
CLK1 ONLY L
CLK1 AND 2 H
CLK1/CLK2
CUSTOMER NAME
SIGNETICS DEVICE #
CF (XXXX)
CUSTOMER SYMBOLIZED PART #
REV
DATE
PROGRAM TABLE
CLOCK 1/2
INITIALIZATION/OUTPUT ENABLE
AND
OR
COMB ARRAY
C1 C0
INPUT (Im)
I15 I14 I13 I12 I11 I10 I9 I8 I7 I6 I5 I4 I3 I2 I1 I0
PRESENT STATE (Ps)
P7 P6 P5 P4 P3 P2 P1 P0
NEXT STATE (Ns)
N7 N6 N5 N4 N3 N2 N1 N0
OUTPUT (Fr)
F7 F6 F5 F4 F3 F2 F1 F0
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
PIN NO.
20 21 22 23 24 25 26 27 2 3 4 5 6 7 8 9
10 11 12 13 16 17 18
PIN LABELS
T803142S

NOTES:
1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the IN/E and H for the clock option, exits in the table, shown BLANK instead for clarity.
2. Unused Cn Im, and Ps bits are normally programmed Don't Care (—).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (—) for maximum speed.

Signetics

# 82S100/82S101

## Field Programmable Logic Array (16×48×8)

*Product Specification*

**Military**
**Customer Specific Products**

### DESCRIPTION

The 82S100 (3-State) and 82S101 (Open-Collector) are bipolar, Fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs ANDed together comprise one P-term. All 48 P-terms are selectively ORed to each output. The user must then only select which P-term will activate an output by disconnecting terms which do not affect the output. In addition, each output can be fused as active-HIGH (H) or active-LOW (L).

The 82S100 and 82S101 are fully TTL compatible, and include chip enable control for expansion of input variables and output inhibit. They feature either Open-Collector or 3-State outputs for ease of expansion of product terms and application in bus-organized systems.

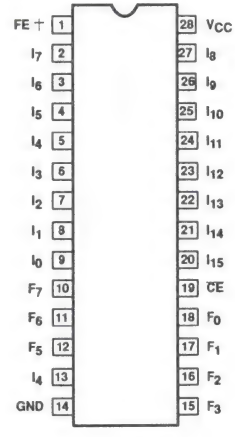
### FEATURES

- **Field-programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **I/O propagation delay: 80ns max**
- **Power dissipation: 600mW typ**
- **Input loading: -150μA max**
- **Chip enable input**
- **Output option:**
  - **82S100: 3-State**
  - **82S101: Open-Collector**
- **Output disable function;**
  - **3-State: HI-Z**
  - **Open-Collector: HI**
- **Separate I/O architecture**

### APPLICATION

- **CRT display systems**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**
- **16-bit to 8-bit bus interface**
- **Random logic replacement**

### PIN CONFIGURATION




NOTE:

† = Open or grounded during normal operation

For LLCC Pin Assignments, see Jedec Standard No. 21

### LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \bullet \overline{B} \bullet C \bullet D$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L

$\overline{Z} = \overline{P0} + \overline{P1} + \overline{P2} + \ldots$

$Z = \overline{P0} \bullet \overline{P1} \bullet \overline{P2} \bullet \ldots$

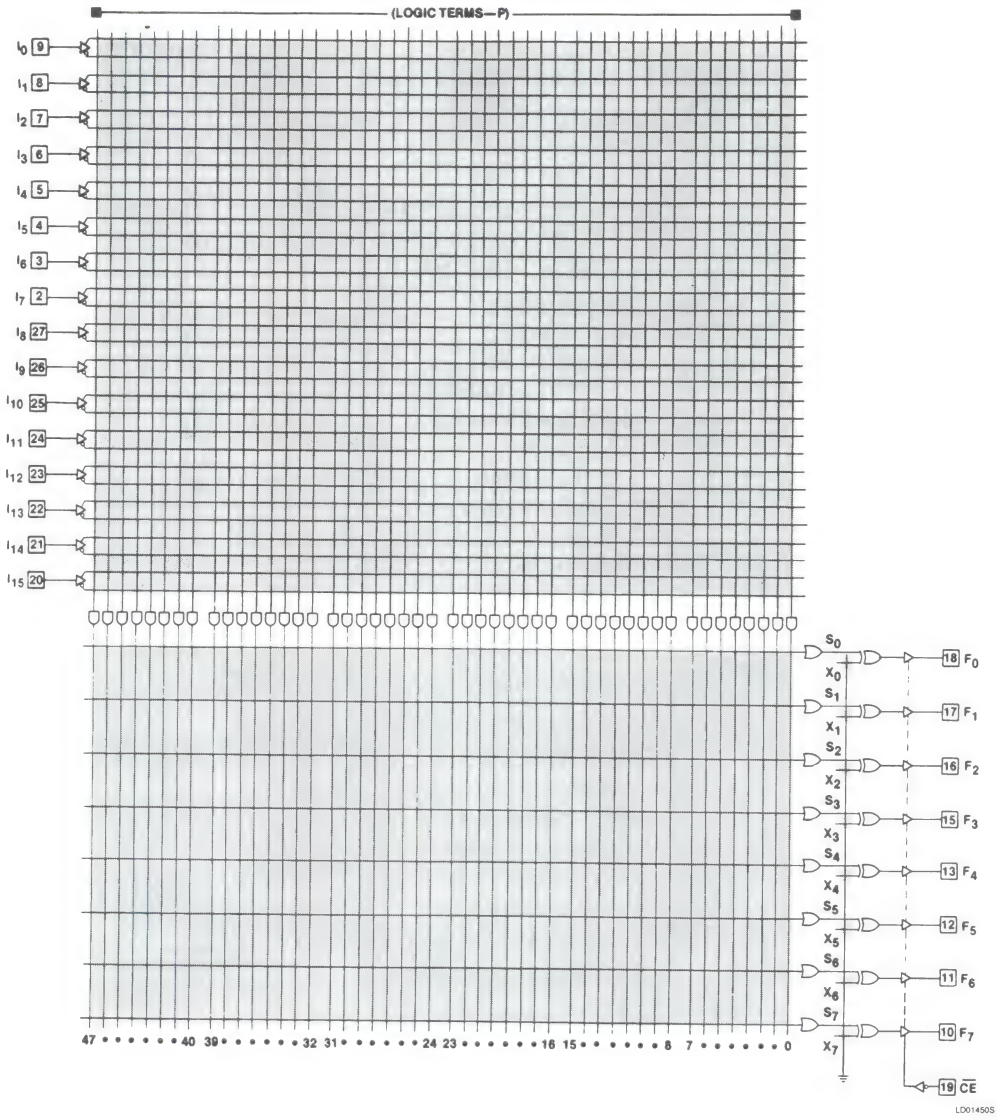
NOTES:

1. For each of the 8 outputs, either function Z (active-High) or $\overline{Z}$ (active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C etc. are user defined connections to fixed inputs (I) and output pins (O).

### ORDERING INFORMATION

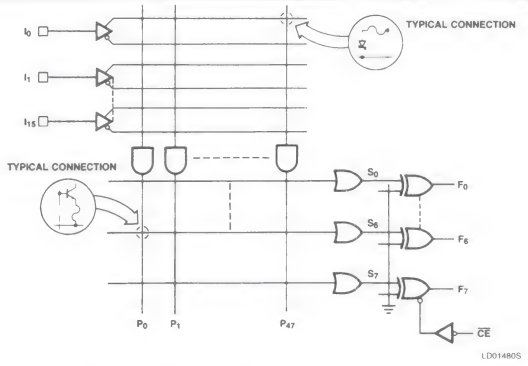
| PACKAGE | 3-STATE | OPEN–COLLECTOR |
|---|---|---|
| 28-pin Ceramic DIP 600mil-wide | 82S100/BXA | 82S101/BXA |
| 28-pin Ceramic Flat Pack | 82S100/BYA | 82S101/BYA |
| 28-pin Ceramic LLCC | 82S100/B3A | 82S101/B3A |

## FPLA LOGIC DIAGRAM




**NOTES:**
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. Programmable connection.

## FUNCTIONAL DIAGRAM




Fusible Ni-Cr links are initially intact at all array cross-points.

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Power supply voltage | +7 | $V_{DC}$ |
| $V_I$ | Input voltage | +10.0 | $V_{DC}$ |
| $V_O$ | Output voltage | +5.5 | $V_{DC}$ |
| $I_I$ | Input currents | -30 to +30 | mA |
| $I_O$ | Output currents | +100 | mA |
| $T_A$ | Operating Temperature range | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature range | -65 to +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS[3] | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[5] | Max | |
| **Input Voltage** | | | | | | |
| $V_{IH}$ | High | $V_{CC}$ = 5.5V | 2.0 | | | V |
| $V_{IL}$ | Low | $V_{CC}$ = 4.5V | | | 0.8 | V |
| $V_{IK}$ | Clamp[4] | $V_{CC}$ = 4.5V, $I_I$ = -18mA | | -0.8 | -1.2 | V |
| **Output Voltage** | | | | | | |
| | | $V_{CC}$ = 4.5V | | | | V |
| $V_{OH}$ | High (82S100)[5, 10] | $I_{OH}$ = -2mA | 2.4 | | | V |
| $V_{OL}$ | Low[6] | $I_{OL}$ = 9.6mA | | 0.35 | 0.5 | V |
| **Input Current** | | | | | | |
| | | $V_{CC}$ = 5.5V | | | | |
| $I_{IH}$ | High | $V_I$ = 5.5V | | <1 | 50 | µA |
| $I_{IL}$ | Low | $V_I$ = 0.45V | | -10 | -150 | µA |
| **Output Current** | | | | | | |
| | | $\overline{CE}$ = HIGH, $V_{CC}$ = Max | | | | |
| $I_{O(OFF)}$ | Hi-Z State | $V_O$ = 5.5V | | 1 | 60 | µA |
| | (82S100) | $V_O$ = 0.45V | | -1 | -60 | µA |
| $I_{OS}$ | Short circuit (82S100)[4, 7, 10] | $\overline{CE}$ = LOW, $V_O$ = 0V | -15 | | -85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[8] | $V_{CC}$ = 5.5V | | 120 | 180 | mA |
| **Capacitance[9]** | | | | | | |
| | | $\overline{CE}$ = HIGH | | | | |
| | | $V_{CC}$ = 5.0V | | | | |
| $C_{IN}$ | Input | $V_I$ = 2.0V | | 8 | 13 | pF |
| $C_{OUT}$ | Output | $V_O$ = 2.0V | | 17 | 22 | pF |

## AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TO | FROM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[5] | Max | |
| **Propagation Delay** | | | | | | | |
| $T_{PD}$ | Input[11] | Output | Input | | 35 | 80 | ns |
| $T_{CE}$ | Chip enable | Output | Chip enable | | 15 | 40 | |
| **Disable Time** | | | | | | | |
| $T_{CD}$ | Chip disable | Output | Chip enable | | 15 | 40 | ns |

**NOTES:**

1. Stresses above those listed under Absolute Maximum Ratings may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one pin at a time.
5. Measured with $V_{IL}$ applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to $V_{CC}$.
7. Duration of short circuit should not exceed 1 second.
8. $I_{CC}$ is measured with the chip enable input at a logic high, $1_1$-$1_{15}$ = GND.
9. Guaranteed, but not tested.
10. On unprogrammed device apply 10V - $1_1$-$I_{15}$.
11. Not testable on unprogrammed device.

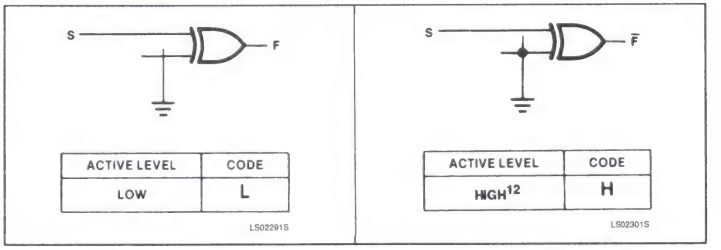
## LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table.

In this Table, the logic state or action of variables I, P and F, associated with each Sum Term $S_n$, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

### OUTPUT POLARITY – (F)



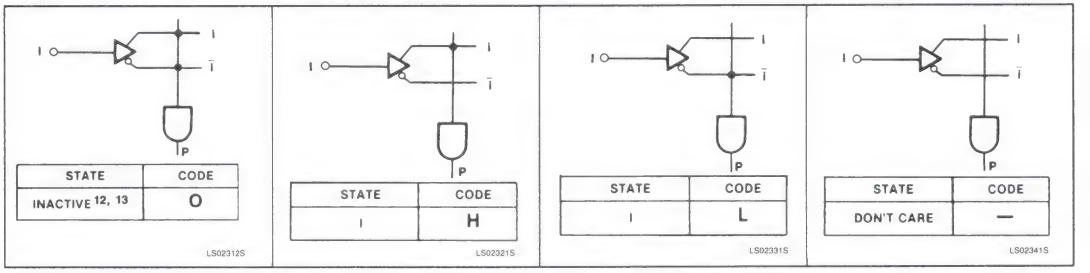

| ACTIVE LEVEL | CODE |
|---|---|
| LOW | L |

LS02291S

| ACTIVE LEVEL | CODE |
|---|---|
| HIGH[12] | H |

LS02301S

### "AND" ARRAY – (I)




| STATE | CODE |
|---|---|
| INACTIVE[12, 13] | O |

LS02312S

| STATE | CODE |
|---|---|
| I | H |

LS02321S

| STATE | CODE |
|---|---|
| I | L |

LS02331S

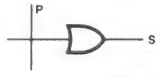
| STATE | CODE |
|---|---|
| DON'T CARE | — |

LS02341S

### "OR" ARRAY – (F)

LS02010S

| $P_n$ STATUS | CODE |
|---|---|
| ACTIVE[12] | A |




LS02020S

| $P_n$ STATUS | CODE |
|---|---|
| INACTIVE | • |

**NOTES:**

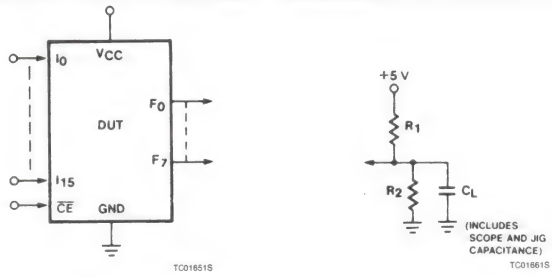
12. This is the initial unprogrammed state of all links.
13. Any gate $P_n$ will be unconditionally inhibited if any one of its (I) link pairs is left intact.

# Field Programmable Logic Array (16×48×8) — 82S100/101

## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{CE}$ | Delay between beginning of Chip Enable Low (with input valid) and when Data Output becomes valid. |
| $T_{CD}$ | Delay between when Chip Enable becomes High and Data Output is in Off-state (Hi-Z or High). |
| $T_{PD}$ | Delay between beginning of valid input (with Chip Enable Low) and when Data Output becomes valid. |

## TEST LOAD CIRCUITS



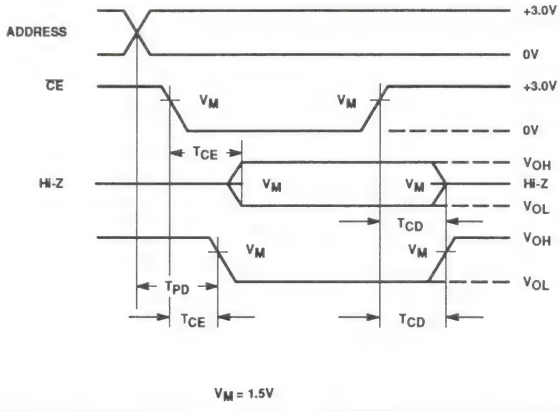

NOTE:
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 50pF$.

## VIRGIN STATE

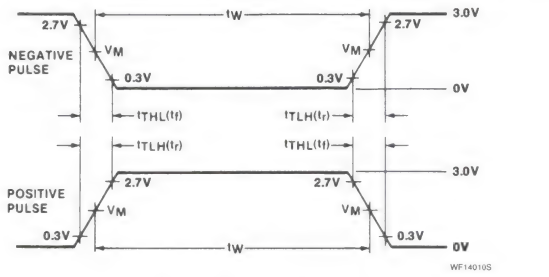
The 82S100/101 virgin devices are factory shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both True and Complement values of every input variable I (P-terms always logically "false").
3. The "OR" Matrix contains all 48 P-terms.
4. The polarity of each output is set to active-High (Fp function).
5. All outputs are at a Low logic level.

## TIMING DIAGRAM




## VOLTAGE WAVEFORM




**Input Pulse Definitions**

| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| $V_M$ | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ⩽5ns | ⩽5ns |

Signetics

# 82S105 (PLS105)

## Field-Programmable Logic Sequencer (16×48×8)

**Signetics Programmable Logic**
***Product Specification***

**Military**
**Application Specific Products**

### DESCRIPTION

The 82S105 is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 $Q_P$, and 8 $Q_F$ edge-triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 16 external inputs, $I_{0\text{-}15}$, with six internal inputs, $P_{0\text{-}5}$, fed back from the State Register to form up to 48 transition terms (AND terms).

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse. Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to $\overline{\text{Output Enable}}$ function, as an additional user-programmable option.

Order codes are listed in the Ordering Information table.

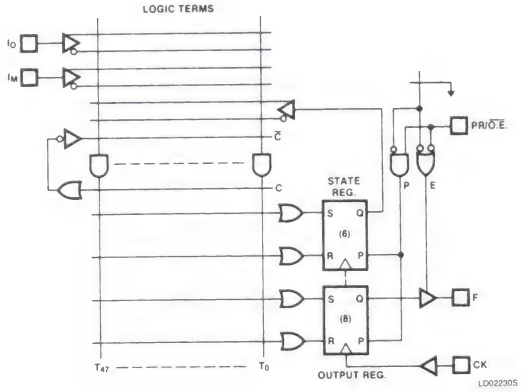
### FEATURES

- **Field-programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **48 transition terms**
- **6-bit State Register**
- **8-bit Output Register**
- **Transition Complement Array**
- **Positive edge-trigger clock**
- **Programmable asynchronous preset or Output Enable**
- **Power-on preset to all "1" of internal registers**
- **$f_{MAX}$ = 10.5MHz**
- **650mW power dissipation (typical)**
- **TTL compatible**
- **Single +5V supply**
- **3-state outputs**

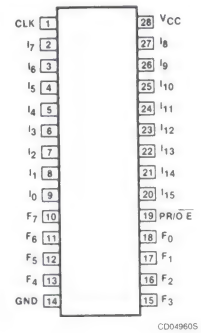
### APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

### FUNCTIONAL DIAGRAM



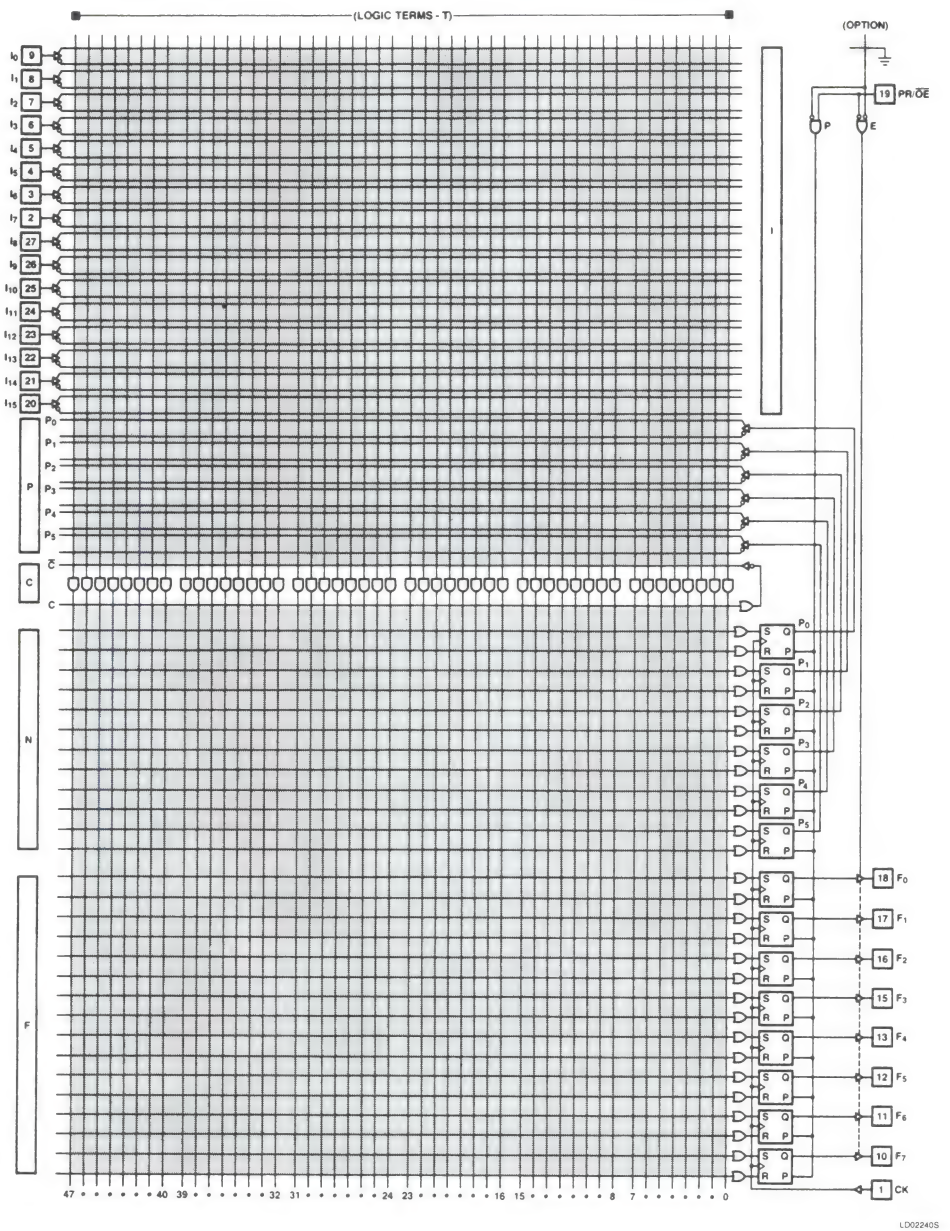

### PIN CONFIGURATION




For LLCC pin assignments see JEDEC Standard 21

# Field–Programmable Logic Sequencer (16×48×8) 82S105

## FPLS LOGIC DIAGRAM




**NOTES:**
1. All AND inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown link float to logic "0".
3. ▒ Programmable connection.

# Field-Programmable Logic Sequencer (16×48×8) — 82S105

## ORDERING INFORMATION

| PACKAGE | ORDER CODE |
|---|---|
| 28–Pin Ceramic DIP 600mil–wide | 82S105/BXA |
| 28–Pin Ceramic Leadless Chip Carrier | 82S105/B3A |
| 28–Pin Ceramic Flat Pack | 82S105/BYA |

## PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION | POLARITY |
|---|---|---|---|
| 1 | CK | **Clock:** The Clock input to the State and Output Registers. A Low–to–High transition on this line is necessary to update the contents of both registers. | Active–High |
| 2 – 8<br>20 – 27 | $I_{1-15}$ | **Logic Inputs:** The 15 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. | Active–High/Low |
| 9 | $I_0$ | **Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercised with standard TTL levels. When $I_0$ is held at +10V, device outputs $F_{0-5}$ reflect the contents of State Register bits $P_{0-5}$. The contents of each Output Register remains unaltered. | Active–High/Low |
| 10 – 13<br>15 – 18 | $F_{0-7}$ | **Logic/Diagnostic Outputs:** Eight device outputs which normally reflect the contents of Output Register bits $Q_{0-7}$, when enabled. When $I_0$ is held at +10V, $F_{0-5} = (P_{0-5})$, and $F_{6,7}$ = Logic "1". | Active–High |
| 19 | PR/$\overline{OE}$ | **Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function:<br>• **Preset:** Provides an asynchronous preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and $F_{0-7}$ are High. Normal clocking resumes with the first full clock pulse following a High–to–Low clock transition, after Preset goes Low.<br>• **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers $F_{0-7}$ from the Output Register. | Active–High (H)<br>Active–Low (L) |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply voltage | | +7 | $V_{DC}$ |
| $V_I$ | Input voltage | | +10.0 | $V_{DC}$ |
| $V_O$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_{IK}$ | Input currents | –30 | +30 | mA |
| $I_O$ | Output currents | | +100 | mA |
| $T_A$ | Operating temperature range | –55 | +125 | °C |
| $T_{STG}$ | Storage temperature range | –65 | +150 | °C |

# Field-Programmable Logic Sequencer (16×48×8) 82S105

## DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER[3] | TEST CONDITIONS[3] | LIMITS[3] | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| **Input Voltage** | | | | | | |
| $V_{IH}$ | High | $V_{CC}$ = 5.5V | 2 | | | V |
| $V_{IL}$ | Low | $V_{CC}$ = 4.5V | | | 0.8 | V |
| $V_{IK}$ | Clamp[4] | $V_{CC}$ = Min, $I_{IK}$ = −18mA | | −0.8 | −1.2 | V |
| **Output Voltage** | | | | | | |
| | | $V_{CC}$ = 4.5V | | | | |
| $V_{OH}$ | High[5] | $I_{OH}$ = −2mA | 2.4 | | | V |
| $V_{OL}$ | Low[6] | $I_{OL}$ = 9.6mA | | 0.35 | 0.5 | V |
| **Input Current** | | | | | | |
| | | $V_{CC}$ = 5.5V | | | | |
| $I_{IH}$ | High | $V_I$ = 5.5V | | <1 | 50 | µA |
| $I_{IL}$ | Low | $V_I$ = 0.45V | | −10 | −150 | µA |
| $I_{IL}$ | Low (CK input) | $V_I$ = 0.45V | | −50 | −350 | µA |
| **Output Current** | | | | | | |
| | | $V_{CC}$ = 5.5V | | | | |
| $I_{O(OFF)}$ | Hi–Z state[7] | $V_O$ = 5.5V | | 1 | 60 | µA |
| | | $V_O$ = 0.45V | | −1 | −60 | µA |
| $I_{OS}$ | Short circuit[4,8] | $V_O$ = 0V | −15 | | −85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[9] | $V_{CC}$ = 5.5V | | 120 | 185 | mA |
| **Capacitance[7, 10]** | | | | | | |
| | | $V_{CC}$ = 5.0V | | | | |
| $C_{IN}$ | Input | $V_I$ = 2.0V | | 8 | 13 | pF |
| $C_{OUT}$ | Output | $V_O$ = 2.0V | | 10 | 15 | pF |

# Field-Programmable Logic Sequencer (16×48×8) 82S105

## AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

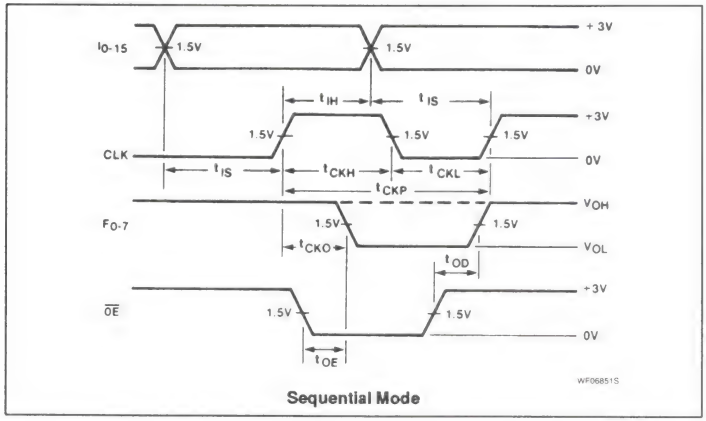
| SYMBOL | PARAMETER | TO | FROM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[11] | Max | |
| **Pulse Width** | | | | | | | |
| $t_{CKH}$ | Clock[12] High | CK– | CK+ | 40 | 15 | | ns |
| $t_{CKL}$ | Clock Low | CK+ | CK– | 40 | 15 | | ns |
| $t_{CKP1}$ | Period (w/o C–array) | CK+ | CK+ | 95 | 40 | | ns |
| $t_{CKP2}$ | Period (w/C–array)[10] | CK+ | CK+ | 135 | 60 | | ns |
| $t_{PRH}$ | Preset pulse | PR+ | PR– | 40 | 15 | | ns |
| **Setup Time** | | | | | | | |
| $t_{IS1}$ | Input | CK+ | Input± | 60 | | | ns |
| $t_{IS2}$ | Input (through Complement array)[13] | CK+ | Input± | 100 | | | ns |
| $t_{VS}$ | Power–on preset[13] | CK– | $V_{CC}$+ | 5 | –10 | | ns |
| $t_{PRS}$ | Preset[10] | CK– | PR– | 5 | –10 | | ns |
| **Hold Time** | | | | | | | |
| $t_{IH}$ | Input[10] | Input± | CK+ | 10 | –10 | | ns |
| **Propagation Delay** | | | | | | | |
| $t_{CKO}$ | Clock | Output± | CK+ | | 15 | 35 | ns |
| $t_{OE}$ | Output Enable[13] | Output– | OE– | | 20 | 40 | ns |
| $t_{OD}$ | Output Disable[13] | Output+ | OE+ | | 20 | 40 | ns |
| $t_{PR}$ | Preset | Output+ | PR+ | | 18 | 45 | ns |
| $t_{PPR}$ | Power–on preset[10] | Output+ | $V_{CC}$+ | | 0 | 20 | ns |
| **Frequency of Operation** | | | | | | | |
| $f_{MAX}$ | w/o C–array | | | | | 10.5 | MHz |
| $f_{MAX}^C$ | w/C–array[10] | | | | | 8.3 | MHz |

**NOTES:**

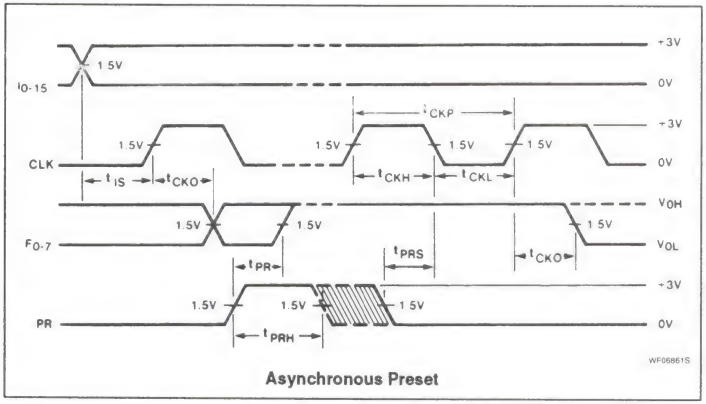
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with $V_{IL}$ applied to $\overline{OE}$ and a logic High stored, or with $V_{IH}$ applied to PR.
6. Measured with a programmed logic condition for which the output is at a Low logic level, and $V_{IL}$ applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to $V_{CC}$.
7. Measured with $V_{IH}$ applied to PR/$\overline{OE}$.
8. Duration of short circuit should not exceed 1 second.
9. $I_{CC}$ is measured with the PR/$\overline{OE}$ input grounded, the outputs open.
10. Guaranteed, but not tested.
11. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
12. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 30ns.
13. Not testable on unprogrammed devices.

# Field-Programmable Logic Sequencer (16×48×8) 82S105

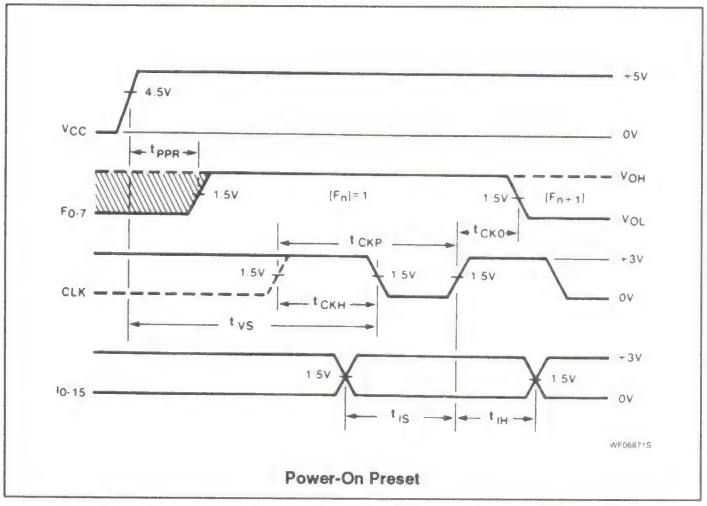
## TIMING DIAGRAMS




**Sequential Mode**




**Asynchronous Preset**



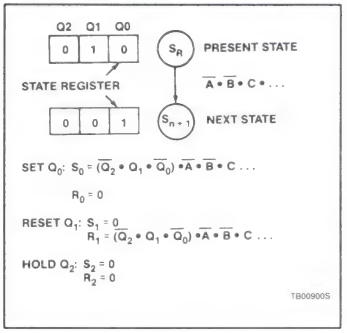

**Power-On Preset**

## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{CKH}$ | Width of input clock pulse. |
| $t_{CKL}$ | Interval between clock pulses. |
| $t_{CKP1}$ | Clock period – when not using Complement Array. |
| $t_{IS1}$ | Required delay between beginning of valid input and positive transition of Clock. |
| $t_{CKP2}$ | Clock period – when using Complement Array. |
| $t_{IS2}$ | Required delay between beginning of valid input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND array). |
| $t_{VS}$ | Required delay between $V_{CC}$ (after power–on) and negative transition of Clock preceding first reliable clock pulse. |
| $t_{PRS}$ | Required delay between negative transition of Asynchronous Preset and negative transition of Clock preceding first reliable clock pulse. |
| $t_{IH}$ | Required delay between positive transition of Clock and end of valid input data. |
| $t_{CKO}$ | Delay between positive transition of clock and when outputs become valid (with PR/$\overline{OE}$ Low). |
| $t_{OE}$ | Delay between beginning of Output Enable Low and when Outputs become valid. |
| $t_{OD}$ | Delay between beginning of Output Enable High and when Outputs are in the Off–State. |
| $t_{PR}$ | Delay between positive transition of Preset and when Outputs become valid at "1". |
| $t_{PPR}$ | Delay between $V_{CC}$ (after power–on) and when Outputs become preset at "1". |
| $t_{PRH}$ | Width of preset input pulse. |
| $f_{MAX}$ | Maximum clock frequency. |

# Field-Programmable Logic Sequencer (16×48×8) — 82S105

## LOGIC FUNCTION


Q2 Q1 Q0
0 1 0
STATE REGISTER
0 0 1
$S_R$
PRESENT STATE
$\overline{A} \bullet \overline{B} \bullet C \bullet \ldots$
$S_{n+1}$
NEXT STATE
SET $Q_0$: $S_0 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$
$R_0 = 0$
RESET $Q_1$: $S_1 = 0$
$R_1 = (\overline{Q}_2 \bullet Q_1 \bullet \overline{Q}_0) \bullet \overline{A} \bullet \overline{B} \bullet C \ldots$
HOLD $Q_2$: $S_2 = 0$
$R_2 = 0$
TB00900S

## VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

5. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power–up procedure.
6. All transition terms are disabled (0).
7. All S/R flip–flop inputs are disabled (0).
8. The device can be clocked via a Test Array pre–programmed with a standard test pattern.

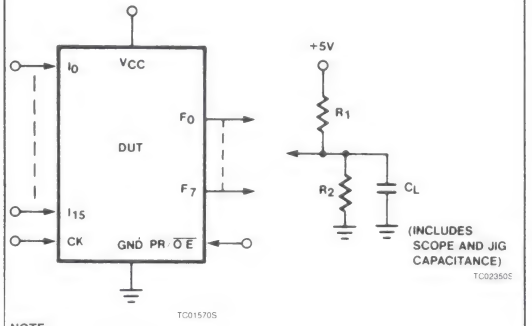
NOTE: The Test Array pattern must be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

## TRUTH TABLE

| $V_{CC}$ | OPTION PR | OPTION $\overline{OE}$ | $I_0$ | CK | S | R | $Q_{P/F}$ | F |
|---|---|---|---|---|---|---|---|---|
| | H | | * | X | X | X | H | H |
| | L | | +10V | X | X | X | $Q_n$ | $(Q_P)_n$ |
| | L | | X | X | X | X | $Q_n$ | $(Q_F)_n$ |
| | | H | * | X | X | X | $Q_n$ | Hi–Z |
| +5V | | L | +10V | X | X | X | $Q_n$ | $(Q_P)_n$ |
| | | L | X | X | X | X | $Q_n$ | $(Q_F)_n$ |
| | | L | X | ↑ | L | L | $Q_n$ | $(Q_F)_n$ |
| | | L | X | ↑ | L | H | L | L |
| | | L | X | ↑ | H | L | H | H |
| | | L | X | ↑ | H | H | IND. | IND. |
| ↑ | X | X | X | X | X | X | H | |

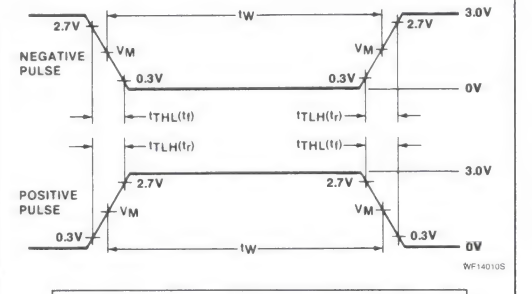
NOTES:
1. Positive Logic $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$; $T_n = C(I_0\, I_1\, I_2 \ldots)(P_0\, P_1 \ldots P_8)$
2. Either Preset (Active–High) or Output Enable (active–Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V.
6. X = Don't Care (≤ 5.5V).

## TEST LOAD CIRCUIT




NOTE:
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 50pF$.

## VOLTAGE WAVEFORMS




| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| VM | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ≤5ns | ≤5ns |

# Field-Programmable Logic Sequencer (16×48×8) — 82S105

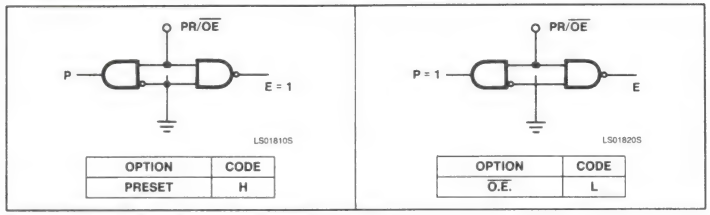
## LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Table on the following page.

In this table, the logic state or action of control variables C, I, P, N and F, associated with each Transition Term $T_n$, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

## PRESET/$\overline{OE}$ OPTION – (P/E)

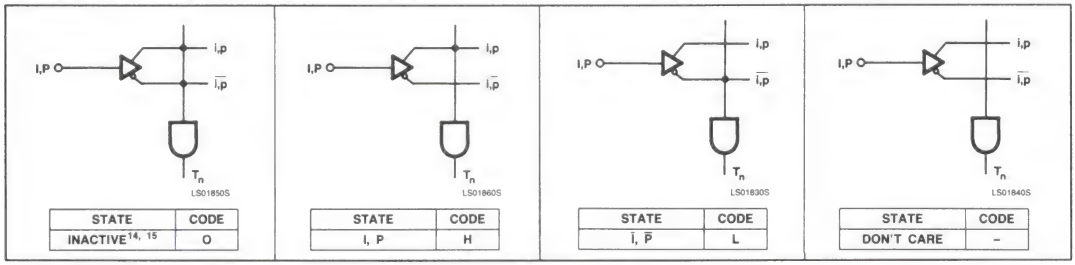



| OPTION | CODE |
|---|---|
| PRESET | H |

| OPTION | CODE |
|---|---|
| $\overline{O.E.}$ | L |

**PROGRAMMING THE 82S105**:
The 82S105 has a power–up preset feature. This feature insures that the device will power–up in a known state with all register elements (state and output register) at a logic High (H). When programming the device, it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

## "AND" ARRAY – (I), (P)



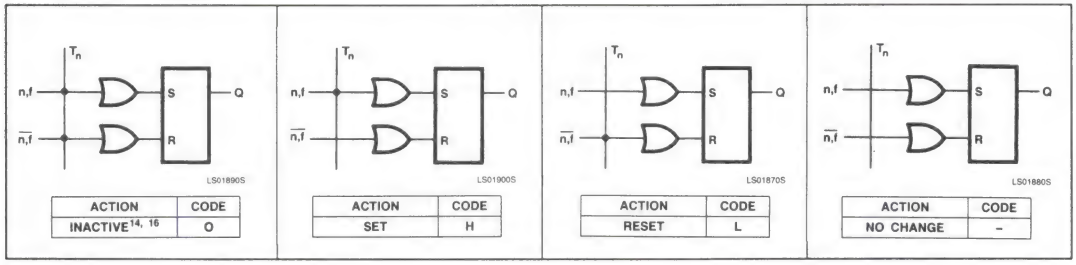

| STATE | CODE |
|---|---|
| INACTIVE[14, 15] | O |

| STATE | CODE |
|---|---|
| I, P | H |

| STATE | CODE |
|---|---|
| $\overline{I}$, $\overline{P}$ | L |

| STATE | CODE |
|---|---|
| DON'T CARE | – |

## "OR" ARRAY – (N), (F)



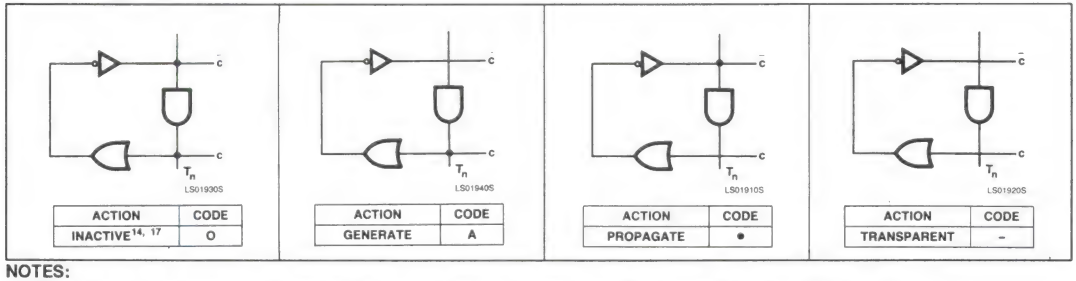

| ACTION | CODE |
|---|---|
| INACTIVE[14, 16] | O |

| ACTION | CODE |
|---|---|
| SET | H |

| ACTION | CODE |
|---|---|
| RESET | L |

| ACTION | CODE |
|---|---|
| NO CHANGE | – |

## "COMPLEMENT" ARRAY – (C)




| ACTION | CODE |
|---|---|
| INACTIVE[14, 17] | O |

| ACTION | CODE |
|---|---|
| GENERATE | A |

| ACTION | CODE |
|---|---|
| PROPAGATE | • |

| ACTION | CODE |
|---|---|
| TRANSPARENT | – |

**NOTES:**
14. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates $T_n$.
15. Any gate $T_n$ will be unconditionally inhibited if any one of its I or P link pairs are left intact.
16. To prevent simultaneous Set and Reset flip–flop commands, this state is not allowed for N and F link pairs coupled to active gates $T_n$ (see flip–flop truth tables).
17. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates $T_n$.

# Field-Programmable Logic Sequencer (16×48×8) 82S105

## FPLS PROGRAM TABLE

CUSTOMER NAME _____
PURCHASE ORDER # _____
SIGNETICS DEVICE # CF (XXXX)
CUSTOMER SYMBOLIZED PART # _____
TOTAL NUMBER OF PARTS _____
PROGRAM TABLE _____
REV _____
DATE _____

| AND | | | OR | | |
|---|---|---|---|---|---|
| INACTIVE | 0 | Cn | INACTIVE | 0 | Ns, Fr |
| GENERATE | A | | SET | H | |
| PROPAGATE | B | | RESET | L | |
| TRANSPARENT | — | | NO CHANGE | — | |
| INACTIVE | 0 | Im, Ps | OPTION | | |
| I, P | H | | PRESET | H | P/E |
| $\overline{I}$, $\overline{P}$ | L | | $\overline{OE}$ | L | |
| DON'T CARE | — | | | | |

| | AND | | | | | | | | | | | | | | | | | | OPTION (P/E) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | OR | | | | | | | | | |
| TERM | Cn | INPUT (Im) | | | | | | | | | | | | | | | | | PRESENT STATE (Ps) | | | | | | REMARKS | NEXT STATE (Ns) | | | | | | OUTPUT (Fr) | | | | | | | |
| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | 5 | 4 | 3 | 2 | 1 | 0 | | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 30 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 33 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 34 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 35 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 37 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 38 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 39 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 40 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 41 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 42 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 43 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 44 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 46 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 46 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 47 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PIN NO. | | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | | | | | | | | | | | | | | 10 | 11 | 12 | 13 | 15 | 16 | 17 | 18 |
| VARIABLE NAME | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

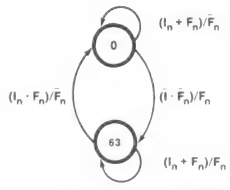
LD02251S

## TEST ARRAY

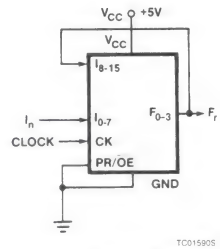
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to $I_{0-7}$ as shown in the test circuit timing diagram.




State Diagram




FPLS Under Test

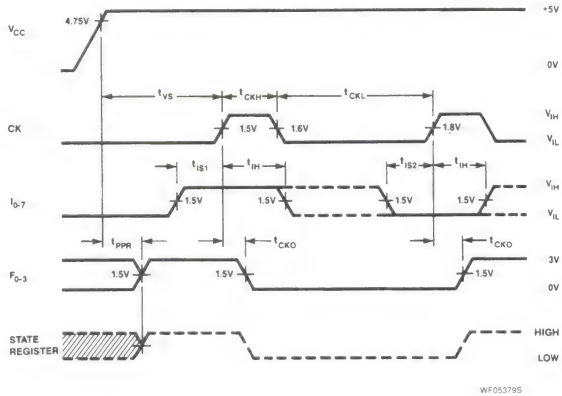
**TEST ARRAY PROGRAM**

| TERM | C | AND: INPUT (Im) 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PRESENT STATE (Ps) 5 | 4 | 3 | 2 | 1 | 0 | OPTION (P · E) H — OR — NEXT STATE (Ns) 5 | 4 | 3 | 2 | 1 | 0 | OUTPUT (Fr) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 | A | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | L | L | L | L | L | L | L | L | L | L | L | L | L |
| 49 | ● | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

TB01760S

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetic's qualified programming equipment.




Test Circuit Timing Diagram

**TEST ARRAY DELETED**

| TERM | C | AND: INPUT (Im) 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | PRESENT STATE (Ps) 5 | 4 | 3 | 2 | 1 | 0 | OPTION (P · E) H — OR — NEXT STATE (Ns) 5 | 4 | 3 | 2 | 1 | 0 | OUTPUT (Fr) 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 | — | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 49 | ● | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | L | — | — | — | — | — | — | — | — | — | — | — | — | — | — |

TB01750S

Test Array Deleted

Signetics

# 82S153A (PLS153A)

## Field Programmable Logic Array (18×42×10)

**Military**
**Customer Specific Products**

**Signetics Programmable Logic**
***Product Specification***

### DESCRIPTION

The 82S153A is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 directional control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I,B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The 82S153A is field programmable, enabling the use to quickly generate custom patterns using standard programming equipment.

Order codes are listed in the Ordering Information Table.

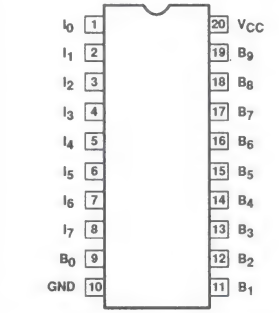
### FEATURES

- **Field-Programmable (Ni-Cr links)**
- **8 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active-High or -Low outputs**
- **42 Product Terms:**
  - **— 32 Logic Terms**
  - **— 10 Control Terms**
- **I/O propagation delay: 42ns (max)**
- **Input loading: -150μA (max)**
- **Power dissipation: 650mW (typ.)**
- **3-State outputs**
- **TTL compatible**

### APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

### PIN CONFIGURATION




For LLCC pin assignments, see Package Section.

### LOGIC FUNCTION

**TYPICAL PRODUCT TERM:**

$Pn = A * B * C * D * \ldots$

**TYPICAL LOGIC FUNCTION:**

**AT OUTPUT POLARITY = H**

$Z = P0 + P1 + P2 \ldots$

**AT OUTPUT POLARITY = L**

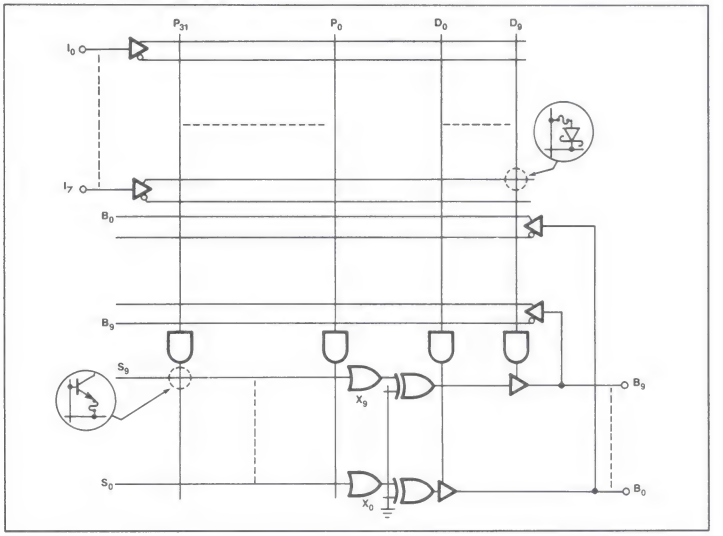
$\overline{Z} = \overline{P0 + P1 + P2 + \ldots}$

$Z = \overline{P0} * \overline{P1} * \overline{P2} \ldots$

**NOTES:**

1. For each of the 10 outputs, either function Z (active-high) or $\overline{Z}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

### FUNCTIONAL DIAGRAM

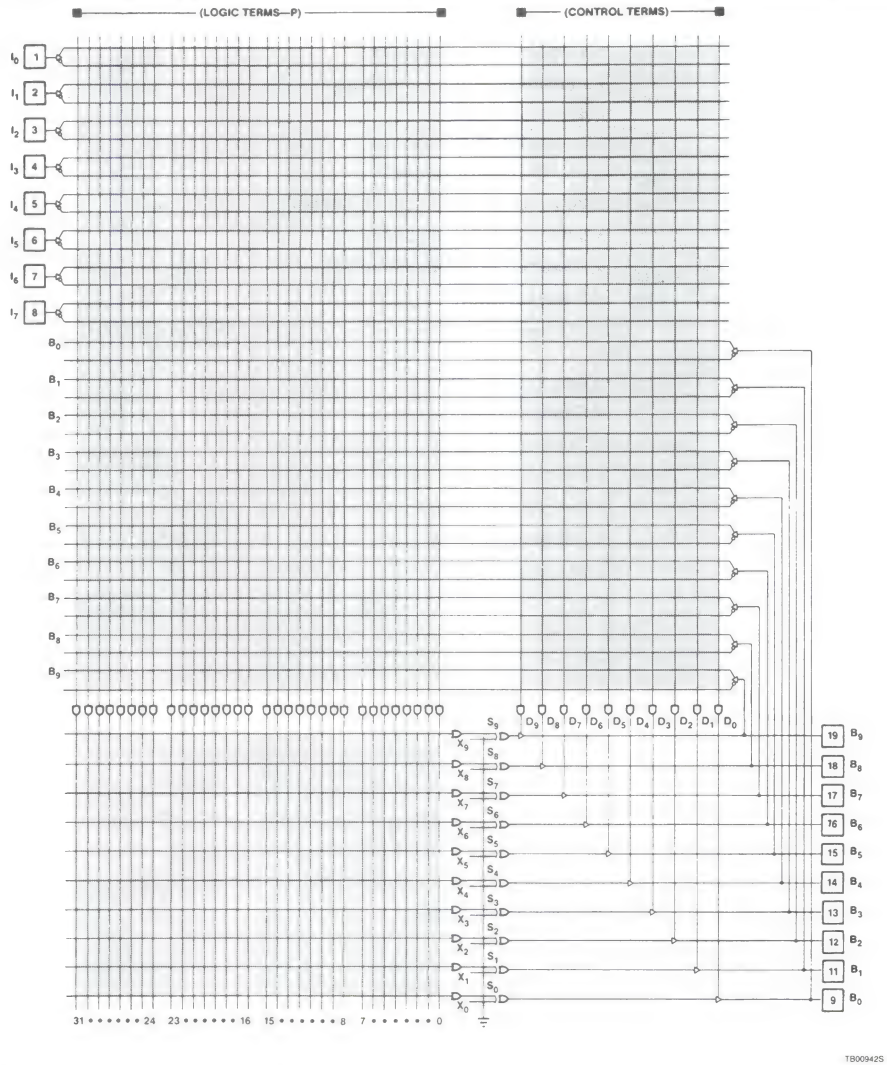


# Field Programmable Logic Array (18×42×10) — 82S153A

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 20–Pin Ceramic DIP 300mil–wide | 82S153A/BRA |
| 20–Pin Ceramic Flat Pack | 82S153A/BSA |
| 20–Pin Ceramic LLCC | 82S153A/B2A |

## FPLA LOGIC DIAGRAM




**NOTES:**
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ⊗ Programmable connection.

# Field Programmable Logic Array (18×42×10) — 82S153A

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | | UNIT |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{CC}$ | Supply Voltage | | +7 | $V_{DC}$ |
| $V_I$ | Input voltage | | +10.0 | $V_{DC}$ |
| $V_O$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_I$ | Input currents | –30 | +30 | mA |
| $I_O$ | Output currents | | +100 | mA |
| $T_A$ | Operating Temperature Range | –55 | +125 | °C |
| $T_{STG}$ | Storage Temperature Range | –65 | +150 | °C |

## DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS[3] | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[2] | Max | |
| **Input Voltage** | | | | | | |
| $V_{IL}$ | Low | $V_{CC} = 4.5V$ | | | 0.80 | V |
| $V_{IH}$ | High | $V_{CC} = 5.5V$ | 2.0 | | | V |
| $V_{IK}$ | Clamp[4] | $V_{CC} = 4.5V$, $I_I = -18mA$ | | –0.8 | –1.2 | V |
| **Output Voltage** | | | | | | |
| | | $V_{CC} = 4.5V$ | | | | |
| $V_{OL}$ | Low[5] | $I_{OL} = 12mA$ | | | 0.5 | V |
| $V_{OH}$ | High[6] | $I_{OH} = 2mA$ | 2.4 | | | V |
| **Input current** | | | | | | |
| | | $V_{CC} = 5.5V$ | | | | |
| $I_{IL}$ | Low | $V_I = 0.45V$ | | | –150 | µA |
| $I_{IH}$ | High | $V_I = 5.5V$ | | | 50 | µA |
| **Output current** | | | | | | |
| | | $V_{CC} = 5.5V$ | | | | |
| $I_{O(OFF)}$ | Hi–Z state[10] | $V_O = 5.5V$ | | | 110 | µA |
| | | $V_O = 0.45V$ | | | –210 | µA |
| $I_{OS}$ | Short circuit[4, 6, 7] | $V_O = 0V$ | –15 | | –85 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[8] | $V_{CC} = 5.5V$ | | 130 | 165 | mA |
| **Capacitance[12]** | | | | | | |
| | | $V_{CC} = 5V$ | | | | |
| $C_{IN}$ | Input | $V_I = 2.0V$ | | 8 | 13 | pF |
| $C_B$ | I/O | $V_B = 2.0V$ | | 15 | 20 | pF |

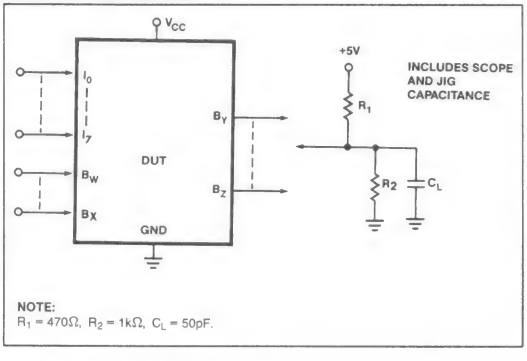
# Field Programmable Logic Array (18×42×10) — 82S153A

## AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

| SYMBOL | PARAMETER | TO | FROM | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ[2] | Max | |
| $t_{PD}$ | Propagation delay | Output ± | Input ± | $C_L$ = 30pF | | 20 | 45 | ns |
| $t_{OE}$ | Output enable | Output ± | Input ± | | | 20 | 40 | ns |
| $t_{OD}$ | Output disable[9, 11] | Output ± | Input ± | $C_L$ = 5pF | | 20 | 40 | ns |

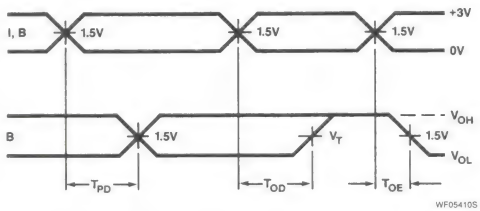
**NOTES:**
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with +10V applied to $I_7$.
6. Measured with +10V applied to $I_{0-7}$. Output sink current is supplied through a resistor to $V_{CC}$.
7. Duration of short circuit should not exceed 1 second.
8. $I_{CC}$ is measured with $I_{0,1}$ grounded, $I_{2-7}$ and $B_{0-9}$ at 4.5V.
9. Measured at $V_T = V_{OL}$ +0.5V.
10. Leakage values are a combination of input and output leakage.
11. Not testable on unprogrammed device.
12. Guaranteed, but not tested.

## TEST LOAD CIRCUIT

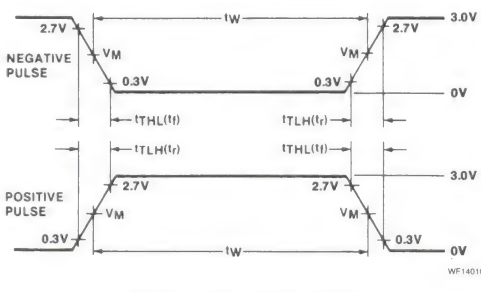



NOTE:
$R_1$ = 470Ω, $R_2$ = 1kΩ, $C_L$ = 50pF.

## TIMING DIAGRAMS




## VOLTAGE WAVEFORMS




## TIMING DEFINITIONS

| | |
|---|---|
| $T_{PD}$ | Propagation delay between input and output. |
| $T_{DD}$ | Delay between input change and when output is off (hi–Z or High). |
| $T_{DE}$ | Delay between input change and when output reflects specified output level. |

## INPUT PULSE DEFINITIONS

| INPUT PULSE CHARACTERISTICS | | | | |
|---|---|---|---|---|
| $V_M$ | Rep. Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 1.5V | 1MHz | 500ns | ≤ 5ns | ≤ 5ns |

# Field Programmable Logic Array (18×42×10) 82S153A

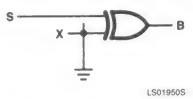
## LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR/EX–OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this Table the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

### OUTPUT POLARITY – (B)



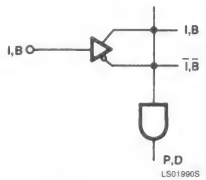

LS01950S

| ACTIVE LEVEL | CODE |
|---|---|
| HIGH | H |

LS01960S

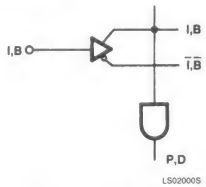
| ACTIVE LEVEL | CODE |
|---|---|
| LOW | L |

### "AND" ARRAY – (I, B)



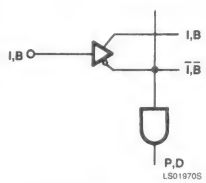

LS01990S

| STATE | CODE |
|---|---|
| INACTIVE[13, 14] | O |



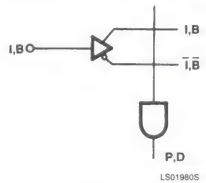

LS02000S

| STATE | CODE |
|---|---|
| I, B | H |




LS01970S

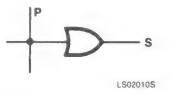
| STATE | CODE |
|---|---|
| $\bar{I}$, $\bar{B}$ | L |




LS01980S

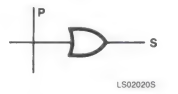
| STATE | CODE |
|---|---|
| DON'T CARE | – |

### OR ARRAY – (B)




LS02010S

| $P_n$ STATUS | CODE |
|---|---|
| ACTIVE | A |




LS02020S

| $P_n$ STATUS | CODE |
|---|---|
| INACTIVE | • |

**NOTES:**
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates $P_n$, $D_n$.
2. Any gates $P_n$, $D_n$ will be unconditionally inhibited if any one of its (I, B) link pairs is left intact.

## VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs at "H" polarity.
2. All $P_n$ terms are disabled.
3. All $p_n$ terms are active on all outputs.

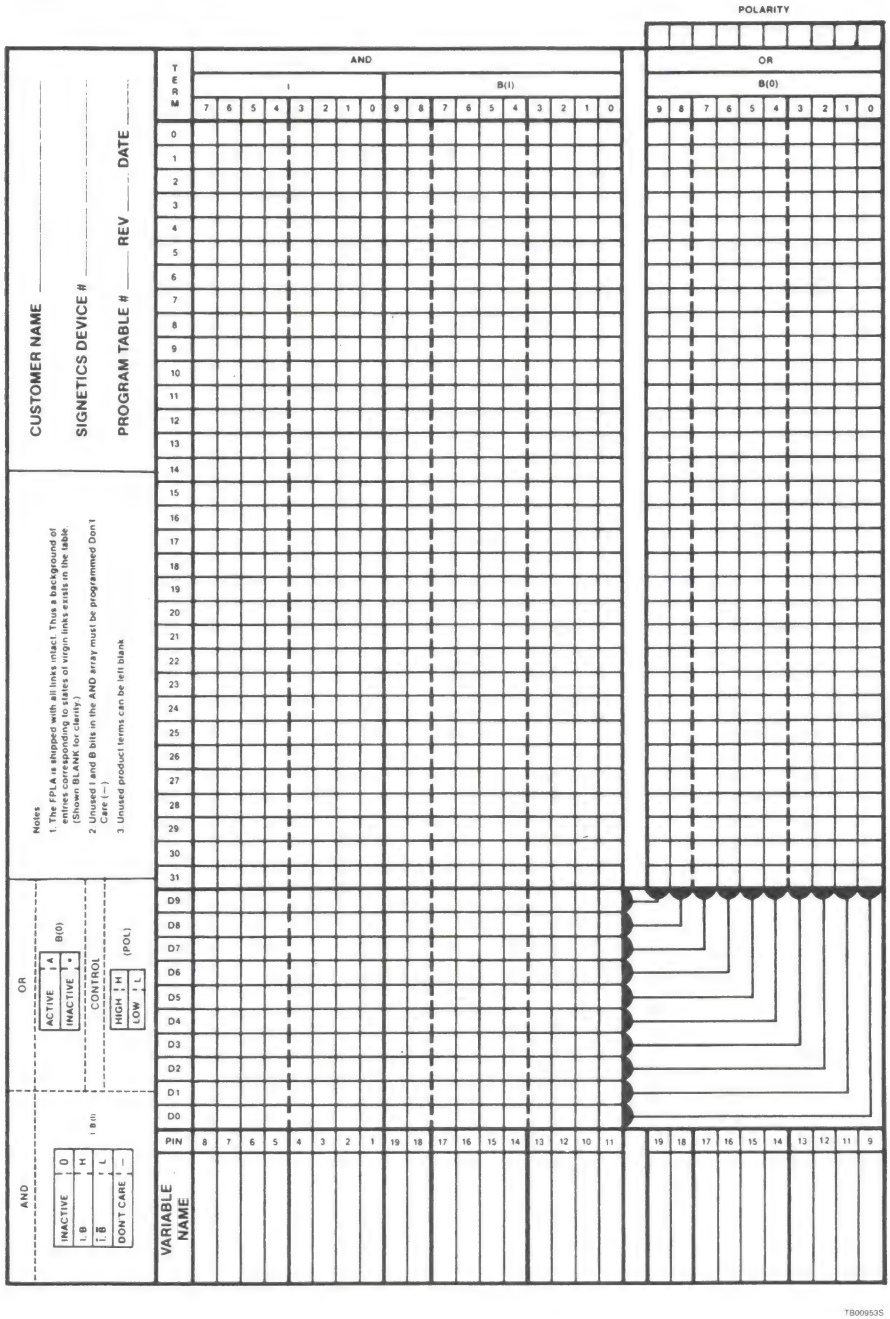
## CAUTION: 82S153A TEST COLUMNS

The 82S153A incorporates two columns not shown in the logic block diagram. These columns are used for in–house testing of the device in the unprogrammed state. These columns must be disabled prior to using the 82S153A in your application. If you are using a Signetics approved programmer the disabling is accomplished during the device programming sequence. If these columns are not disabled, abnormal operation is possible.

# Field Programmable Logic Array (18×42×10)

# 82S153A

## FPLA PROGRAM TABLE

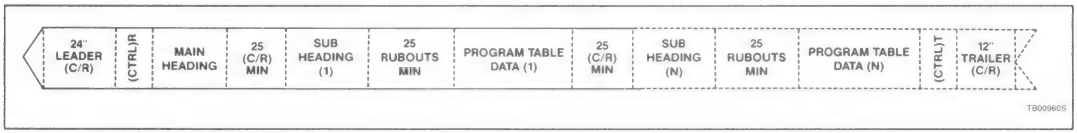

POLARITY
AND
OR
I
B(I)
B(O)
TERM
7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0
9 8 7 6 5 4 3 2 1 0
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
CUSTOMER NAME _____
SIGNETICS DEVICE # _____
PROGRAM TABLE # _____ REV _____ DATE _____
Notes
1. The FPLA is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table (Shown BLANK for clarity.)
2. Unused I and B bits in the AND array must be programmed Don't Care (—)
3. Unused product terms can be left blank
OR
ACTIVE H A
INACTIVE L *
B(O)
CONTROL
HIGH H
LOW L
(POL)
AND
INACTIVE 0
I, B H
I, B L
DON'T CARE —
I, B(I)
D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
PIN 8 7 6 5 4 3 2 1 19 18 17 16 15 14 13 12 10 11 19 18 17 16 15 14 13 12 11 9
VARIABLE NAME

TB00953S

## TWX TAPE CODING (LOGIC FORMAT)

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8–level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339–9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however, limit tape length to a roll of 1.75 inch inside diameter and 4.25 outside diameter.



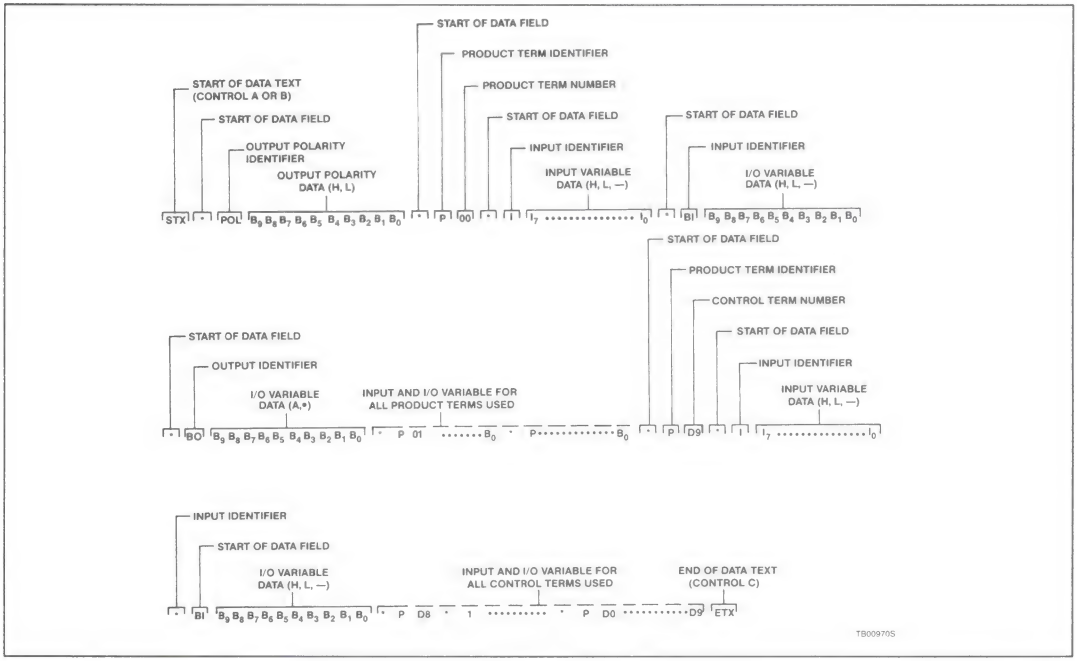

A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name
2. Customer TWX No.
3. Date
4. Purchase Order No.
5. Number of Program Tables
6. Total Number of Parts

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No.
2. Program Table No.
3. Revision
4. Date
5. Customer Symbolized Part No.
6. Number of Parts

c. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of output polarity, product term, and output information separated by appropriate identifiers in accordance with the following format. Entries for the data fields correspond to those defined in the Logic PROGRAM TABLE:



Signetics

Military Products

# Section 7
# Package Outlines

Please refer to the Packaging Information of the Introduction on page 9.

Signetics

Military Products

# Section 8
# Alphanumeric Index

# Signetics

# Alphanumeric Index

## Military Products


| | | |
|---|---|---|
| **LM119** | Dual Voltage Comparator | 17 |
| **LM124** | Low Power Quad Op Amp | 22 |
| **LM139A/LM139** | Qual Voltage Comparator | 26 |
| **PLHS18P8A** | Programmable AND Array Logic (18×72×8) | 641 |
| **PLHS473** | Field-Programmable Logic Array (20×24×11) | 646 |
| **PLHS501** | Programmable Macro Logic Random Logic Unit (32×72×24) | 652 |
| **PLS159A** | Field-Programmable Logic Sequencer (16×45×12) | 658 |
| **PLS167** | Field-Programmable Logic Sequencer (14×48×6) | 668 |
| **PLS168** | Field-Programmable Logic Sequencer (12×48×8) | 679 |
| **PLS173** | Field-Programmable Logic Array (22×42×10) | 689 |
| **PLS179** | Field-Programmable Logic Sequencer (20×45×12) | 697 |
| **PLUS16L8/PLUS16R8** | PAL®-Type Devices | 708 |
| **PLUS20L8/PLUS20R8** | PAL®-Type Devices | 718 |
| **PLUS405** | Field-Programmable Logic Sequencer (16×64×8) | 728 |
| **521** | High-Speed Dual Differential Comparator/Sense Amp | 32 |
| **522** | High-Speed Dual Diffential Comparator/Sense Amp | 36 |
| **527** | Voltage Comparator | 38 |
| **529** | Voltage Comparator | 43 |
| **555** | Timer | 48 |
| **556-1** | Dual Timer | 54 |
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| **2691** | Universal Asynchronous Receiver/Transmitter (UART) | 187 |
| **2692** | Dual Asynchronous Receiver/Transmitter (DUART) | 205 |
| **2698-B** | Enhanced Octal Universal Asynchronous Receiver/Transmitter | 228 |
| **26LS31** | Quad High Speed Differential Line Driver | 30 |
| **27C64A** | 64K CMOS UV Erasable PROM (8K×8) | 613 |
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| **27C512** | 512K CMOS UV Erasable PROM (64K×8) | 630 |
| **27HC641** | 64K-Bit CMOS PROM (8K×8) | 634 |
| **5018** | 8-Bit µP-Compatible D/A Converter | 99 |
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| **5212** | Transimpedance Amplifier | 111 |
| **5512** | Dual High-Performance Operational Amplifier | 116 |
| **5521** | LVDT Signal Conditioner | 118 |
| **5532/5532A** | Internally Compensated Dual Low Noise Op Amp | 122 |
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| **5537** | Sample-and-Hold Amplifier | 133 |
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| **5560** | Switched-Mode Power Supply Control Circuit | 146 |
| **68000** | 16-/32-Bit Microprocessor | 363 |
| **68154** | Interrupt Generator | 427 |
| **68155** | Interrupt Handler | 437 |
| **68172** | VMEbus Controller (BUSCON) | 453 |

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| **68562** | Dual Universal Serial Communications Controller (DUSCC) | 249 |
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| **68681** | Dual Asynchronous Receiver/Transmitter (DUART) | 319 |
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| **8X60** | FIFO RAM Controller (FRC) | 562 |
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| **8X371** | 8-Bit Latched Bidirectional I/O Port | 595 |
| **8X372/8X376** | Addressable/Bidirectional I/O Ports | 601 |
| **80C31BH/80C51BH** | CMOS Single-Chip 8-Bit Microcontroller | 479 |
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| **82S100/82S101** | Field-Programmable Logic Array (16×48×8) | 743 |
| **82S105(PLS105)** | Field-Programmable Logic Sequencer (16×48×8) | 749 |
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| **83C552/80C552** | Single-Chip 8-Bit Microcontroller | 510 |
| **83C751** | CMOS Single-Chip 8-Bit Microcontroller | 511 |
| **87C51** | CMOS Single-Chip 8-Bit EPROM Microcontroller | 522 |
| **87C451** | CMOS Single-Chip 8-Bit EPROM Microcontroller | 524 |
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| **87C751** | CMOS Single-Chip 8-Bit Microcontroller | 545 |
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| **µA733** | Differential Video Amplifier | 160 |

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Military Products

# Section 9
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Military Products

# Appendix A
# Product Listing of Contents of Volume 2

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# Product Listing of Contents of Volume 2

**Military Products**

The following is a list of products whose data sheets are available in the Military Products Handbook, Volume 2.

## SECTION 1: ERASABLE PROM PRODUCTS

| Part Number | Device Description | Part Number | Device Description | Part Number | Device Description |
|---|---|---|---|---|---|
| 27C512/BXA–20 | 32KX8 | 27C64/BUA–20 | 8KX8 | 27C256/BXA–20 OT | 32KX8 |
| 27C512/BXA–25 | 32KX8 | 27C64/BUA–25 | 8KX8 | 27C256/BXA–25 OT | 32K8X |
| 27C256/BXA–20 | 32KX8 | 27C64/BXA–20 | 8KX8 | 27C256/BXA–30 OT | 32KX8 |
| 27C256/BXA–25 | 32KX8 | 27C64/BXA–25 | 8KX8 | 27C64/BXA–20 OT | 8KX8 |
| 27C256/BXA–30 | 32KX8 | 27C64/BXA–35 | 8KX8 | 27C64/BXA–25 OT | 8KX8 |
| 27C256/BUA–20 | 32KX8 | 27HC641–55/BJA | 8KX8 | 27C64/BXA–35 OT | 8KX8 |
| 27C256/BUA–25 | 32KX8 | 27HC641–70/BJA | 8KX8 | | |

## SECTION 2: FAST LOGIC PRODUCTS

| Part Number | Device Description | Part Number | Device Description | Part Number | Device Description |
|---|---|---|---|---|---|
| 54F00/BCA | GATE | 54F138/BEA | DEMUX | 54F163A/BEA | COUNTER |
| 54F00/BDA | GATE | 54F138/BFA | DEMUX | 54F163A/BFA | COUNTER |
| 54F00/B2A | GATE | 54F138/B2A | DEMUX | 54F163A/B2A | COUNTER |
| 54F02/BCA | GATE | 54F125/BCA | BUFFER | 54F164/B2A | S REG |
| 54F02/BDA | GATE | 54F125/BDA | BUFFER | 54F164/BCA | S REG |
| 54F02/B2A | GATE | 54F125/B2A | BUFFER | 54F164/BDA | S REG |
| 54F04/BCA | MUX | 54F139/BEA | DEMUX | 54F169/BEA | COUNTER |
| 54F04/BDA | MUX | 54F139/BFA | DEMUX | 54F169/BFA | COUNTER |
| 54F04/B2A | MUX | 54F139/B2A | DEMUX | 54F169/B2A | COUNTER |
| 54F08/BCA | GATE | 54F14/BCA | SCHMITT | 54F173/BEA | QUAD FF |
| 54F08/BDA | GATE | 54F14/BDA | SCHMITT | 54F173/BFA | QUAD FF |
| 54F08/B2A | GATE | 54F14/B2A | SCHMITT | 54F173/B2A | QUAD FF |
| 54F10/BCA | GATE | 54F148/BEA | ENCODER | 54F174/BEA | HEX FF |
| 54F10BDA | GATE | 54F148/BFA | ENCODER | 54F174/BFA | HEX FF |
| 54F10/B2A | GATE | 54F148/B2A | ENCODER | 54F174/B2A | HEX FF |
| 54F109/BEA | DUAL FF | 54F151/BEA | MUX | 54F175/BEA | QUAD FF |
| 54F109/BFA | DUAL FF | 54F151/BFA | MUX | 54F175/BFA | QUAD FF |
| 54F109/B2A | DUAL FF | 54F151B2A | MUX | 54F175/B2A | QUAD FF |
| 54F11/BCA | GATE | 54F154/BLA | DEMUX | 54F181/BJA | ALU |
| 54F11/BDA | GATE | 54F154/BKA | DEMUX | 54F181/BLA | ALU |
| 54F11/B2A | GATE | 54F154/B3A | DEMUX | 54F181/BKA | ALU |
| 54F112/BEA | DUAL FF | 54F157A/BEA | MUX | 54F181/B3A | ALU |
| 54F112/BFA | DUAL FF | 54F157A/BFA | MUX | 54F190/BEA | COUNTER |
| 54F112/B2A | DUAL FF | 54F157A/B2A | MUX | 54F190/BFA | COUNTER |
| 54F113/BCA | DUAL FF | 54F158A/BEA | MUX | 54F190/B2A | COUNTER |
| 54F113/BDA | DUAL FF | 54F158A/BFA | MUX | 54F191/BEA | COUNTER |
| 54F113/B2A | DUAL FF | 54F158A/B2A | MUX | 54F191/BFA | COUNTER |
| 54F1240/BRA | OCT BUFFER | 54F161A/BEA | COUNTER | 54F191/B2A | COUNTER |
| 54F1240/BSA | OCT BUFFER | 54F161A/BFA | COUNTER | 54F193/BEA | COUNTER |
| 54F1240/B2A | OCT BUFFER | 54F161A/B2A | COUNTER | 54F193/BFA | COUNTER |

# Product Listing of Contents of Volume 2

## FAST LOGIC PRODUCTS (Continued)

| Part Number | Device Description | Part Number | Device Description | Part Number | Device Description |
|---|---|---|---|---|---|
| 54F193/B2A | COUNTER | 54F30244/B3A | OCT BUFFER | 54F538/BSA | DECODER |
| 54F194/BEA | S REG | 54F30245/BKA | OCT XCVR | 54F538/B2A | DECODER |
| 54F194/BFA | S REG | 54F30245/BLA | OCT XCVR | 54F543/BKA | OCT XCVR |
| 54F194/B2A | S REG | 54F30245/B3A | OCT XCVR | 54F543/BLA | OCT XCVR |
| 54F198/BKA | S REG | 54F3037/BEA | BUFFER | 54F543/B3A | OCT XCVR |
| 54F198/BLA | S REG | 54F3037/BFA | BUFFER | 54F544/BKA | OCT XCVR |
| 54F198/B3A | S REG | 54F3037/B2A | BUFFER | 54F544/BLA | OCT XCVR |
| 54F20/BCA | GATE | 54F32/BCA | GATE | 54F544/B3A | OCT XCVR |
| 54F20/BDA | GATE | 54F32/BDA | GATE | 54F573/BRA | OCT LATCH |
| 54F20/B2A | GATE | 54F32/B2A | GATE | 54F573/BSA | OCT LATCH |
| 54F240/BRA | OCT BUFFER | 54F350/BEA | SHIFTER | 54F573/B2A | OCT LATCH |
| 54F240/BSA | OCT BUFFER | 54F350/BFA | SHIFTER | 54F574/BRA | OCT FF |
| 54F240/B2A | OCT BUFFER | 54F350B2A | SHIFTER | 54F574/BSA | OCT FF |
| 54F241/BRA | OCT BUFFER | 54F367/BEA | HEX BUFFER | 54F574/B2A | OCT FF |
| 54F241/BSA | OCT BUFFER | 54F367/BFA | HEX BUFFER | 54F579/BRA | COUNTER |
| 54F241/B2A | OCT BUFFER | 54F367/B2A | HEX BUFFER | 54F579/BSA | COUNTER |
| 54F244/BRA | OCT BUFFER | 54F37/BCA | BUFFER | 54F579/B2A | COUNTER |
| 54F244/BSA | OCT BUFFER | 54F37/BDA | BUFFER | 54F620/BRA | OCT XCVR |
| 54F244/B2A | OCT BUFFER | 54F37/B2A | BUFFER | 54F620/BSA | OCT XCVR |
| 54F245/BRA | OCT XCVR | 54F373/BRA | OCT LATCH | 54F620/B2A | OCT XCVR |
| 54F245/BSA | OCT XCVR | 54F373/BSA | OCT LATCH | 54F623/BRA | XCVR |
| 54F245/B2A | OCT XCVR | 54F373/B2A | OCT LATCH | 54F623/BSA | XCVR |
| 54F251/BEA | MUX | 54F374/BRA | OCT FF | 54F623/B2A | XCVR |
| 54F251/BFA | MUX | 54F374/BSA | OCT FF | 54F64/BCA | GATE |
| 54F251/B2A | MUX | 54F374/B2A | OCT FF | 54F64/BDA | GATE |
| 54F253/BEA | MUX | 54F38/BCA | OCT BUFFER | 54F64/B2A | GATE |
| 54F253/BFA | MUX | 54F38/BDA | OCT BUFFER | 54F640/BRA | OCT XCVR |
| 54F253/B2A | MUX | 54F38/B2A | OCT BUFFER | 54F640/BSA | OCT XCVR |
| 54F257A/BEA | MUX | 54F398/BRA | REGISTER | 54F640/B2A | OCT XCVR |
| 54F257A/BFA | MUX | 54F398/BSA | REGISTER | 54F655A/BKA | BUFFER |
| 54F257A/B2A | MUX | 54F398/B2A | REGISTER | 54F655A/BLA | BUFFER |
| 54F258A/BEA | MUX | 54F399/BEA | REGISTER | 54F655A/B3A | BUFFER |
| 54F258A/BFA | MUX | 54F399/BFA | REGISTER | 54F656A/BKA | BUFFER |
| 54F258A/B2A | MUX | 54F399/B2A | REGISTER | 54F656A/BLA | BUFFER |
| 54F259/BEA | LATCH | 54F432/BKA | LATCH | 54F656A/B3A | BUFFER |
| 54F259/BFA | LATCH | 54F432/BLA | LATCH | 54F657/BKA | OCT XCVR |
| 54F259/B2A | LATCH | 54F432/B3A | LATCH | 54F657/BLA | OCT XCVR |
| 54F269/BKA | COUNTER | 54F455/BKA | OCT BUFFER | 54F657/B3A | OCT XCVR |
| 54F269/BLA | COUNTER | 54F455/BLA | OCT BUFFER | 54F676/BKA | SHIFT REG |
| 54F269/B3A | COUNTER | 54F455/B3A | OCT BUFFER | 54F676/BLA | SHIFT REG |
| 54F273/BRA | OCT FF | 54F51/BCA | GATE | 54F676/B3A | SHIFT REG |
| 54F273/BSA | OCT FF | 54F51/BDA | GATE | 54F74/BCA | DUAL FF |
| 54F273/B2A | OCT FF | 54F51/B2A | GATE | 54F74/BDA | DUAL FF |
| 54F280A/BEA | PARITY | 54F521/BRA | OCT COMP | 54F74/B2A | DUAL FF |
| 54F280A/BFA | PARITY | 54F521/BSA | OCT COMP | 54F776/BXA | PI–BUS |
| 54F280A/B2A | PARITY | 54F521/B2A | OCT COMP | 54F776/BYA | PI–BUS |
| 54F299/BRA | S REG | 54F534/BRA | OCT FF | 54F776/B3A | PI–BUS |
| 54F299/BSA | S REG | 54F534/BSA | OCT FF | 54F779/BEA | COUNTER |
| 54F299/B2A | S REG | 54F534/B2A | OCT FF | 54F779/BFA | COUNTER |
| 54F30244/BKA | OCT BUFFER | 54F538/BRA | DECODER | 54F779B2A | COUNTER |
| 54F30244/BLA | OCT BUFFER | | | | |

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## SECTION 3:
## LOW POWER SCHOTTKY LOGIC PRODUCTS

| Part Number | Device Description | Part Number | Device Description | Part Number | Device Description |
|---|---|---|---|---|---|
| 54LS00/BCA | GATE | 54LS173/B2A | QUAD FF | 54LS295B/BDA | S REG |
| 54LS00/BDA | GATE | 54LS174/BEA | HEX FF | 54LS295B/B2A | S REG |
| 54LS00/B2A | GATE | 54LS174/BFA | HEX FF | 54LS32/BCA | GATE |
| 54LS02/BCA | GATE | 54LS174/B2A | HEX FF | 54LS32/BDA | GATE |
| 54LS02/BDA | GATE | 54LS175/BEA | QUAD FF | 54LS32/B2A | GATE |
| 54LS02/B2A | GATE | 54LS175/BFA | QUAD FF | 54LS365A/BEA | HEX BUF |
| 54LS04/BCA | INVTR | 54LS175/B2A | QUAD FF | 54LS365A/BFA | HEX BUF |
| 54LS04/BDA | INVTR | 54LS191/BEA | COUNTER | 54LS365A/B2A | HEX BUF |
| 54LS04/B2A | INVTR | 54LS191/BFA | COUNTER | 54LS367A/BEA | HEX BUF |
| 54LS08/BCA | GATE | 54LS191B2A | COUNTER | 54LS367A/BFA | HEX BUF |
| 54LS08/BDA | GATE | 54LS193/BEA | COUNTER | 54LS367A/B2A | HEX BUF |
| 54LS08/B2A | GATE | 54LS193/BFA | COUNTER | 54LS368A/BEA | INVTR |
| 54LS10/BCA | GATE | 54LS193/B2A | COUNTER | 54LS368A/BFA | INVTR |
| 54LS10/BDA | GATE | 54LS195A/BEA | S REG | 54LS368A/B2A | INVTR |
| 54LS10/B2A | GATE | 54LS195A/BFA | S REG | 54LS37/SCA | BUFFER |
| 54LS109/BEA | DUAL FF | 54LS195A/B2A | S REG | 54LS37/SDA | BUFFER |
| 54LS109/BFA | DUAL FF | 54LS197/BCA | COUNTER | 54LS373/BRA | OCT LATCH |
| 54LS109/B2A | DUAL FF | 54LS197/BDA | COUNTER | 54LS373/BSA | OCT LATCH |
| 54LS112/SEA | DUAL FF | 54LS197/B2A | COUNTER | 54LS373/B2A | OCT LATCH |
| 54LS112/SFA | DUAL FF | 54LS20/BCA | GATE | 54LS374/BRA | OCT FF |
| 54LS125/BCA | QUAD BUF | 54LS20/BDA | GATE | 54LS374/BSA | OCT FF |
| 54LS125/BDA | QUAD BUF | 54LS20/B2A | GATE | 54LS374/B2A | OCT FF |
| 54LS125/B2A | QUAD BUF | 54LS240/BRA | OCT BUFF | 54LS377/BRA | OCT FF |
| 54LS132/BCA | SCHMITT | 54LS240/BSA | OCT BUFF | 54LS377/BSA | OCT FF |
| 54LS132/BDA | SCHMITT | 54LS240/B2A | OCT BUFF | 54LS377/B2A | OCT FF |
| 54LS138/BEA | DEMUX | 54LS241/BRA | OCT BUFF | 54LS393/BCA | COUNTER |
| 54LS138/BFA | DEMUX | 54LS241/BSA | OCT BUFF | 54LS393/BDA | COUNTER |
| 54LS138/B2A | DEMUX | 54LS241/B2A | OCT BUFF | 54LS393/B2A | COUTNER |
| 54LS14/BCA | SCHMITT | 54LS244/BRA | OCT BUFF | 54LS395A/BEA | S REG |
| 54LS14/BDA | SCHMITT | 54LS244/BSA | OCT BUFF | 54LS395A/BFA | S REG |
| 54LS14/B2A | SCHMITT | 54LS244/B2A | OCT BUFF | 54LS395A/B2A | S REG |
| 54LS153/BFA | MUX | 54LS245/BRA | XCVR | 54LS74A/BCA | DUAL FF |
| 54LS153/SEA | MUX | 54LS245/BSA | XCVR | 54LS74A/BDA | DUAL FF |
| 54LS154/BJA | DEMUX | 54LS245/B2A | XCVR | 54LS74A/B2A | DUAL FF |
| 54LS154/BKA | DEMUX | 54LS257A/BEA | MUX | 54LS75/BEA | QUAD LTCH |
| 54LS161A/BEA | COUNTER | 54LS257A/BFA | MUX | 54LS75/BFA | QUAD LTCH |
| 54LS161A/BFA | COUNTER | 54LS257A/B2A | MUX | 54LS75/B2A | QUAD LTCH |
| 54LS161A/B2A | COUNTER | 54LS258A/BEA | MUX | 54LS85/BEA | COMP |
| 54LS163A/BEA | COUNTER | 54LS258A/BFA | MUX | 54LS85/BFA | COMP |
| 54LS163A/BFA | COUNTER | 54LS258A/B2A | MUX | 54LS85/B2A | COMP |
| 54LS163A/B2A | COUNTER | 54LS26/SCA | GATE | 54LS86/BCA | GATE |
| 54LS164/BCA | S REG | 54LS26/SDA | GATE | 54LS86/BDA | GATE |
| 54LS164/BDA | S REG | 54LS273/BRA | OCT FF | 54LS86/B2A | GATE |
| 54LS164/B2A | S REG | 54LS273/BSA | OCT FF | 54LS95B/BCA | S REG |
| 54LS173/BEA | QUAD FF | 54LS273/B2A | OCT FF | 54LS95B/BDA | S REG |
| 54LS173/BFA | QUAD FF | 54LS295B/BCA | S REG | | |

# Product Listing of Contents of Volume 2

## SECTION 4.
## SCHOTTKY LOGIC PRODUCTS

| Part Number | Device Description | Part Number | Device Description | Part Number | Device Description |
|---|---|---|---|---|---|
| 54S00/BCA | GATE | 54S151/BEA | MUX | 54S251/BFA | MUX |
| 54S00/BDA | GATE | 54S151/BFA | MUX | 54S251/B2A | MUX |
| 54S00/B2A | GATE | 54S151/B2A | MUX | 54S253/BEA | MUX |
| 54S02/BCA | GATE | 54S153/BEA | MUX | 54S253/BFA | MUX |
| 54S02/BDA | GATE | 54S153/BFA | MUX | 54S253/B2A | MUX |
| 54S02/B2A | GATE | 54S153/B2A | MUX | 54S273/BRA | OCT FF |
| 54S04/BCA | INVTR | 54S157/BEA | MUX | 54S273/BSA | OCT FF |
| 54S04/BDA | INVTR | 54S157/BFA | MUX | 54S273/B2A | OCT FF |
| 54S04/B2A | INVTR | 54S157/B2A | MUX | 54S373/BEA | OCT LATCH |
| 54S08/BCA | GATE | 54S158/BEA | MUX | 54S373/BSA | OCT LATCH |
| 54S08/B2A | GATE | 54S158/BFA | MUX | 54S373/B2A | OCT LATCH |
| 54S08/B2A | GATE | 54S158/B2A | MUX | 54S374/BRA | OCT FF |
| 54S10/BCA | GATE | 54S174/BEA | HEX FF | 54S374/BSA | OCT FF |
| 54S10/BDA | GATE | 54S174/BFA | HEX FF | 54S374/B2A | OCT FF |
| 54S10/B2A | GATE | 54S174/B2A | HEX FF | 54S40/BCA | DUAL BUFF |
| 54S11/BCA | GATE | 54S181/BJA | ALU | 54S40/BDA | DUAL BUFF |
| 54S11/BDA | GATE | 54S181/B3A | ALU | 54S40/B2A | DUAL BUFF |
| 54S11/B2A | GATE | 54S20/BCA | GATE | 54S51/BCA | GATE |
| 54S113/BCA | DUAL FF | 54S20/BDA | GATE | 54S51/BDA | GATE |
| 54S113/BDA | DUAL FF | 54S20/B2A | GATE | 54S51/B2A | GATE |
| 54S113/B2A | DUAL FF | 54S240/BRA | OCT BUFF | 54S74/BCA | DUAL FF |
| 54S133/BEA | GATE | 54S240/BSA | OCT BUFF | 54S74/BDA | DUAL FF |
| 54S133/BFA | GATE | 54S240/B2A | OCT BUFF | 54S74/B2A | DUAL FF |
| 54S133/B2A | GATE | 54S241/BRA | OCT BUFF | 54S85/BEA | COMP |
| 54S138/BEA | DEMUX | 54S241/BSA | OCT BUFF | 54S85/BFA | COMP |
| 54S138/.BFA | DEMUX | 54S241/B2A | OCT BUFF | 54S85/B2A | COMP |
| 54S138/B2A | DEMUX | 54S244/BRA | OCT BUFF | 54S86/BCA | COMP |
| 54S140/BCA | DRIVER | 54S244/BSA | OCT BUFF | 54S86/B2A | COMP |
| 54S140/BDA | DRIVER | 54S244/B2A | OCT BUFF | 54S86/BDA | GATE |
| 54S140/B2A | DRIVER | 54S251/BEA | MUX | 8T26A/BEA | XCVR |

## SECTION 5:
## GOLD DOPED LOGIC PRODUCTS

| Part Number | Device Description | Part Number | Device Description | Part Number | Device Description |
|---|---|---|---|---|---|
| 5400/BCA | GATE | 54164/BCA | S REG | 54365A/BEA | HEX BUFF |
| 5400/BDA | GATE | 54174/BEA | HEX FF | 53367A/BEA | HEX BUFF |
| 5404/BCA | INVTR | 54174/BFA | HEX FF | 54368A/BEA | INVTR |
| 5404/BDA | INVTR | 54175/BEA | QUAD FF | 5485/BEA | COMP |
| 54123/BEA | MVBTR | 54175/BFA | QUAD FF | 5485/BFA | COMP |
| 54126/BCA | QUAD BUFF | 54193/BEA | COUNTER | 5493/BCA | COUNTER |
| 54161/BEA | COUNTER | 54194/BEA | S REG | 5493/BDA | COUNTER |
| 54161/BFA | COUNTER | 54194/BFA | S REG | 8T09/BCA | DRIVER |
| 54163/BEA | COUNTER | 5432/BCA | GATE | 8T09/BDA | DRIVER |
| 54163/BFA | COUNTER | 5432/BDA | GATE | | |

# Product Listing of Contents of Volume 2

## SECTION 6:
## BIPOLAR PROM PRODUCTS

| Part Number | Device Description | Part Number | Device Description | Part Number | Device Description |
|---|---|---|---|---|---|
| 82HS187/BLA | 8K REG | 82HS641A/B3A | 8KX8–100 | 82S137A/BYA | 1KX4 |
| 82HS187/B3X | 8K REG | 82HS641B/BJA | 8KX8–35 | 82S141/BJA | 512X8 |
| 82HS187A/BLA | 8K REG | 82HS641B/B3A | 8KX8–35 | 82S141/BKA | 512X8 |
| 82HS187A/B3A | 8K REG | 82LS181/BJA | 1KX8 | 82S147/BRA | 512X8 |
| 82HS189/BLA | 8K REG | 82LS181/B3A | 1KX8 | 82S147A/BRA | 512X8 |
| 82HS189/B3A | 8K REG | 82LS181A/BJA | 1KX8 | 82S147B/BRA | 512X8 |
| 82HS189A/BLA | 8K REG | 82LS181A/B3A | 1KX8 | 82S181/BJA | 1KX8 |
| 82HS189A/B3A | 8K REG | 82LS181B/BJA | 1KX8 | 82S181/BKA | 1KX8 |
| 82HS191/BJA | 2KX8 | 82S115/BJA | 512X8 | 82S181/B3A | 1KX8 |
| 82HS191/B3A | 2KX8 | 82S115/BKA | 512X8 | 82S181A/BJA | 1KX8 |
| 82HS195A/BRA | 4KX4 | 82S123/BEA | 32X8 | 82S181A/BKA | 1KX8 |
| 82HS321A/BJA | 4KX8–45 | 82S123/BFA | 32X8 | 82S181A/B3A | 1KX8 |
| 82HS321A/BJA | 4KX8–55 | 82S123A/BEA | 32X8 | 82S185/BVA | 2KX4 |
| 82HS321A/BJA | 4KX8–85 | 82S123A/BFA | 32X8 | 82S185/BYA | 2KX4 |
| 82HS321A/BJA | 4KX8–95 | 82S123B/BEA | 32X8 | 82S185A/BVA | 2KX4 |
| 82HS321A/BKA | 4KX8–45 | 82S123B/BFA | 32X8 | 82S185A/BYA | 2KX4 |
| 82HS321A/BKA | 4KX8–55 | 82S126/BEA | 256X4 | 82S191/BJA | 2KX8 |
| 82HS321A/BKA | 4KX8–95 | 82S126/BFA | 256X4 | 82S191/BKA | 2KX8 |
| 82HS321A/B3A | 4KX8–45 | 82S126A/BEA | 256X4 | 82S191/BLA | 2KX8 |
| 82HS321A/B3A | 4KX8–55 | 82S126A/BFA | 256X4 | 82S191/B3A | 2KX8 |
| 82HS321A/B3A | 4KX8–85 | 82S129/BEA | 256X4 | 82S191A/BJA | 2KX8 |
| 82HS321A/B3A | 4KX8–95 | 82S129/BFA | 256X4 | 82S191A/BKA | 2KX8 |
| 82HS321B/BLA | 4KX8–35 | 82S129A/BEA | 256X4 | 82S191A/BLA | 2KX8 |
| 82HS321B/BJA | 4KX8–35 | 82S129A/BFA | 256X4 | 82S191A/B3A | 2KX8 |
| 82HS321B/BKA | 4KX8–35 | 82S130/BEA | 512X4 | 82S23/BEA | 32X8 |
| 82HS321B/B3A | 4KX8–35 | 82S130/BFA | 512X4 | 82S23/BFA | 32X8 |
| 82HS641/BJA | 8KX8–100 | 82S130A/BEA | 512X4 | 82S23A/BEA | 32X8 |
| 82HS641/BJA | 8KX8–100 | 82S130A/BFA | 512X4 | 82S23A/BFA | 32X8 |
| 82HS641/BJA | 8KX8–50 | 82S131/BEA | 512X4 | 82S23B/BEA | 32X8 |
| 82HS641/BJA | 8KX8–55 | 82S131/BFA | 512X4 | 82S23B/BFA | 32X8 |
| 82HS641/BJA | 8KX8–70 | 82S131A/BEA | 512X4 | 82S2708/BJA | 1KX8 |
| 82HS641A/B3A | 8KX8–45 | 82S131A/BFA | 512X4 | 82S291A/BLA | 2KX8 |
| 82HS641A/B3A | 8KX8–50 | 82S137/BVA | 1KX4 | 82US123/BEA | 32X8 |
| 82HS641A/B3A | 8KX8–55 | 82S137/BYA | 1KX4 | 82US23/BEA | 32X8 |
| 82HS641A/B3A | 8KX8–70 | 82S137A/BVA | 1KX4 | | |

## SECTION 7:
## RANDOM ACCESS MEMORY PRODUCTS

| Part Number | Device Description | Part Number | Device Description | Part Number | Device Description |
|---|---|---|---|---|---|
| 54S189/BEA | 16X4 | 82S09/BXA | 64X9 | 82S16/BFA | 256X1 |
| 54S189/BFA | 16X4 | 82S09/BYA | 64X9 | 82S212/BWA | 256X9 |
| 8X350/BWA | 256X8 | 82S16/BEA | 256X1 | 82S212/BWA–40 | 256X9 |
| 8X350/B3A | 256X8 | | | | |

# NOTES

# NOTES

# NOTES

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Last name _____ First name _____

Company _____

Department or Division _____

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Area code _____ Phone number _____ Extension _____

**YES**, I would like more information about Signetics Military Products.

( ) Please send a Military Products Handbook. Volume 1 ( ) Volume 2 ( )

( ) My current Military Application is: _____

( ) Please have a salesman call.

**1. Your company and its products/services fit into the following category:**

( ) Aerospace
( ) Consumer Products
( ) Computers
( ) Computer Peripherals
( ) Communications Products
( ) Basic Chemicals/ Petroleum
( ) Instruments & Controls
( ) Utilities
( ) Office & Business Machines
( ) Telecommunications Products
( ) Bio/Medical Products
( ) Transportation
( ) Research & Development
( ) Industrial Equipment
( ) Defense & Military
( ) Government Agency
( ) Electronics System Integration
( ) Components & Sub–Assemblies
( ) Electrical Equipment
( ) Test & Measurement Equipment
( ) Auto/Truck/Bus Manufacturing
( ) Scientific Equipment
( ) Educational Institution
( ) Other _____

**2. Your location is the:**

( ) Company Headquarters
( ) Regional Headquarters
( ) Division Headquarters
( ) Military Facility
( ) Sales Office
( ) R & D Lab
( ) Engineering/Design Facility
( ) Distribution Facility
( ) Manufacturing Facility
( ) Repair/Retrofit Facility
( ) Other _____

**3. Number of employees at your location:** ( ) 1–250 ( ) 251–500 ( ) 501–1000 ( ) More than 1000

**4. Number of engineers at your location:** _____

**5. Approximate annual company billings:** ( ) Don't Know ( ) Under $5mm ( ) $5mm to $10mm ( ) $10mm to $100mm ( ) Over $100mm

**6. Would you like a sales engineer to call you?** ( ) YES ( ) NO

**7. Please indicate your area(s) of specific product interest by checking the block(s) below:**

( ) **Digital Logic**
( ) TTL/LS/S
( ) 10K/100K ECL
( ) FAST
( ) HC/HCT/CMOS
( ) 400 Series CMOS
( ) ACL
( ) ALS
( ) **Memory**
( ) RAM/DRAM/SRAM
( ) ROM
( ) PROM
( ) EPROM/OTP
( ) DRAM Controller
( ) FIFO
( ) **Microprocessor**
( ) 68000 Family
( ) 68000 Peripherals
( ) Data Communications
( ) CRT/Graphics
( ) DSP
( ) **Surface Mount Devices**
( ) SO
( ) PLCC
( ) LCC
( ) **VME Interface Devices**
( ) MPU
( ) Memory
( ) Data Communications
( ) Disc Controller
( ) VME/VMS Bus Controller
( ) **Military & Govt. Products** (All As Required)
( ) **Other Products**
( ) **Linear Products**
( ) Amplifier
( ) Communication
( ) Video
( ) Power Conversion
( ) Interface/Data Conversion
( ) Small Area Networks
( ) **ASIC/Semicustom Products**
( ) Bipolar Std. Cell (CCL)
( ) CMOS Standard Cell (Semicustom)
( ) Gate Arrays
( ) Programmable Logic Devices (PLD)
( ) PAL®
( ) Software
( ) **Microcontroller**
( ) NMOS/CMOS Family
( ) Bipolar Family
( ) 80C51 Derivatives
( ) OTP Microcontroller
( ) $1^2C$ Microcontroller

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**8. Your primary job responsibility/title is (check one only):**

**MANAGEMENT**
( ) Senior Corp Manager
( ) Engineering Manager
( ) Financial
( ) Purchasing/ Procurement
( ) Production
( ) Project
( ) Other

**ENGINEERING**
( ) Section Leader
( ) Group Leader
( ) Project Engineer
( ) Design
( ) Aerospace
( ) Applications
( ) Component Evaluation
( ) Software
( ) Mechanical
( ) Materials Specifications
( ) Production
( ) Systems
( ) Ocean/Naval
( ) Quality Assurance
( ) Other

**PURCHASING/ PROCUREMENT**
( ) Electronics Buyer
( ) General Purchasing Agent
( ) Production Component Buyer
( ) Engineering Buyer
( ) Other

**EDUCATION/ INSTRUCTION**
( ) Professor
( ) Asst. Professor
( ) Instructor
( ) Industrial Instructor
( ) Student
( ) Research Scientist

**CONSULTING**
( ) Government
( ) Military
( ) Product Design
( ) Software Development
( ) Electronics Systems Design
( ) Systems Integration
( ) Component Evaluation
( ) Other

**9. Do you recommend, specify, approve or direct purchasing of electronic components?**

( ) Yes
( ) No

If yes, which of these:

( ) Digital Logic
( ) Linear
( ) ASIC/Semi Custom
( ) PLDS
( ) Memory
( ) Microprocessor
( ) Microcontroller
( ) Microsystems/VME Bus
( ) SMD
( ) Military
( ) Other

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